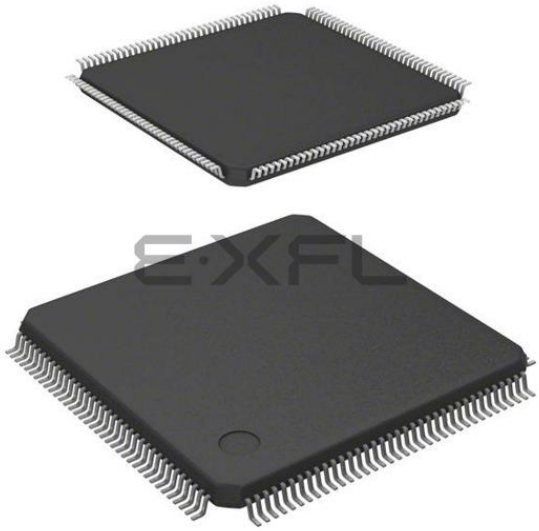

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f415zgt6

Table 2. STM32F415xx and STM32F417xx: features and peripheral counts

Peripherals	STM32F415RG	STM32F415OG	STM32F415VG	STM32F415ZG	STM32F417Vx	STM32F417Zx	STM32F417Ix
GPIOs	51	72	82	114	82	114	140
12-bit ADC Number of channels	3						
	16	13	16	24	16	24	24
12-bit DAC Number of channels	Yes 2						
Maximum CPU frequency	168 MHz						
Operating voltage	1.8 to 3.6 V(3)						
Operating temperatures	Ambient temperatures: –40 to +85 °C /–40 to +105 °C						
	Junction temperature: –40 to + 125 °C						
Package	LQFP64	WLCSP90	LQFP100	LQFP144	LQFP100	LQFP144	UFBGA176 LQFP176

1. For the LQFP100 and WLCSP90 packages, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to *Section : Internal reset OFF*).

Table 5. USART feature comparison

USART name	Standard features	Modem (RTS/ CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s (oversampling by 16)	Max. baud rate in Mbit/s (oversampling by 8)	APB mapping
USART1	X	X	X	X	X	X	5.25	10.5	APB2 (max. 84 MHz)
USART2	X	X	X	X	X	X	2.62	5.25	APB1 (max. 42 MHz)
USART3	X	X	X	X	X	X	2.62	5.25	APB1 (max. 42 MHz)
UART4	X	-	X	-	X	-	2.62	5.25	APB1 (max. 42 MHz)
UART5	X	-	X	-	X	-	2.62	5.25	APB1 (max. 42 MHz)
USART6	X	X	X	X	X	X	5.25	10.5	APB2 (max. 84 MHz)

2.2.24 Serial peripheral interface (SPI)

The STM32F41xxx feature up to three SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1 can communicate at up to 42 Mbits/s, SPI2 and SPI3 can communicate at up to 21 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

2.2.25 Inter-integrated sound (I^2S)

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) are available. They can be operated in master or slave mode, in full duplex and half-duplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I^2Sx can be served by the DMA controller.

Table 7. STM32F41xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
-	A8	-	143	C6	171	PDR_ON	I	FT	-	-	-
64	A1	100	144	C5	172	V_{DD}	S	-	-	-	-
-	-	-	-	D4	173	PI4	I/O	FT	-	TIM8_BKIN / DCMI_D5/ EVENTOUT	-
-	-	-	-	C4	174	PI5	I/O	FT	-	TIM8_CH1 / DCMI_VSYNC/ EVENTOUT	-
-	-	-	-	C3	175	PI6	I/O	FT	-	TIM8_CH2 / DCMI_D6/ EVENTOUT	-
-	-	-	-	C2	176	PI7	I/O	FT	-	TIM8_CH3 / DCMI_D7/ EVENTOUT	-

1. Function availability depends on the chosen device.
2. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).
3. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F4xx reference manual, available from the STMicroelectronics website: *www.st.com*.
4. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
5. If the device is delivered in an UFBGA176 or WLCSP90 and the BYPASS_REG pin is set to VDD (Regulator off/internal reset ON mode), then PA0 is used as an internal Reset (active low).

Table 8. FSMC pin definition

Pins(1)	FSMC				LQFP100(2)	WLCSP90 (2)
	CF	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit		
PE2	-	A23	A23	-	Yes	-
PE3	-	A19	A19	-	Yes	-
PE4	-	A20	A20	-	Yes	-
PE5	-	A21	A21	-	Yes	-
PE6	-	A22	A22	-	Yes	-
PF0	A0	A0	-	-	-	-

Table 9. Alternate function mapping (continued)

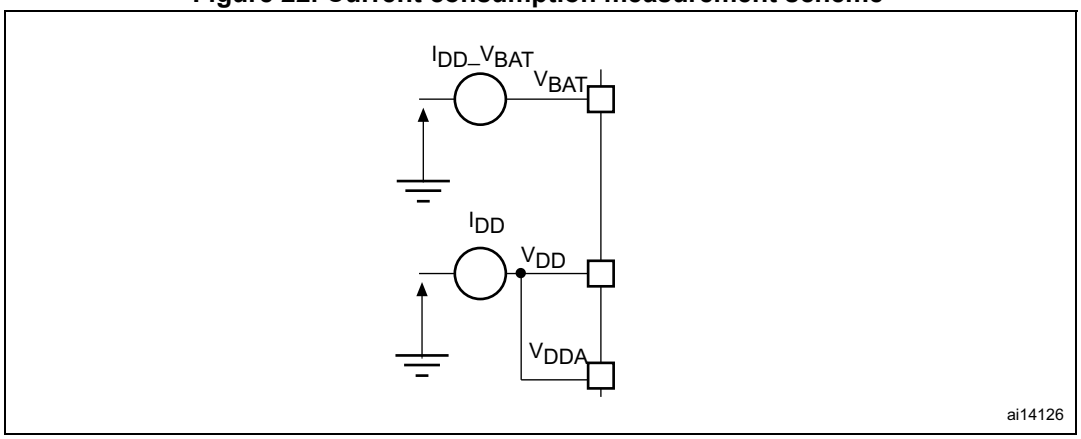
Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/I2S2/I2S2ext	SPI3/I2Sext/I2S3	USART1/2/3/I2S3ext	UART4/5/USART6	CAN1/2 TIM12/13/14	OTG_FS/OTG_HS	ETH	FSMC/SDIO/OTG_FS	DCMI		
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	-	-	-	-	OTG_HS_ULPI_D1	ETH _MII_RXD2	-	-	-	EVENTOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N		-	-	-	-	-	OTG_HS_ULPI_D2	ETH _MII_RXD3	-	-	-	EVENTOUT
	PB2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB3	JTDO/TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK I2S3_CK	-	-	-	-	-	-	-	-	EVENTOUT
	PB4	NJTRST	-	TIM3_CH1		-	SPI1_MISO	SPI3_MISO	I2S3ext_SD	-	-	-	-	-	-	-	EVENTOUT
	PB5	-	-	TIM3_CH2		I2C1_SMBA	SPI1_MOSI	SPI3_MOSI I2S3_SD		-	CAN2_RX	OTG_HS_ULPI_D7	ETH _PPS_OUT	-	DCMI_D10	-	EVENTOUT
	PB6	-	-	TIM4_CH1		I2C1_SCL	-	-	USART1_TX	-	CAN2_TX	-	-	-	DCMI_D5	-	EVENTOUT
	PB7	-	-	TIM4_CH2		I2C1_SDA	-	-	USART1_RX	-	-	-	-	FSMC_NL	DCMI_VSYNC	-	EVENTOUT
	PB8	-	-	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	-	-	-	CAN1_RX	-	ETH _MII_TXD3	SDIO_D4	DCMI_D6	-	EVENTOUT
	PB9	-	-	TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS I2S2_WS	-	-	-	CAN1_TX	-	-	SDIO_D5	DCMI_D7	-	EVENTOUT
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK I2S2_CK	-	USART3_TX	-	-	OTG_HS_ULPI_D3	ETH_ MII_RX_ER	-	-	-	EVENTOUT
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	-	USART3_RX	-	-	OTG_HS_ULPI_D4	ETH _MII_TX_EN ETH _RMII_TX_EN	-	-	-	EVENTOUT
	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS I2S2_WS	-	USART3_CK	-	CAN2_RX	OTG_HS_ULPI_D5	ETH _MII_TXD0 ETH _RMII_TXD0	OTG_HS_ID	-	-	EVENTOUT
	PB13	-	TIM1_CH1N	-	-	-	SPI2_SCK I2S2_CK	-	USART3_CTS	-	CAN2_TX	OTG_HS_ULPI_D6	ETH _MII_TXD1 ETH _RMII_TXD1	-	-	-	EVENTOUT
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	-	SPI2_MISO	I2S2ext_SD	USART3_RTS	-	TIM12_CH1	-	-	OTG_HS_DM	-	-	EVENTOUT
	PB15	RTC_REFIN	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI I2S2_SD	-	-	-	TIM12_CH2	-	-	OTG_HS_DP	-	-	EVENTOUT

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/I2S2/I2S2ext	SPI3/I2Sext/I2S3	USART1/2/3/I2S3ext	UART4/5/USART6	CAN1/2 TIM12/13/14	OTG_FS/OTG_HS	ETH	FSMC/SDIO/OTG_FS	DCMI		
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	FSMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	-	FSMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	-	FSMC_A2	-	-	EVENTOUT
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A3	-	-	EVENTOUT
	PF4	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A4	-	-	EVENTOUT
	PF5	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A5	-	-	EVENTOUT
	PF6	-	-	-	TIM10_CH1	-	-	-	-	-	-	-	-	FSMC_NIORD	-	-	EVENTOUT
	PF7	-	-	-	TIM11_CH1	-	-	-	-	-	-	-	-	FSMC_NREG	-	-	EVENTOUT
	PF8	-	-	-	-	-	-	-	-	-	TIM13_CH1	-	-	FSMC_NIOWR	-	-	EVENTOUT
	PF9	-	-	-	-	-	-	-	-	-	TIM14_CH1	-	-	FSMC_CD	-	-	EVENTOUT
	PF10	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_INTR	-	-	EVENTOUT
	PF11	-	-	-	-	-	-	-	-	-	-	-	-		DCMI_D12	-	EVENTOUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A6	-	-	EVENTOUT
	PF13	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A7	-	-	EVENTOUT
	PF14	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A8	-	-	EVENTOUT
	PF15	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A9	-	-	EVENTOUT

5.1.7 Current consumption measurement

Figure 22. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 11: Voltage characteristics*, *Table 12: Current characteristics*, and *Table 13: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 11. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{DD})(1)	–0.3	4.0	V
V_{IN}	Input voltage on five-volt tolerant pin(2)	V_{SS}–0.3	V_{DD}+4	
	Input voltage on any other pin	V_{SS}–0.3	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins including V_{REF-}	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.14: Absolute maximum ratings (electrical sensitivity)*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum value must always be respected. Refer to *Table 12* for the values of the maximum allowed injected current.

Table 15. Limitations depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait state ($f_{Flashmax}$)	Maximum Flash memory access frequency with wait states(1) (2)	I/O operation	Clock output Frequency on I/O pins	Possible Flash memory operations
V_{DD} =1.8 to 2.1 V(3)	Conversion time up to 1.2 Msps	20 MHz(4)	160 MHz with 7 wait states	– Degraded speed performance – No I/O compensation	up to 30 MHz	8-bit erase and program operations only
V_{DD} = 2.1 to 2.4 V	Conversion time up to 1.2 Msps	22 MHz	168 MHz with 7 wait states	– Degraded speed performance – No I/O compensation	up to 30 MHz	16-bit erase and program operations
V_{DD} = 2.4 to 2.7 V	Conversion time up to 2.4 Msps	24 MHz	168 MHz with 6 wait states	– Degraded speed performance – I/O compensation works	up to 48 MHz	16-bit erase and program operations
V_{DD} = 2.7 to 3.6 V(5)	Conversion time up to 2.4 Msps	30 MHz	168 MHz with 5 wait states	– Full-speed operation – I/O compensation works	– up to 60 MHz when V_{DD} = 3.0 to 3.6 V – up to 48 MHz when V_{DD} = 2.7 to 3.0 V	32-bit erase and program operations

1. It applies only when code executed from Flash memory access, when code executed from RAM, no wait state is required.
2. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
3. V_{DD}/VDDA minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to *Section : Internal reset OFF*).
4. Prefetch is not available. Refer to AN3430 application note for details on how to adjust performance and power.
5. The voltage range for OTG USB FS can drop down to 2.7 V. However it is degraded between 2.7 and 3 V.

Table 28. Peripheral current consumption (continued)

Peripheral		I_{DD}(Typ)(1)		Unit
		Scale1 (up t 168 MHz)	Scale2 (up to 144 MHz)	
APB2 (up to 84 MHz)	SDIO	7.08	7.92	µA/MHz
	TIM1	16.79	15.51	
	TIM8	17.88	16.53	
	TIM9	7.64	7.28	
	TIM10	4.89	4.82	
	TIM11	5.19	4.82	
	ADC1(5)	4.67	4.58	
	ADC2(5)	4.67	4.58	
	ADC3(5)	4.43	4.44	
	SPI1	1.32	1.39	
	USART1	3.51	3.72	
	USART6	3.55	3.75	
	SYSCFG	0.74	0.56	

1. When the I/O compensation cell is ON, I_{DD} typical value increases by 0.22 mA.
2. The BusMatrix is automatically active when at least one master is ON.
3. To enable an I2S peripheral, first set the I2SMOD bit and then the I2SE bit in the SPI_I2SCFGR register.
4. When the DAC is ON and EN1/2 bits are set in DAC_CR register, add an additional power consumption of 0.8 mA per DAC channel for the analog part.
5. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.

5.3.7 Wakeup time from low-power mode

The wakeup times given in *Table 29* is measured on a wakeup phase with a 16 MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 47. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}(1)	Injected current on BOOT0 pin	− 0	NA	mA
	Injected current on NRST pin	− 0	NA	
	Injected current on PE2, PE3, PE4, PE5, PE6, PI8, PC13, PC14, PC15, PI9, PI10, PI11, PF0, PF1, PF2, PF3, PF4, PF5, PF10, PH0/OSC_IN, PH1/OSC_OUT, PC0, PC1, PC2, PC3, PB6, PB7, PB8, PB9, PE0, PE1, PI4, PI5, PI6, PI7, PDR_ON, BYPASS_REG	− 0	NA	
	Injected current on all FT pins	− 5	NA	
	Injected current on any other pin	− 5	+5	

1. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

5.3.16 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under the conditions summarized in *Table 14*. All I/Os are CMOS and TTL compliant.

Table 48. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	FT, TTa and NRST I/O input low level voltage	1.7 V ≤V_{DD} ≤3.6 V	-	-	$0.3V_{DD}$-0.04(1)	V
			-	-	$0.3V_{DD}$(2)	
	BOOT0 I/O input low level voltage	1.75 V ≤V_{DD} ≤3.6 V -40 °C≤T_A ≤105 °C	-	-	$0.1V_{DD}$-+0.1(1)	
		1.7 V ≤V_{DD} ≤3.6 V 0 °C≤T_A ≤105 °C	-	-		
V_{IH}	FT, TTa and NRST I/O input low level voltage	1.7 V ≤V_{DD} ≤3.6 V	$0.45V_{DD}$+0.3(1)	-	-	
			$0.7V_{DD}$(2)	-	-	
	BOOT0 I/O input low level voltage	1.75 V ≤V_{DD} ≤3.6 V -40 °C≤T_A ≤105 °C	$0.17V_{DD}$+0.7(1)	-	-	
		1.7 V ≤V_{DD} ≤3.6 V 0 °C≤T_A ≤105 °C		-	-	

Figure 44. USB OTG FS timings: definition of data signal rise and fall time

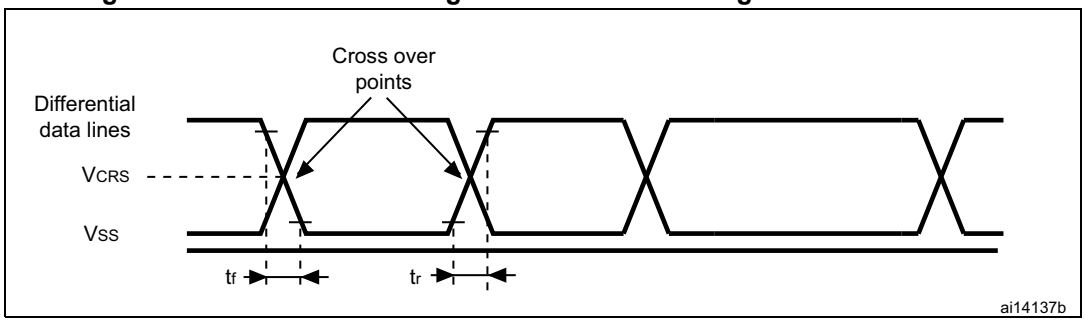


Table 59. USB OTG FS electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

USB HS characteristics

Unless otherwise specified, the parameters given in *Table 62* for ULPI are derived from tests performed under the ambient temperature, f_{HCLK} frequency summarized in *Table 61* and V_{DD} supply voltage conditions summarized in *Table 60*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to Section *Section 5.3.16: I/O port characteristics* for more details on the input/output characteristics.

Table 60. USB HS DC electrical characteristics

Symbol		**Parameter**	**Min.(1)**	**Max.(1)**	**Unit**
Input level	V_{DD}	USB OTG HS operating voltage	2.7	3.6	V

1. All the voltages are measured from the local ground potential.

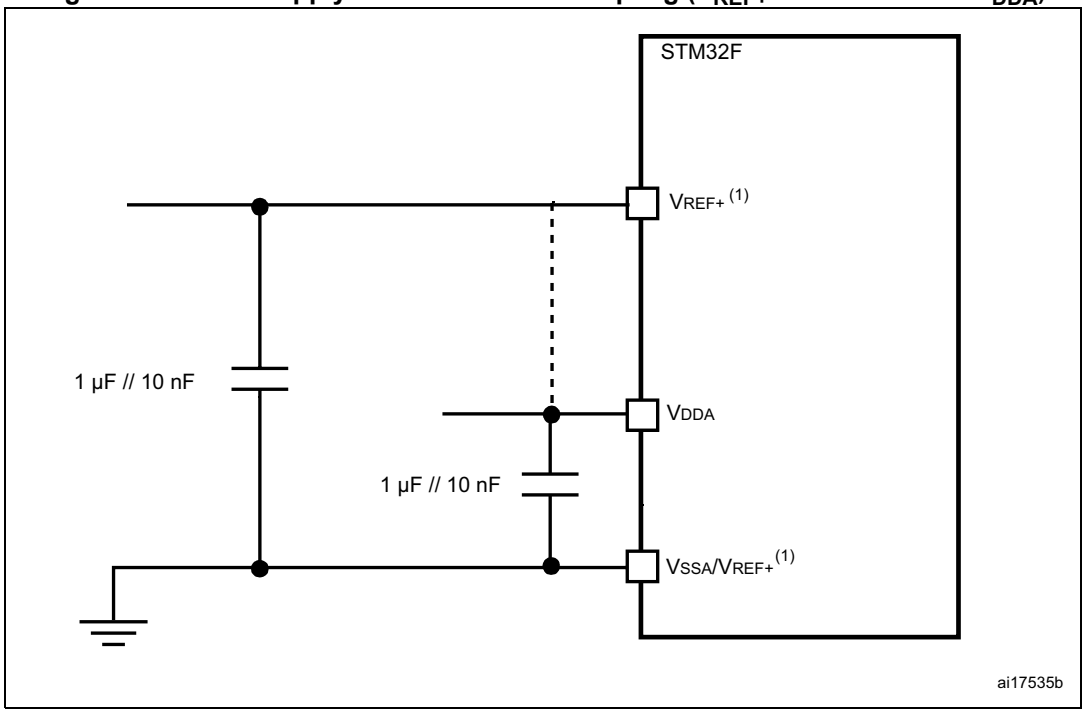
Table 61. USB HS clock timing parameters(1)

Parameter		**Symbol**	**Min**	**Nominal**	**Max**	**Unit**
f_{HCLK} value to guarantee proper operation of USB HS interface		-	30	-	-	MHz
Frequency (first transition)	8-bit ±10%	F_{START_8BIT}	54	60	66	MHz

General PCB design guidelines

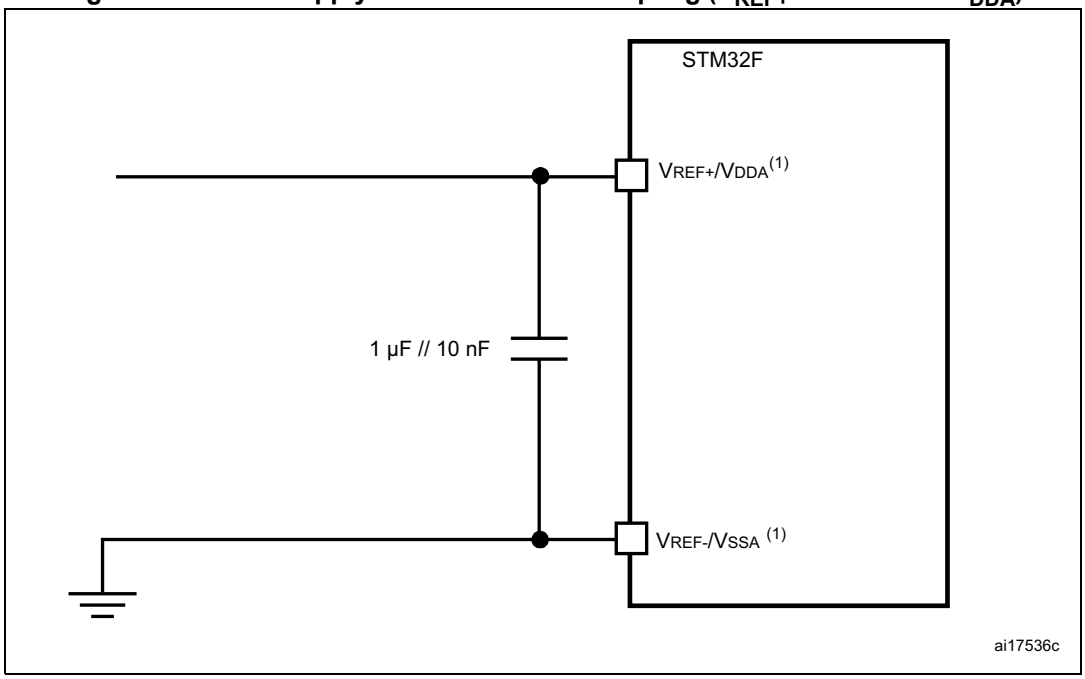
Power supply decoupling should be performed as shown in *Figure 51* or *Figure 52*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 51. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176. V_{REF+} is also available on LQFP100, LQFP144, and LQFP176. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

Figure 52. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176. V_{REF+} is also available on LQFP100, LQFP144, and LQFP176. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

5.3.22 Temperature sensor characteristics

Table 69. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	-	2.5		mV/°C
V_{25}(1)	Voltage at 25 °C	-	0.76		V
t_{START}(2)	Startup time	-	6	10	µs
T_{S_temp}(2)	ADC sampling time when reading the temperature (1 °C accuracy)	10	-	-	µs

1. Guaranteed by characterization.
2. Guaranteed by design.

Table 70. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}=3.3 V	0x1FFF 7A2C - 0x1FFF 7A2D
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C, V_{DDA}=3.3 V	0x1FFF 7A2E - 0x1FFF 7A2F

Figure 61. Synchronous non-multiplexed PSRAM write timings

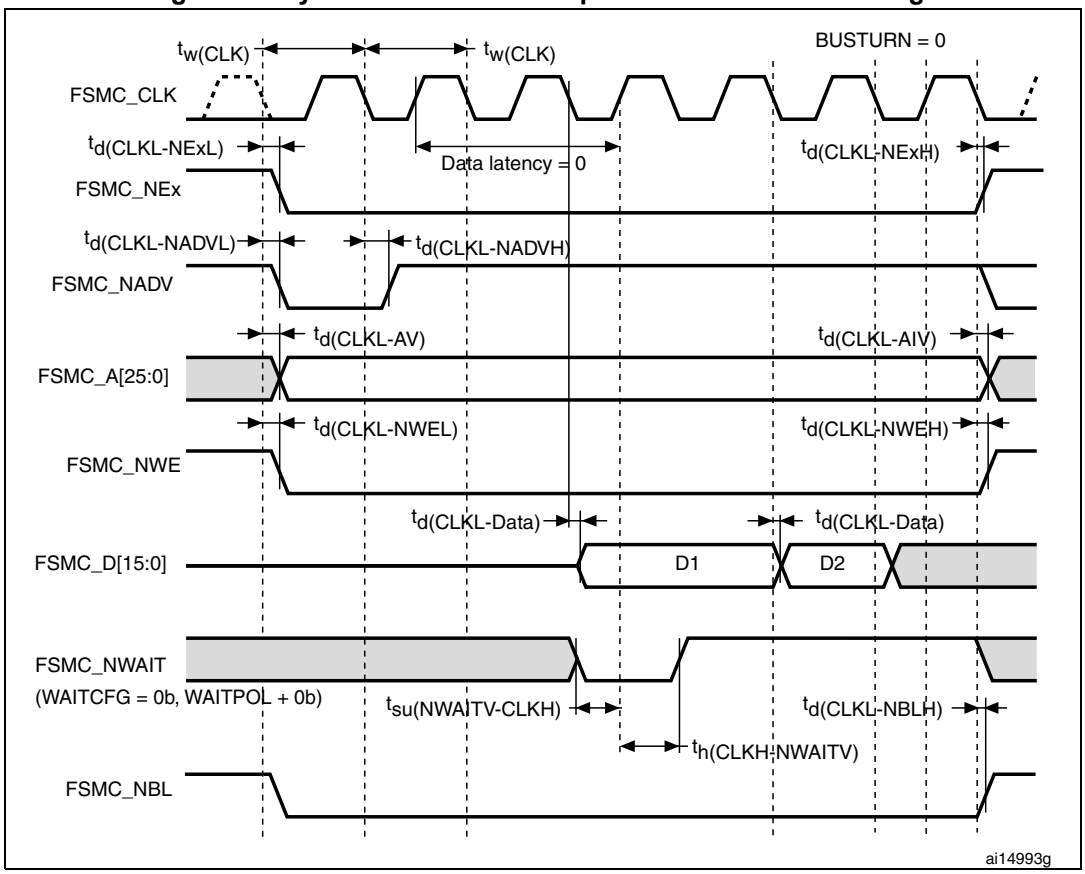


Table 82. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$	-	ns
$t^{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	1	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0…2)	1	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	7	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	6	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16…25)	6	-	ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	2	-	ns
$t_{d(CLKL-Data)}$	FSMC_D[15:0] valid data after FSMC_CLK low	-	3	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	3	-	ns
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	4	-	ns
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization.

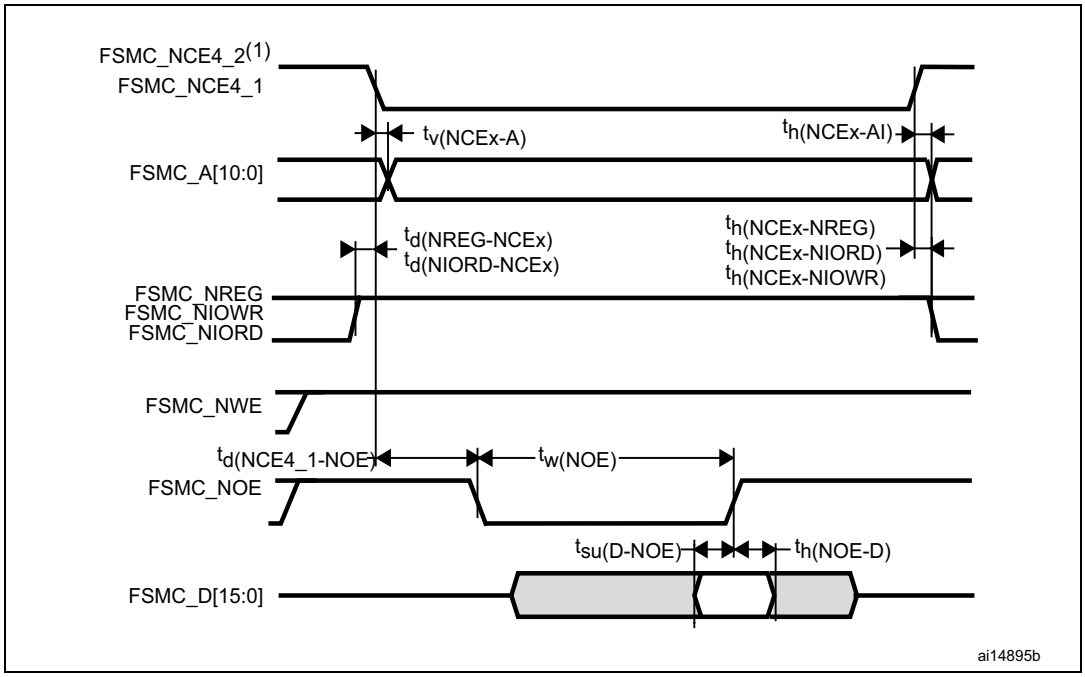
PC Card/CompactFlash controller waveforms and timings

Figure 62 through *Figure 67* represent synchronous waveforms, and *Table 83* and *Table 84* provide the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x04;
- COM.FSMC_WaitSetupTime = 0x07;
- COM.FSMC_HoldSetupTime = 0x04;
- COM.FSMC_HiZSetupTime = 0x00;
- ATT.FSMC_SetupTime = 0x04;
- ATT.FSMC_WaitSetupTime = 0x07;
- ATT.FSMC_HoldSetupTime = 0x04;
- ATT.FSMC_HiZSetupTime = 0x00;
- IO.FSMC_SetupTime = 0x04;
- IO.FSMC_WaitSetupTime = 0x07;
- IO.FSMC_HoldSetupTime = 0x04;
- IO.FSMC_HiZSetupTime = 0x00;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 62. PC Card/CompactFlash controller waveforms for common memory read access



1. FSMC_NCE4_2 remains high (inactive during 8-bit access.

Figure 70. NAND controller waveforms for common memory read access

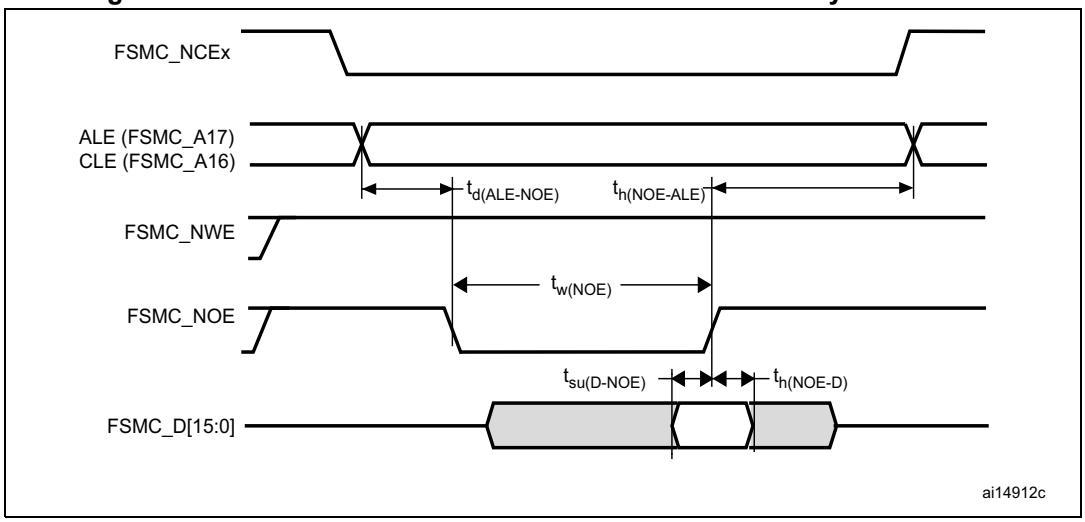


Figure 71. NAND controller waveforms for common memory write access

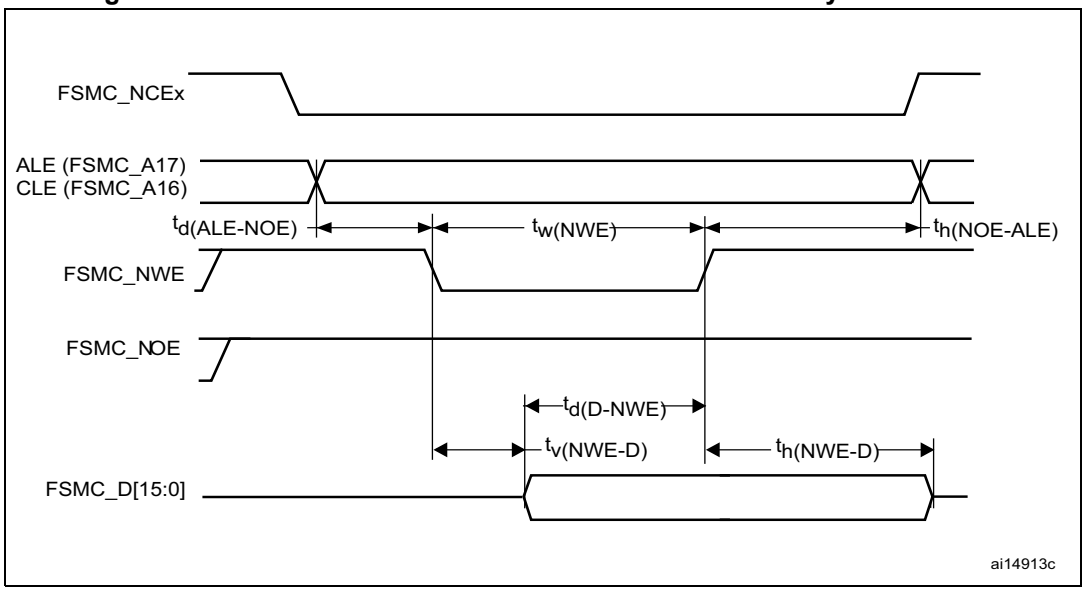


Table 85. Switching characteristics for NAND Flash read cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(N0E)}$	FSMC_NOE low width	$4T_{HCLK}-0.5$	$4T_{HCLK}+3$	ns
$t_{su(D-NOE)}$	FSMC_D[15-0] valid data before FSMC_NOE high	10	-	ns
$t_{h(NOE-D)}$	FSMC_D[15-0] valid data after FSMC_NOE high	0	-	ns
$t_{d(ALE-NOE)}$	FSMC_ALE valid before FSMC_NOE low	-	$3T_{HCLK}$	ns
$t_{h(NOE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$3T_{HCLK}-2$	-	ns

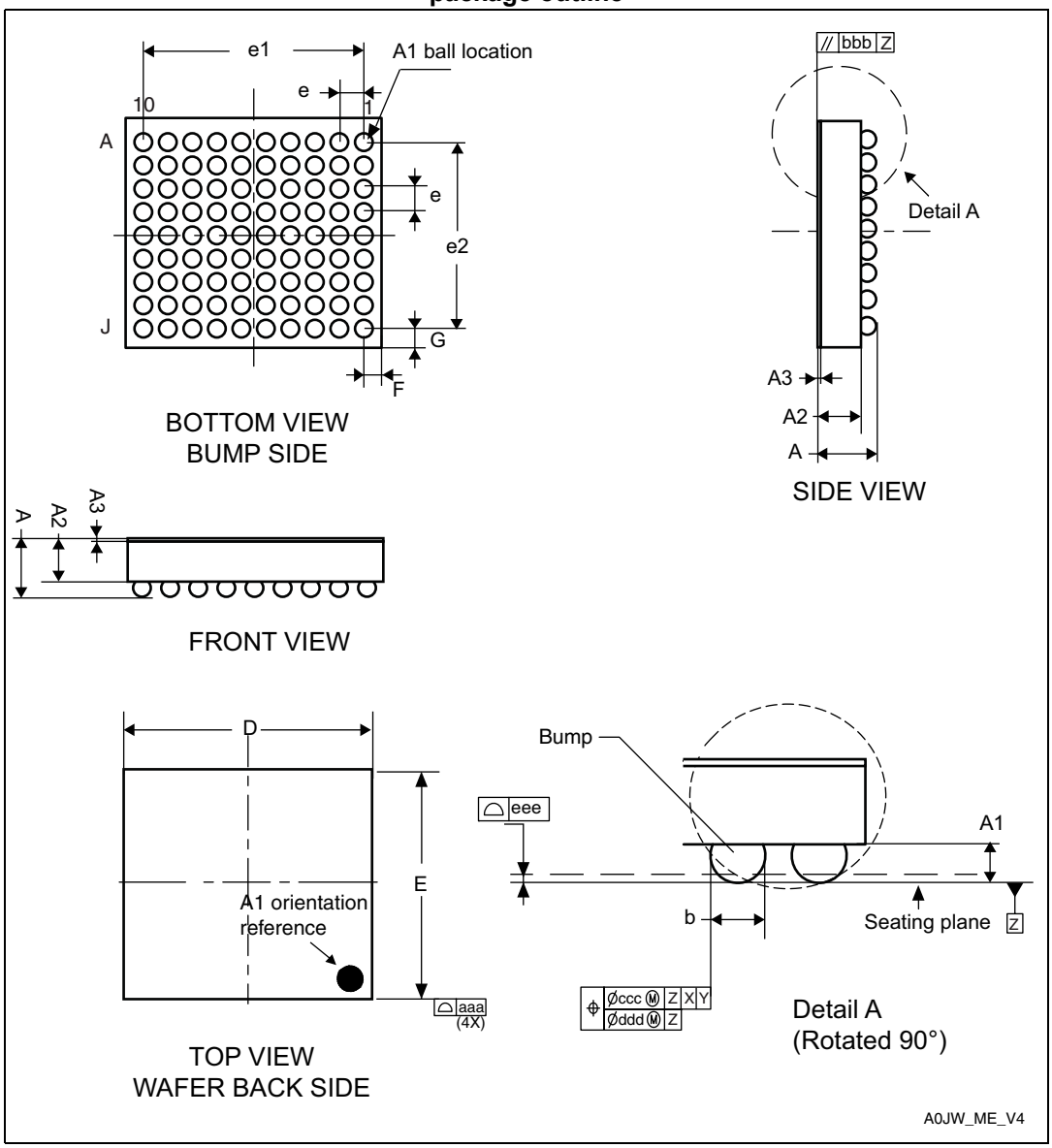
1. C_L = 30 pF.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

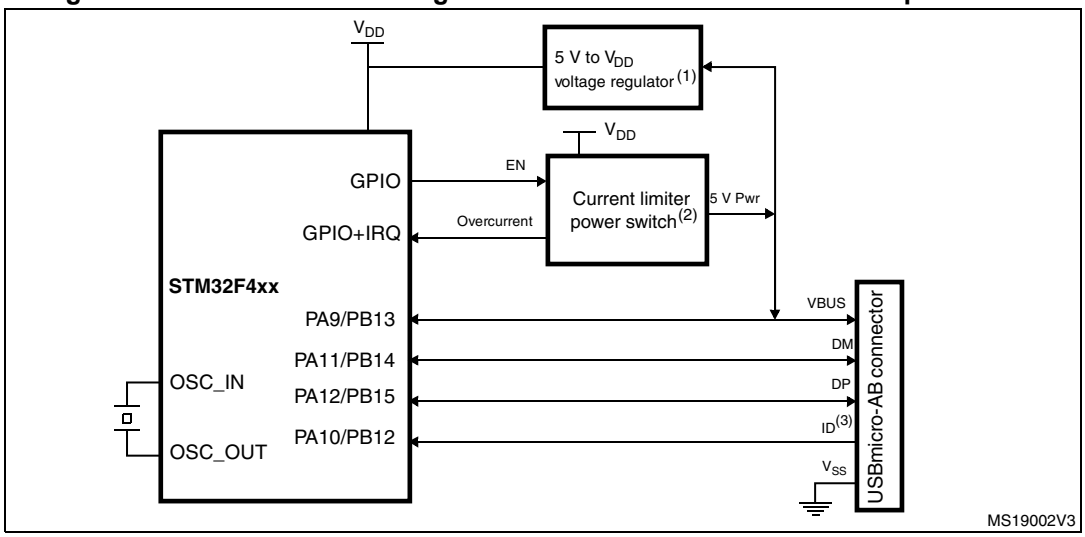
6.1 WLCSP90 package information

Figure 75. WLCSP90 - 4.223 x 3.969 mm, 0.400 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

Figure 95. USB controller configured in dual mode and used in full speed mode



1. External voltage regulator only needed when building a V_{BUS} powered device.
2. The current limiter is required only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.
3. The ID pin is required in dual role only.
4. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

8 Revision history

Table 100. Document revision history

Date	Revision	Changes
15-Sep-2011	1	Initial release.
24-Jan-2012	2	Added WLCSP90 package on cover page. Renamed USART4 and USART5 into UART4 and UART5, respectively. Updated number of USB OTG HS and FS in *Table 2: STM32F415xx and STM32F417xx: features and peripheral counts*. Updated *Figure 3: Compatible board design between STM32F10xx/STM32F2/STM32F41xxx for LQFP144 package* and *Figure 4: Compatible board design between STM32F2 and STM32F41xxx for LQFP176 and BGA176 packages*, and removed note 1 and 2. Updated *Section 2.2.9: Flexible static memory controller (FSMC)*. Modified I/Os used to reprogram the Flash memory for CAN2 and USB OTG FS in *Section 2.2.13: Boot modes*. Updated note in *Section 2.2.14: Power supply schemes*. PDR_ON no more available on LQFP100 package. Updated *Section 2.2.16: Voltage regulator*. Updated condition to obtain a minimum supply voltage of 1.7 V in the whole document. Renamed USART4/5 to UART4/5 and added LIN and IrDA feature for UART4 and UART5 in *Table 5: USART feature comparison*. Removed support of I2C for OTG PHY in *Section 2.2.30: Universal serial bus on-the-go full-speed (OTG_FS)*. Added *Table 6: Legend/abbreviations used in the pinout table*. *Table 7: STM32F41xxx pin and ball definitions*: replaced V_{SS}_3, V_{SS}_4, and V_{SS}_8 by V_{SS}; reformatted *Table 7: STM32F41xxx pin and ball definitions* to better highlight I/O structure, and alternate functions versus additional functions; signal corresponding to LQFP100 pin 99 changed from PDR_ON to V_{SS}; EVENTOUT added in the list of alternate functions for all I/Os; ADC3_IN8 added as alternate function for PF10; FSMC_CLE and FSMC_ALE added as alternate functions for PD11 and PD12, respectively; PH10 alternate function TIM15_CH1_ETR renamed TIM5_CH1; updated PA4 and PA5 I/O structure to TTa. Removed OTG_HS_SCL, OTG_HS_SDA, OTG_FS_INTN in *Table 7: STM32F41xxx pin and ball definitions* and *Table 9: Alternate function mapping*. Changed TCM data RAM to CCM data RAM in *Figure 18: STM32F41xxx memory map*. Added I_{VDD} and I_{VSS} maximum values in *Table 12: Current characteristics*. Added *Note 1* related to f_{HCLK}, updated *Note 2* in *Table 14: General operating conditions*, and added maximum power dissipation values. Updated *Table 15: Limitations depending on the operating power supply range*.

Table 100. Document revision history (continued)

Date	Revision	Changes
04-Jun-2013	4 (continued)	Updated *Figure 6: Multi-AHB matrix*. Updated *Figure 7: Power supply supervisor interconnection with internal reset OFF* Changed 1.2 V to V_{12} in *Section : Regulator OFF* Updated LQFP176 pin 48. Updated *Section 1: Introduction*. Updated *Section 2: Description*. Updated operating voltage in *Table 2: STM32F415xx and STM32F417xx: features and peripheral counts*. Updated *Note 1*. Updated *Section 2.2.15: Power supply supervisor*. Updated *Section 2.2.16: Voltage regulator*. Updated *Figure 9: Regulator OFF*. Updated *Table 3: Regulator ON/OFF and internal reset ON/OFF availability*. Updated *Section 2.2.19: Low-power modes*. Updated *Section 2.2.20: VBAT operation*. Updated *Section 2.2.22: Inter-integrated circuit interface (I²C)* . Updated pin 48 in *Figure 15: STM32F41xxx LQFP176 pinout*. Updated *Table 6: Legend/abbreviations used in the pinout table*. Updated *Table 7: STM32F41xxx pin and ball definitions*. Updated *Table 14: General operating conditions*. Updated *Table 15: Limitations depending on the operating power supply range*. Updated *Section 5.3.7: Wakeup time from low-power mode*. Updated *Table 34: HSI oscillator characteristics*. Updated *Section 5.3.15: I/O current injection characteristics*. Updated *Table 48: I/O static characteristics*. Updated *Table 51: NRST pin characteristics*. Updated *Table 56: I^2C characteristics*. Updated *Figure 39: I^2C bus AC waveforms and measurement circuit*. Updated *Section 5.3.19: Communications interfaces*. Updated *Table 67: ADC characteristics*. Added *Table 70: Temperature sensor calibration values*. Added *Table 73: Internal reference voltage calibration values*. Updated *Section 5.3.26: FSMC characteristics*. Updated *Section 5.3.28: SD/SDIO MMC card host interface (SDIO) characteristics*. Updated *Table 23: Typical and maximum current consumptions in Stop mode*. Updated *Section : SPI interface characteristics* included *Table 55*. Updated *Section : I2S interface characteristics* included *Table 56*. Updated *Table 64: Dynamic characteristics: Eternity MAC signals for SMI*. Updated *Table 66: Dynamic characteristics: Ethernet MAC signals for MII*.