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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	CANbus, DCMI, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	140
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f417igt7

2 Description

The STM32F415xx and STM32F417xx family is based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 168 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F415xx and STM32F417xx family incorporates high-speed embedded memories (Flash memory up to 1 Mbyte, up to 192 Kbytes of SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, three AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers, a true random number generator (RNG), and a cryptographic acceleration cell. They also feature standard and advanced communication interfaces.

- Up to three I²Cs
- Three SPIs, two I²Ss full duplex. To achieve audio class accuracy, the I2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus two UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI),
- Two CANs
- An SDIO/MMC interface
- Ethernet and the camera interface available on STM32F417xx devices only.

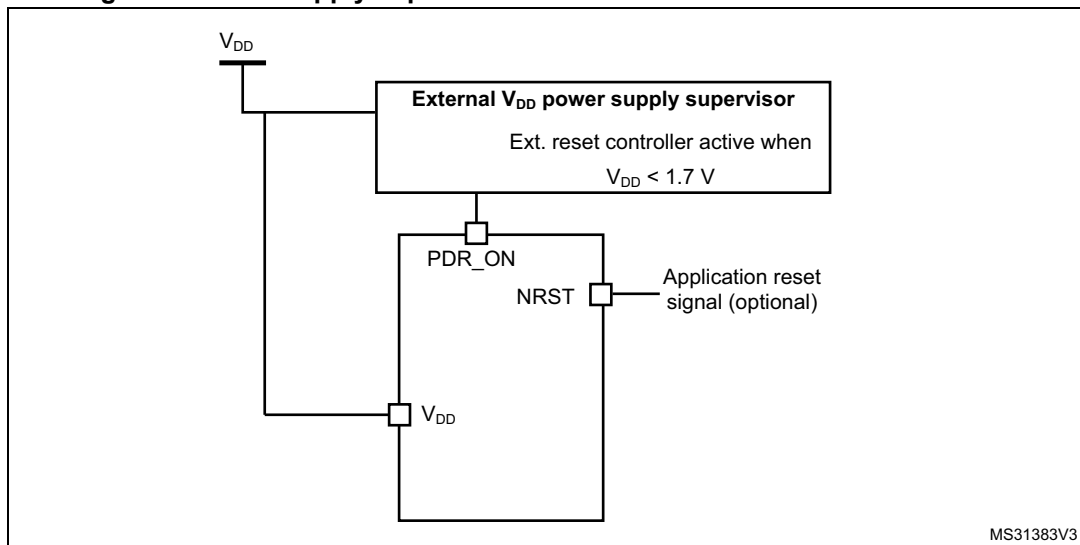
New advanced peripherals include an SDIO, an enhanced flexible static memory control (FSMC) interface (for devices offered in packages of 100 pins and more), a camera interface for CMOS sensors and a cryptographic acceleration cell. Refer to [Table 2: STM32F415xx and STM32F417xx: features and peripheral counts](#) for the list of peripherals available on each part number.

The STM32F415xx and STM32F417xx family operates in the –40 to +105 °C temperature range from a 1.8 to 3.6 V power supply. The supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor: refer to [Section : Internal reset OFF](#). A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F415xx and STM32F417xx family offers devices in various packages ranging from 64 pins to 176 pins. The set of included peripherals changes with the device chosen.

These features make the STM32F415xx and STM32F417xx microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances

Figure 7. Power supply supervisor interconnection with internal reset OFF

1. PDR = 1.7 V for reduce temperature range; PDR = 1.8 V for all temperature range.

The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.8 V (see [Figure 7](#)). This supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range.

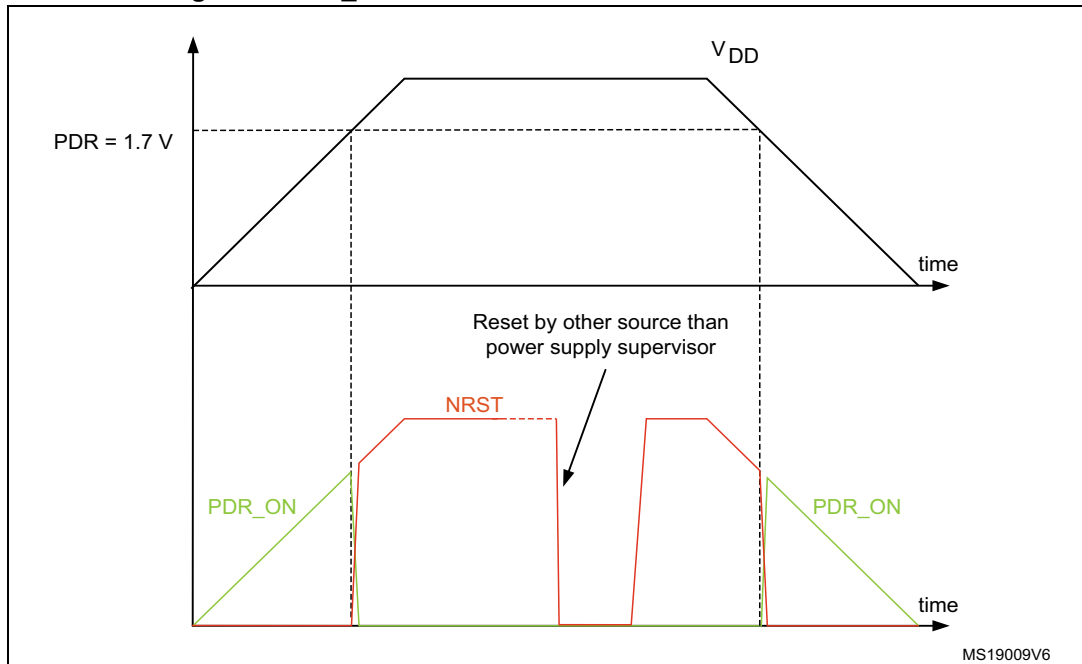
A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry is disabled
- The embedded programmable voltage detector (PVD) is disabled
- V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}

All packages, except for the LQFP64 and LQFP100, allow to disable the internal reset through the PDR_ON signal.

Figure 8. PDR_ON and NRST control with internal reset OFF



1. PDR = 1.7 V for reduce temperature range; PDR = 1.8 V for all temperature range.

2.2.16 Voltage regulator

The regulator has four operating modes:

- Regulator ON
 - Main regulator mode (MR)
 - Low-power regulator (LPR)
 - Power-down
- Regulator OFF

Regulator ON

On packages embedding the BYPASS_REG pin, the regulator is enabled by holding BYPASS_REG low. On all other packages, the regulator is always enabled.

There are three power modes configured by software when regulator is ON:

- MR is used in the nominal regulation mode (With different voltage scaling in Run)
In Main regulator mode (MR mode), different voltage scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption. Refer to [Table 14: General operating conditions](#).
- LPR is used in the Stop modes
The LP regulator mode is configured by software when entering Stop mode.
- Power-down is used in Standby mode.
The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost)

2.2.26 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I²S application. It allows to achieve error-free I²S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I²S sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I²S flow with an external PLL (or Codec output).

2.2.27 Secure digital input/output interface (SDIO)

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 48 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

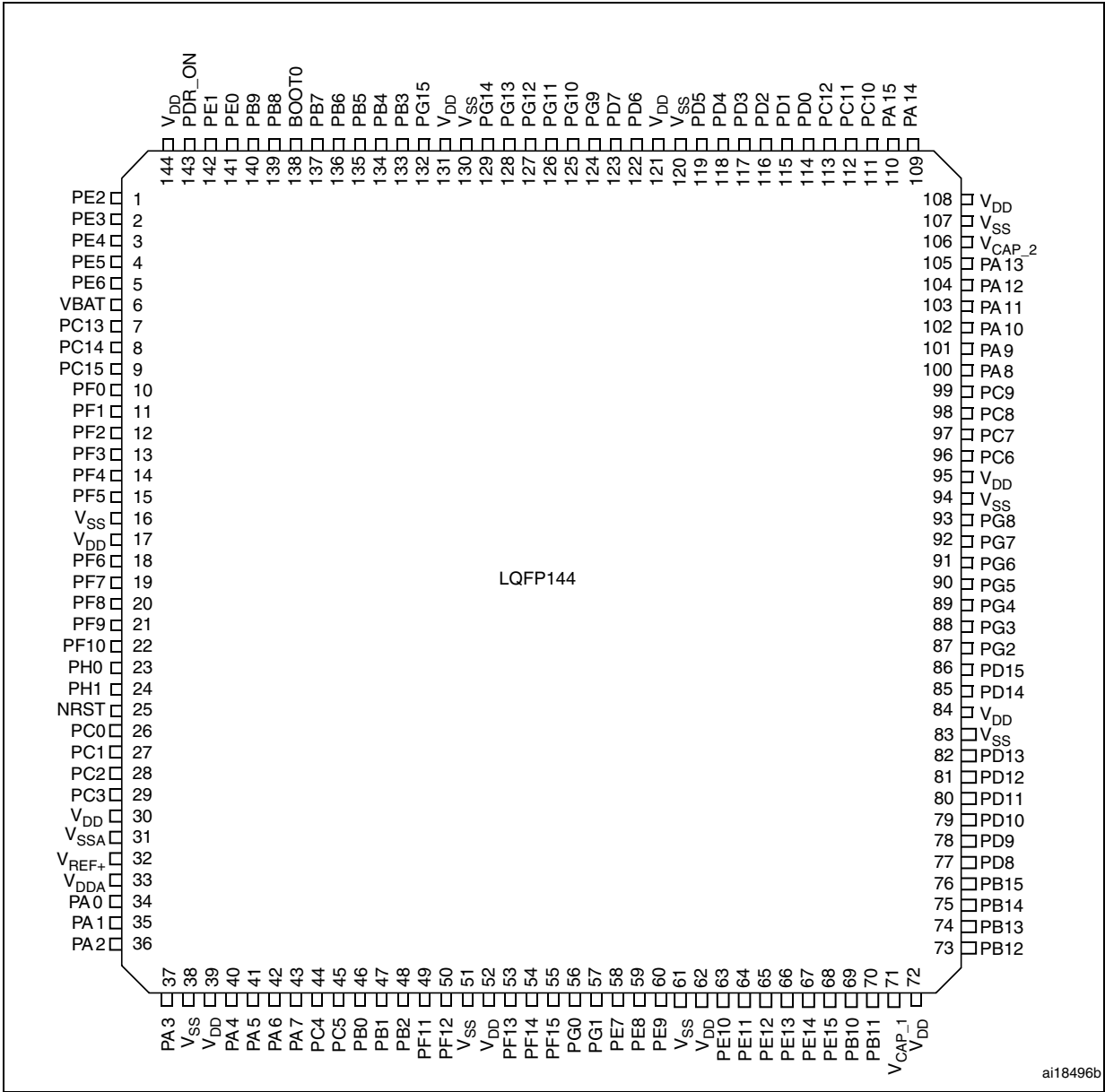
In addition to SD/SDIO/MMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

2.2.28 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

Peripheral available only on the STM32F417xx devices.

The STM32F417xx devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The STM32F417xx requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). the PHY is connected to the STM32F417xx MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the STM32F417xx.

Figure 14. STM32F41xxx LQFP144 pinout



1. The above figure shows the package top view.

Table 7. STM32F41xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset) ⁽¹⁾	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
40	E3	66	99	F14	118	PC9	I/O	FT	-	I2S_CKIN/ MCO2 / TIM8_CH4/SDIO_D1 / I2C3_SDA / DCMI_D3 / TIM3_CH4/ EVENTOUT	-
41	D1	67	100	F15	119	PA8	I/O	FT	-	MCO1 / USART1_CK/ TIM1_CH1/ I2C3_SCL/ OTG_FS_SOF/ EVENTOUT	-
42	D2	68	101	E15	120	PA9	I/O	FT	-	USART1_TX/ TIM1_CH2 / I2C3_SMBA / DCMI_D0/ EVENTOUT	OTG_FS_VBUS
43	D3	69	102	D15	121	PA10	I/O	FT	-	USART1_RX/ TIM1_CH3/ OTG_FS_ID/DCMI_D1/ EVENTOUT	-
44	C1	70	103	C15	122	PA11	I/O	FT	-	USART1_CTS / CAN1_RX / TIM1_CH4 / OTG_FS_DM/ EVENTOUT	-
45	C2	71	104	B15	123	PA12	I/O	FT	-	USART1_RTS / CAN1_TX/ TIM1_ETR/ OTG_FS_DP/ EVENTOUT	-
46	D4	72	105	A15	124	PA13 (JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO/ EVENTOUT	-
47	B1	73	106	F13	125	V _{CAP_2}	S	-	-	-	-
-	E7	74	107	F12	126	V _{SS}	S	-	-	-	-
48	E6	75	108	G13	127	V _{DD}	S	-	-	-	-
-	-	-	-	E12	128	PH13	I/O	FT	-	TIM8_CH1N / CAN1_TX/ EVENTOUT	-
-	-	-	-	E13	129	PH14	I/O	FT	-	TIM8_CH2N / DCMI_D4/ EVENTOUT	-
-	-	-	-	D13	130	PH15	I/O	FT	-	TIM8_CH3N / DCMI_D11/ EVENTOUT	-
-	C3	-	-	E14	131	PI0	I/O	FT	-	TIM5_CH4 / SPI2_NSS / I2S2_WS / DCMI_D13/ EVENTOUT	-
-	B2	-	-	D14	132	PI1	I/O	FT	-	SPI2_SCK / I2S2_CK / DCMI_D8/ EVENTOUT	-

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/I2S2/I2S2ext	SPI3/I2Sext/I2S3	USART1/2/3/I2S3ext	UART4/5/USART6	CAN1/2/TIM12/13/14	OTG_FS/OTG_HS	ETH	FSMC/SDIO/OTG_FS	DCMI		
PortH	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH2	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_CRS	-	-	-	EVENTOUT
	PH3	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_COL	-	-	-	EVENTOUT
	PH4	-	-	-	-	I2C2_SCL	-	-	-	-	-	OTG_HS_ULPI_NXT	-	-	-	-	EVENTOUT
	PH5	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH6	-	-	-	-	I2C2_SMBA	-	-	-	-	TIM12_CH1	-	ETH_MII_RXD2	-	-	-	EVENTOUT
	PH7	-	-	-	-	I2C3_SCL	-	-	-	-	-	-	ETH_MII_RXD3	-	-	-	EVENTOUT
	PH8	-	-	-	-	I2C3_SDA	-	-	-	-	-	-	-	-	DCMI_HSYNC	-	EVENTOUT
	PH9	-	-	-	-	I2C3_SMBA	-	-	-	-	TIM12_CH2	-	-	-	DCMI_D0	-	EVENTOUT
	PH10	-	-	TIM5_CH1	-	-	-	-	-	-	-	-	-	-	DCMI_D1	-	EVENTOUT
	PH11	-	-	TIM5_CH2	-	-	-	-	-	-	-	-	-	-	DCMI_D2	-	EVENTOUT
	PH12	-	-	TIM5_CH3	-	-	-	-	-	-	-	-	-	-	DCMI_D3	-	EVENTOUT
	PH13	-	-	-	TIM8_CH1N	-	-	-	-	-	CAN1_TX	-	-	-	-	-	EVENTOUT
	PH14	-	-	-	TIM8_CH2N	-	-	-	-	-	-	-	-	-	DCMI_D4	-	EVENTOUT
	PH15	-	-	-	TIM8_CH3N	-	-	-	-	-	-	-	-	-	DCMI_D11	-	EVENTOUT

Table 12. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power lines (source) ⁽¹⁾	240	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink) ⁽¹⁾	240	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	25	
$I_{INJ(PIN)}^{(2)}$	Injected current on five-volt tolerant I/O ⁽³⁾	-5/+0	
	Injected current on any other pin ⁽⁴⁾	±5	
$\Sigma I_{INJ(PIN)}^{(4)}$	Total injected current (sum of all I/O and control pins) ⁽⁵⁾	±25	

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note in [Section 5.3.21: 12-bit ADC characteristics](#).
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to [Table 11](#) for the values of the maximum allowed input voltage.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to [Table 11](#) for the values of the maximum allowed input voltage.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 13. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	125	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 14. General operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency	VOS bit in PWR_CR register = 0 ⁽¹⁾	0	-	144	MHz
		VOS bit in PWR_CR register = 1	0	-	168	
f_{PCLK1}	Internal APB1 clock frequency	-	0	-	42	
f_{PCLK2}	Internal APB2 clock frequency	-	0	-	84	
V_{DD}	Standard operating voltage	-	1.8 ⁽²⁾	-	3.6	V
$V_{DDA}^{(3)(4)}$	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as $V_{DD}^{(5)}$	1.8 ⁽²⁾	-	2.4	V
	Analog operating voltage (ADC limited to 1.4 M samples)		2.4	-	3.6	
V_{BAT}	Backup operating voltage	-	1.65	-	3.6	V

Low-speed external user clock generated from an external source

The characteristics given in [Table 31](#) result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 14](#).

Table 31. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency ⁽¹⁾	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{f(LSE)}$	OSC32_IN high or low time ⁽¹⁾		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time ⁽¹⁾		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance ⁽¹⁾	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 1	μA

1. Guaranteed by design.

Figure 30. High-speed external clock source AC timing diagram

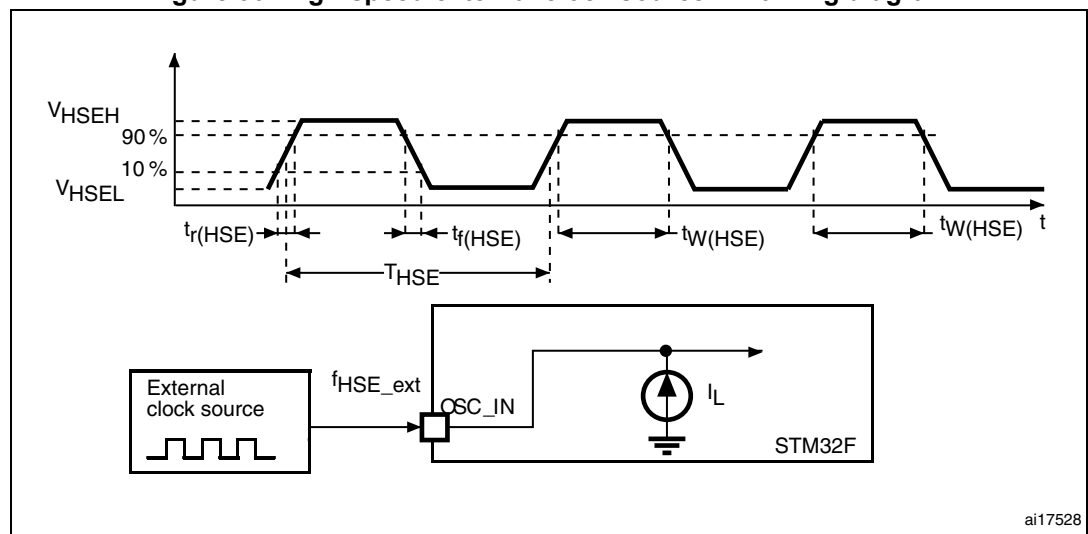
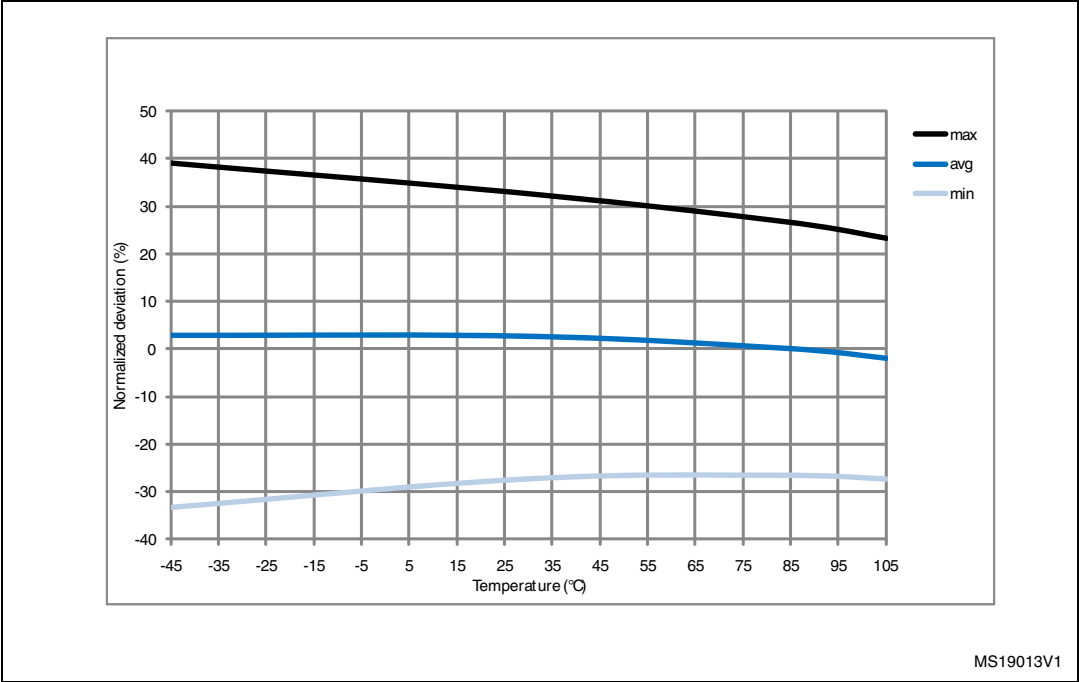


Figure 34. ACC_{LSI} versus temperature



5.3.10 PLL characteristics

The parameters given in [Table 36](#) and [Table 37](#) are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in [Table 14](#).

Table 36. Main PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{PLL_IN}	PLL input clock ⁽¹⁾	-	0.95 ⁽²⁾	1	2.10	MHz
f _{PLL_OUT}	PLL multiplier output clock	-	24	-	168	MHz
f _{PLL48_OUT}	48 MHz PLL multiplier output clock	-	-	48	75	MHz
f _{VCO_OUT}	PLL VCO output	-	100	-	432	MHz
t _{LOCK}	PLL lock time	VCO freq = 100 MHz	75	-	200	μs
		VCO freq = 432 MHz	100	-	300	

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ± 3 mA. When using the PC13 to PC15 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 5.2](#). In particular:

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum Run consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating I_{VDD} (see [Table 12](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see [Table 12](#)).

Output voltage levels

Unless otherwise specified, the parameters given in [Table 49](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 14](#). All I/Os are CMOS and TTL compliant.

Table 49. Output voltage characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(2)}$	Output low level voltage	CMOS port $I_{IO} = +8$ mA $2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage		$V_{DD}-0.4$	-	
$V_{OL}^{(2)}$	Output low level voltage	TTL port $I_{IO} = +8$ mA $2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage		2.4	-	
$V_{OL}^{(2)(4)}$	Output low level voltage	$I_{IO} = +20$ mA $2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-	1.3	V
$V_{OH}^{(3)(4)}$	Output high level voltage		$V_{DD}-1.3$	-	
$V_{OL}^{(2)(4)}$	Output low level voltage	$I_{IO} = +6$ mA $2\text{ V} < V_{DD} < 2.7\text{ V}$	-	0.4	V
$V_{OH}^{(3)(4)}$	Output high level voltage		$V_{DD}-0.4$	-	

1. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
2. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 12](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 12](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .
4. Guaranteed by characterization.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 37](#) and [Table 50](#), respectively.

Unless otherwise specified, the parameters given in [Table 50](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 14](#).

Table 50. I/O AC characteristics⁽¹⁾⁽²⁾

OSPEEDRy [1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	4	MHz
			$C_L = 50 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	2	
			$C_L = 10 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	8	
			$C_L = 10 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	4	
	$t_{f(\text{IO})\text{out}}/$ $t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 50 \text{ pF}, V_{DD} = 1.8 \text{ V to}$ 3.6 V	-	-	100	ns
01	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	25	MHz
			$C_L = 50 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	12.5	
			$C_L = 10 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	50 ⁽⁴⁾	
			$C_L = 10 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	20	
	$t_{f(\text{IO})\text{out}}/$ $t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 50 \text{ pF}, V_{DD} > 2.7 \text{ V}$	-	-	10	ns
			$C_L = 50 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	20	
			$C_L = 10 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	6	
			$C_L = 10 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	10	
10	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 40 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	50 ⁽⁴⁾	MHz
			$C_L = 40 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	25	
			$C_L = 10 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	100 ⁽⁴⁾	
			$C_L = 10 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	50 ⁽⁴⁾	
	$t_{f(\text{IO})\text{out}}/$ $t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 40 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	6	ns
			$C_L = 40 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	10	
			$C_L = 10 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	4	
			$C_L = 10 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	6	

5.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see [Table 48](#)).

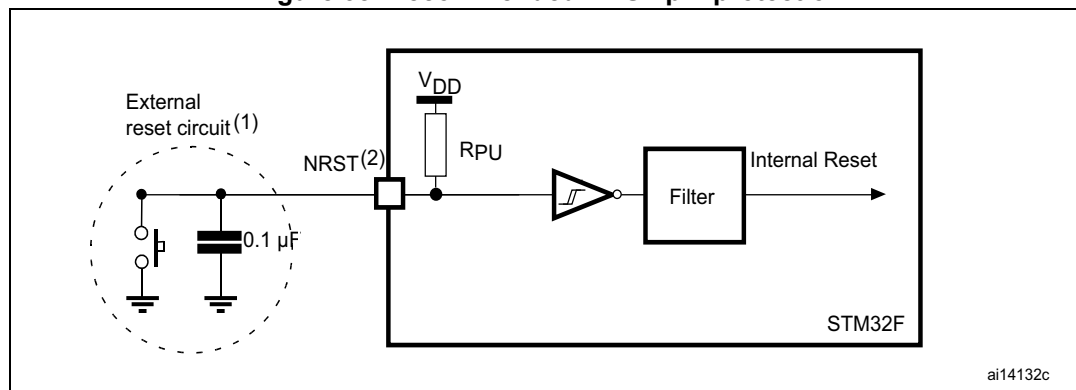
Unless otherwise specified, the parameters given in [Table 51](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 14](#).

Table 51. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}^{(1)}$	NRST Input low level voltage	TTL ports $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-	-	0.8	V
$V_{IH(NRST)}^{(1)}$	NRST Input high level voltage		2	-	-	
$V_{IL(NRST)}^{(1)}$	NRST Input low level voltage	CMOS ports $1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-	-	$0.3V_{DD}$	
$V_{IH(NRST)}^{(1)}$	NRST Input high level voltage		$0.7V_{DD}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor ⁽²⁾	$V_{IN} = V_{SS}$	30	40	50	k Ω
$V_{F(NRST)}^{(1)}$	NRST Input filtered pulse		-	-	100	ns
$V_{NF(NRST)}^{(1)}$	NRST Input not filtered pulse	$V_{DD} > 2.7\text{ V}$	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	μs

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 38. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 51](#). Otherwise the reset is not taken into account by the device.

5.3.18 TIM timer characteristics

The parameters given in [Table 52](#) and [Table 53](#) are guaranteed by design.

Refer to [Section 5.3.16: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 52. Characteristics of TIMx connected to the APB1 domain⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APB1 prescaler distinct from 1, $f_{TIMxCLK} = 84\text{ MHz}$	1	-	$t_{TIMxCLK}$
			11.9	-	ns
		AHB/APB1 prescaler = 1, $f_{TIMxCLK} = 42\text{ MHz}$	1	-	$t_{TIMxCLK}$
			23.8	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK} = 84\text{ MHz}$ APB1= 42 MHz	0	$f_{TIMxCLK}/2$	MHz
	0		42	MHz	
Res_{TIM}	Timer resolution		-	16/32	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected		1	65536	$t_{TIMxCLK}$
	32-bit counter clock period when internal clock is selected		0.0119	780	μs
			1	-	$t_{TIMxCLK}$
			0.0119	51130563	μs
			-	65536×65536	$t_{TIMxCLK}$
t_{MAX_COUNT}	Maximum possible count		-	51.1	s

1. TIMx is used as a general term to refer to the TIM2, TIM3, TIM4, TIM5, TIM6, TIM7, and TIM12 timers.

2. Guaranteed by characterization.

Synchronous waveforms and timings

Figure 58 through Figure 61 represent synchronous waveforms and Table 80 through Table 82 provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F40xxx/41xxx reference manual)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the T_{HCLK} is the HCLK clock period (with maximum FSMC_CLK = 60 MHz).

Figure 58. Synchronous multiplexed NOR/PSRAM read timings

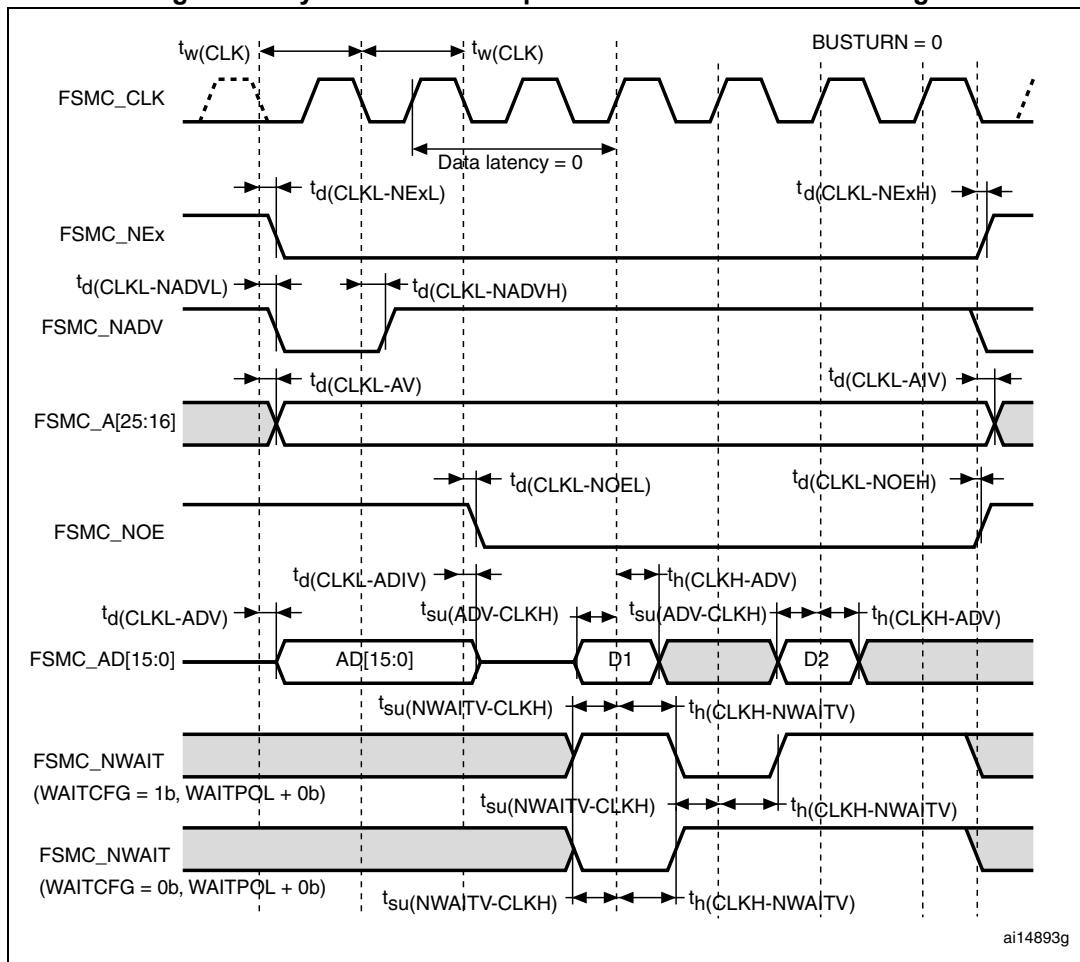


Figure 63. PC Card/CompactFlash controller waveforms for common memory write access

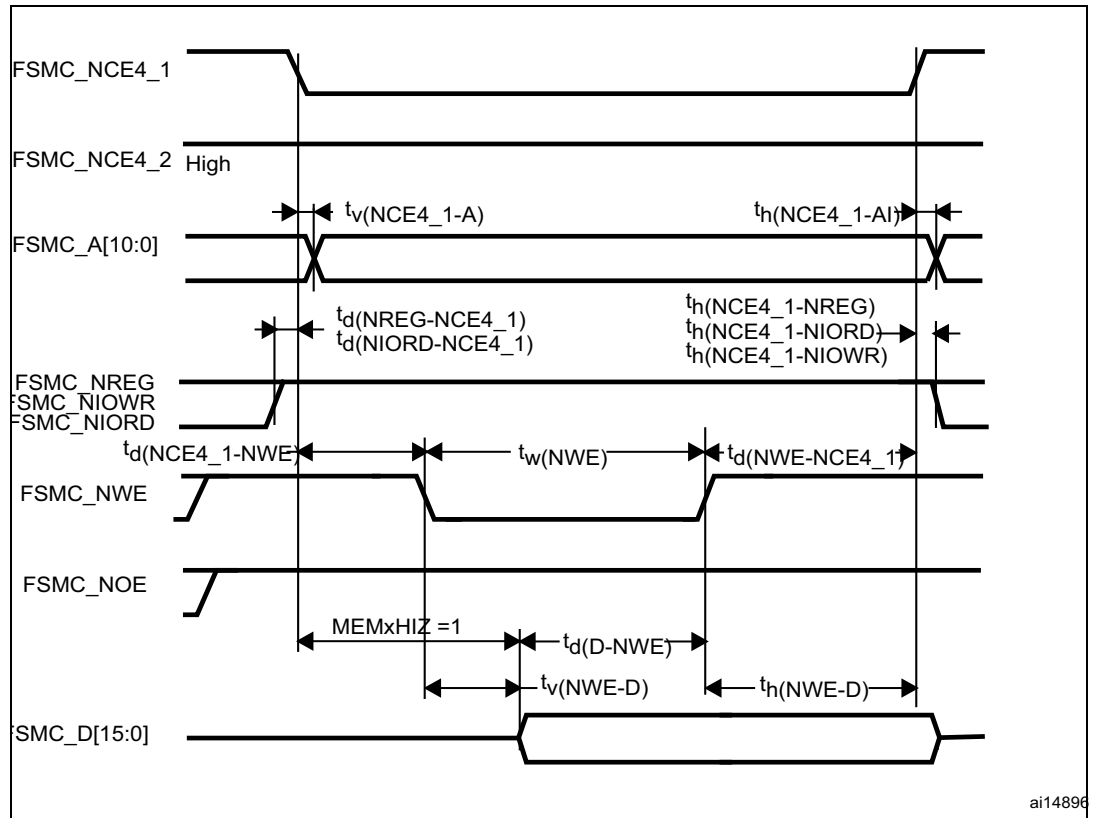


Table 86. Switching characteristics for NAND Flash write cycles⁽¹⁾

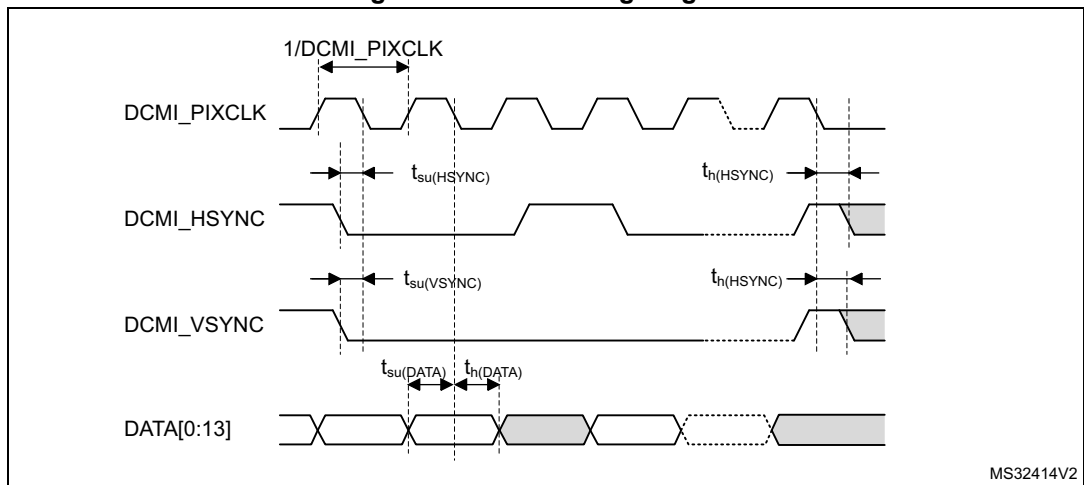
Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FSMC_NWE low width	$4T_{HCLK}-1$	$4T_{HCLK}+3$	ns
$t_{v(NWE-D)}$	FSMC_NWE low to FSMC_D[15-0] valid	-	0	ns
$t_{h(NWE-D)}$	FSMC_NWE high to FSMC_D[15-0] invalid	$3T_{HCLK}-2$	-	ns
$t_{d(D-NWE)}$	FSMC_D[15-0] valid before FSMC_NWE high	$5T_{HCLK}-3$	-	ns
$t_{d(ALE-NWE)}$	FSMC_ALE valid before FSMC_NWE low	-	$3T_{HCLK}$	ns
$t_{h(NWE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$3T_{HCLK}-2$	-	ns

1. $C_L = 30$ pF.

5.3.27 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in [Table 87](#) for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in [Table 13](#), with the following configuration:

- PCK polarity: falling
- VSYNC and HSYNC polarity: high
- Data format: 14 bits

Figure 72. DCMI timing diagram**Table 87. DCMI characteristics⁽¹⁾**

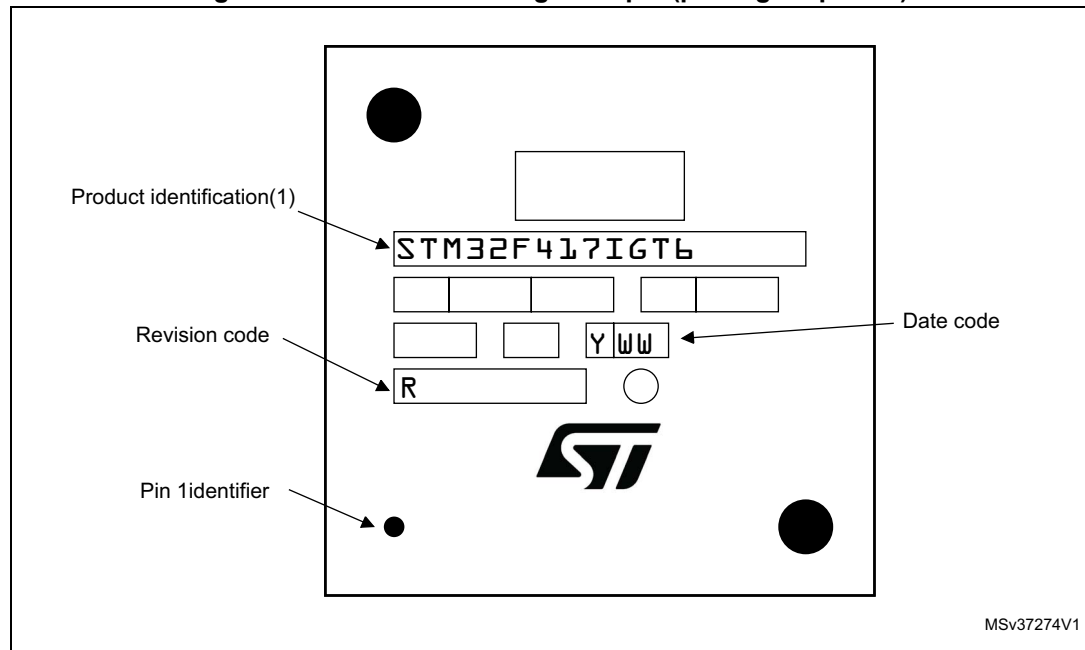
Symbol	Parameter	Min	Max	Unit
	Frequency ratio DCMI_PIXCLK/ f_{HCLK}	-	0.4	
DCMI_PIXCLK	Pixel clock input	-	54	MHz
D_{pixel}	Pixel clock input duty cycle	30	70	%

Device marking for LQFP176

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

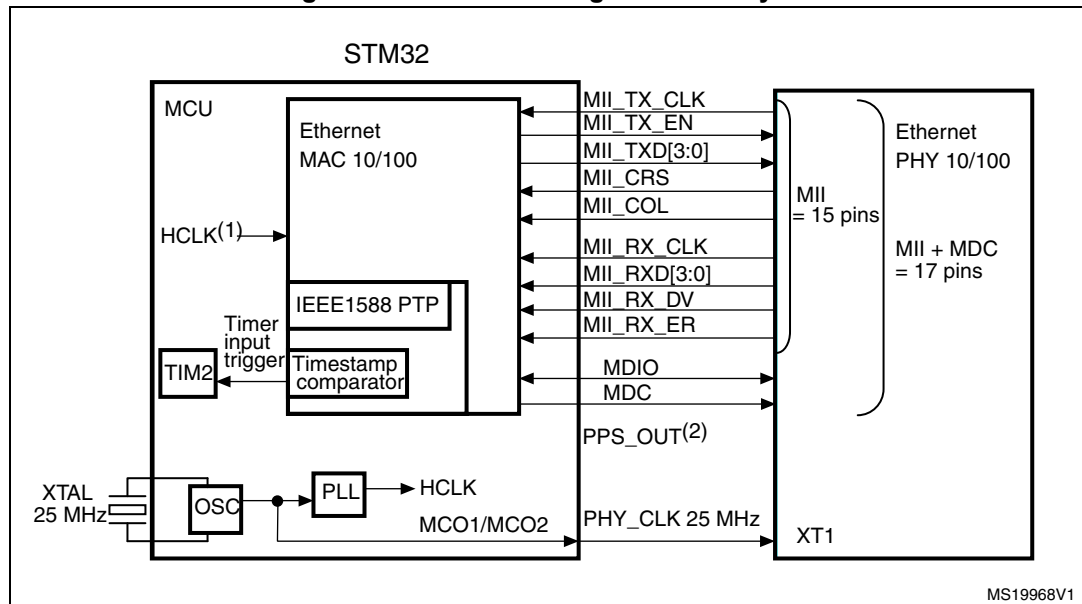
Figure 92. LQFP176 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

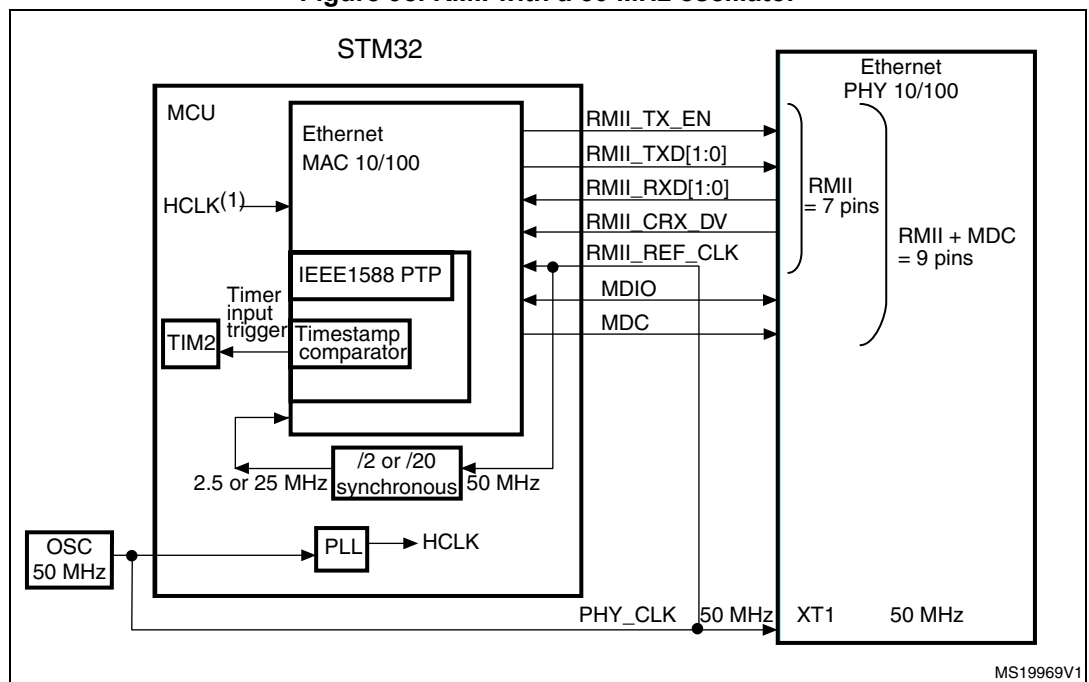
A.3 Ethernet interface solutions

Figure 97. MII mode using a 25 MHz crystal



1. f_{HCLK} must be greater than 25 MHz.
2. Pulse per second when using IEEE1588 PTP optional signal.

Figure 98. RMII with a 50 MHz oscillator



1. f_{HCLK} must be greater than 25 MHz.

Table 100. Document revision history (continued)

Date	Revision	Changes
06-Mar-2015	5	<p>Replace Cortex-M4F by Cortex-M4 with FPU throughout the document.</p> <p>Updated Section : Regulator OFF and Table 3: Regulator ON/OFF and internal reset ON/OFF availability for LQFP176.</p> <p>Updated Figure 15: STM32F41xxx LQFP176 pinout and Table 7: STM32F41xxx pin and ball definitions.</p> <p>Updated Figure 6: Multi-AHB matrix.</p> <p>Added note 1 below Figure 12: STM32F41xxx LQFP64 pinout, Figure 13: STM32F41xxx LQFP100 pinout, Figure 14: STM32F41xxx LQFP144 pinout and Figure 15: STM32F41xxx LQFP176 pinout.</p> <p>Updated I_{VDD} and I_{VSS} in Table 12: Current characteristics.</p> <p>Updated PLS[2:0]=101 (falling edge) configuration in Table 19: Embedded reset and power control block characteristics.</p> <p>Added Section : Additional current consumption. Updated Section : On-chip peripheral current consumption.</p> <p>Updated Table 29: Low-power mode wakeup timings.</p> <p>Updated Table 32: HSE 4-26 MHz oscillator characteristics and Table 33: LSE oscillator characteristics (fLSE = 32.768 kHz).</p> <p>Changed condition related to $V_{ESD(CDM)}$ in Table 45: ESD absolute maximum ratings.</p> <p>Updated Table 47: I/O current injection susceptibility, Table 48: I/O static characteristics, Table 49: Output voltage characteristics conditions, Table 50: I/O AC characteristics and Figure 37: I/O AC characteristics definition.</p> <p>Updated Section : I2C interface characteristics.</p> <p>Remove note 3 in Table 69: Temperature sensor characteristics.</p> <p>Updated Figure 72: DCMI timing diagram.</p> <p>Modified Figure 75: WLCSP90 - 4.223 x 3.969 mm, 0.400 mm pitch wafer level chip scale package outline and Table 90: WLCSP90 - 4.223 x 3.969 mm, 0.400 mm pitch wafer level chip scale package mechanical data. Added Figure 76: WLCSP90 - 4.223 x 3.969 mm, 0.400 mm pitch wafer level chip scale recommended footprint and Table 91: WLCSP90 recommended PCB design rules.</p> <p>Modified Figure 78: LQFP64 – 64-pin, 10 x 10 mm low-profile quad flat package outline and Table 92: LQFP64 – 64-pin 10 x 10 mm low-profile quad flat package mechanical data.</p> <p>Updated Figure 87: UFBGA176+25 ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline and Table 95: UFBGA176+25 ball, 10 x 10 x 0.65 mm pitch, ultra thin fine pitch ball grid array mechanical data. Added Figure 88: UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array recommended footprint and Table 96: UFBGA176+2 recommended PCB design rules (0.65 mm pitch BGA).</p> <p>Updated Figure 90: LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package outline.</p> <p>Added Section : Device marking for WLCSP90, Section : Device marking for LQFP64, Section : Device marking for LFP100, Section : Device marking for LQPF144, Section : Device marking for UFBGA176+25 and Section : Device marking for LQFP176.</p>