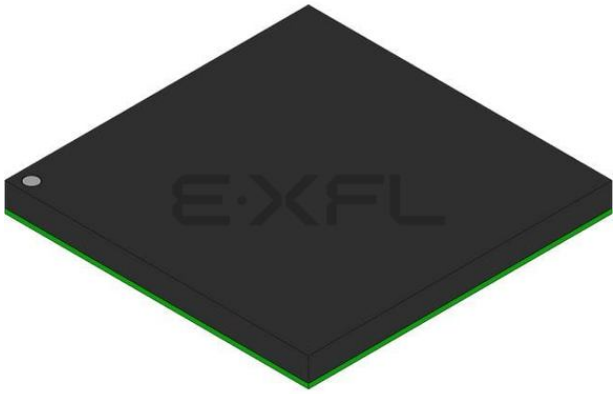

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Understanding Embedded - Microprocessors

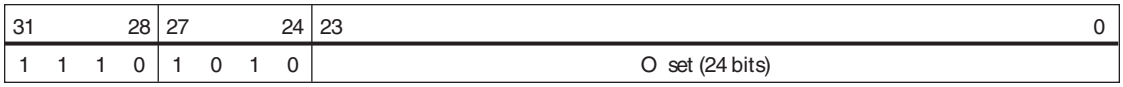
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, LPSDR, DDR2, SDR, SRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD, Touchscreen, Video Decoder
Ethernet	10/100Mbps
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	324-TFBGA
Supplier Device Package	324-TFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at91sam9m10-cu

Figure 11-5. B Opcode



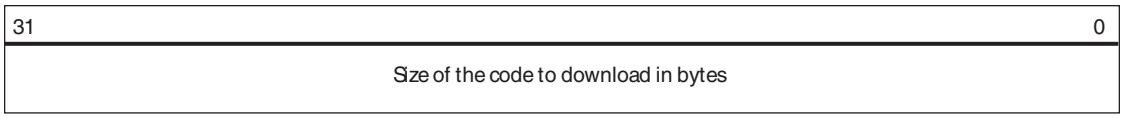
Unconditional instruction: 0xE for bits 31 to 28

Load PC with PC relative addressing instruction:

- Rn = Rd = PC = 0xF
- I==0 (12-bit immediate value)
- P==1 (pre-indexed)
- U offset added (U==1) or subtracted (U==0)
- W==1

The sixth vector, at offset 0x14, contains the size of the image to download. The user must replace this vector with his/her own vector. This information is described below.

Figure 11-6. Structure of the ARM Vector 6



The value has to be smaller than 60 KBytes. 60 KBytes is the maximum size for a valid code. This size is the internal SRAM size minus the stack size used by the ROM Code at the end of the internal SRAM.

Example

An example of valid vectors follows:

```
00    ea000006  B       0x20
04    eafffffe  B       0x04
08    ea00002f  B       _main
0c    eafffffe  B       0x0c
10    eafffffe  B       0x10
14    00001234  B       0x14      <- Code size = 4660 bytes < 60KB
18    eafffffe  B       0x18
```

11.4.2.2 boot.bin file check

The NVM bootloader program looks for a boot.bin file in the root directory of a FAT12/16/32 formatted NVM Flash.

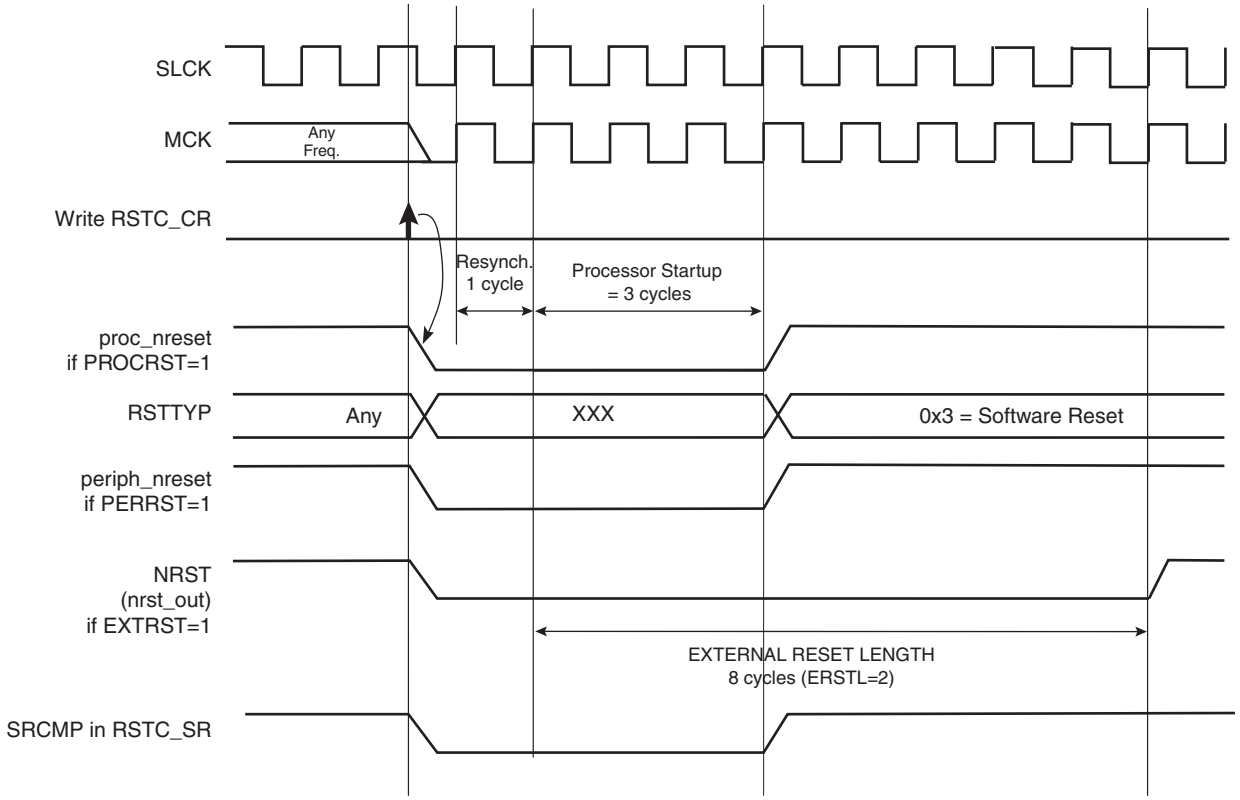
The internal reset signals are asserted as soon as the register write is performed. This is detected on the Master Clock (MCK). They are released when the software reset is left, i.e.; synchronously to SLCK.

If EXTRST is set, the nrst_out signal is asserted depending on the programming of the field ERSTL. However, the resulting falling edge on NRST does not lead to a User Reset.

If and only if the PROCRST bit is set, the Reset Controller reports the software status in the field RSTTYP of the Status Register (RSTC_SR). Other Software Resets are not reported in RSTTYP.

As soon as a software operation is detected, the bit SRCMP (Software Reset Command in Progress) is set in the Status Register (RSTC_SR). It is cleared as soon as the software reset is left. No other software reset can be performed while the SRCMP bit is set, and writing any value in RSTC_CR has no effect.

Figure 12-7. Software Reset



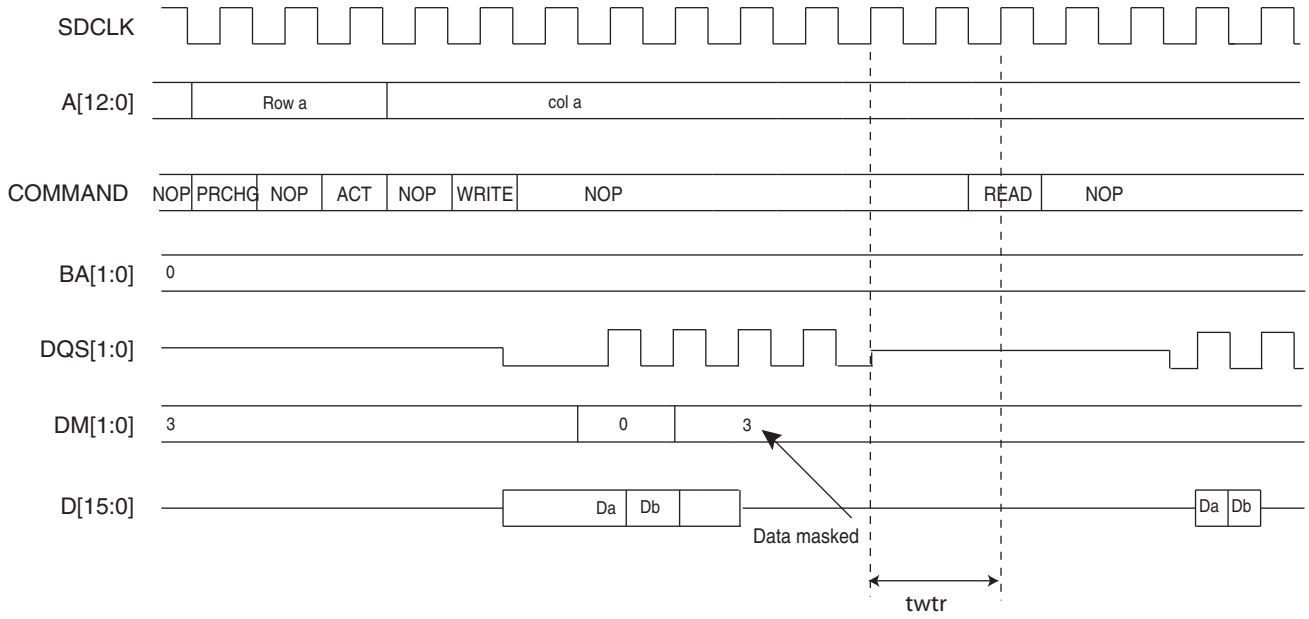
12.4.4.5 Watchdog Reset

The Watchdog Reset is entered when a watchdog fault occurs. This state lasts 3 Slow Clock cycles.

When in Watchdog Reset, assertion of the reset signals depends on the WDRPROC bit in WDT_MR:

- If WDRPROC is 0, the Processor Reset and the Peripheral Reset are asserted. The NRST line is also asserted, depending on the programming of the field ERSTL. However, the resulting low level on NRST does not result in a User Reset state.

Figure 22-10. SINGLE Write Access Followed By A Read Access, DDR2 -SDRAM Device



22.5.2 SDRAM Controller Read Cycle

The DDRSDRC allows burst access or single access in normal mode (mode =000). Whatever access type, the DDRSDRC keeps track of the active row in each bank, thus maximizing performance of the DDRSDRC.

The SDRAM devices are programmed with a burst length equal to 8 which determines the length of a sequential data output by the read command that is set to 8. The latency from read command to data output is equal to 2 or 3. This value is programmed during the initialization phase (see Section 22.4.1 “SDR-SDRAM Initialization” on page 232).

To initiate a single access, the DDRSDRC checks if the page access is already open. If row/bank addresses match with the previous row/bank addresses, the controller generates a read command. If the bank addresses are not identical or if bank addresses are identical but the row addresses are not identical, the controller generates a precharge command, activates the new row and initiates a read command. To comply with SDRAM timing parameters, additional clock cycles are inserted between precharge/active (Trp) commands and active/read (Trcd) command. After a read command, additional wait states are generated to comply with cas latency. The DDRSDRC supports a cas latency of two, two and half, and three (2 or 3 clocks delay). As the burst length is fixed to 8, in the case of single access or burst access inferior to 8 data requests, it has to stop the burst otherwise seven or X values could be read. Burst Stop Command (BST) is used to stop output during a burst read.

To initiate a burst access, the DDRSDRC checks the transfer type signal. If the next accesses are sequential read accesses, reading to the SDRAM device is carried out. If the next access is a read non-sequential access, then an automatic page break can be inserted. If the bank addresses are not identical or if bank addresses are identical but the row addresses are not identical, the controller generates a precharge command, activates the new row and initiates a read command. In the case where the page access is already open, a read command is generated.

27.9.2 AIC Source Mode Register

Name: AIC_SMR0..AIC_SMR31

Address: 0xFFFFF000

Access: Read-write

Reset Value: 0x0

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	SRCTYPE		–	–	PRIOR		

- **PRIOR: Priority Level**

Programs the priority level for all sources except FIQ source (source 0).

The priority level can be between 0 (lowest) and 7 (highest).

The priority level is not used for the FIQ in the related SMR register AIC_SMRx.

- **SRCTYPE: Interrupt Source Type**

The active level or edge is not programmable for the internal interrupt sources.

SRCTYPE		Internal Interrupt Sources	External Interrupt Sources
0	0	High level Sensitive	Low level Sensitive
0	1	Positive edge triggered	Negative edge triggered
1	0	High level Sensitive	High level Sensitive
1	1	Positive edge triggered	Positive edge triggered

30.6.25 PIO Peripheral B Select Register

Name: PIO_BSR

Addresses: 0xFFFFF274 (PIOA), 0xFFFFF474 (PIOB), 0xFFFFF674 (PIOC), 0xFFFFF874 (PIOD), 0xFFFFFA74 (PIOE)

Access: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Peripheral B Select.**

0 = No effect.

1 = Assigns the I/O line to the peripheral B function.

30.6.26 PIO Peripheral A B Status Register

Name: PIO_ABSR

Addresses: 0xFFFFF278 (PIOA), 0xFFFFF478 (PIOB), 0xFFFFF678 (PIOC), 0xFFFFF878 (PIOD), 0xFFFFFA78 (PIOE)

Access: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Peripheral A B Status.**

0 = The I/O line is assigned to the Peripheral A.

1 = The I/O line is assigned to the Peripheral B.

– Check the LIN errors

Figure 31-49. Slave Node Configuration, NACT = PUBLISH

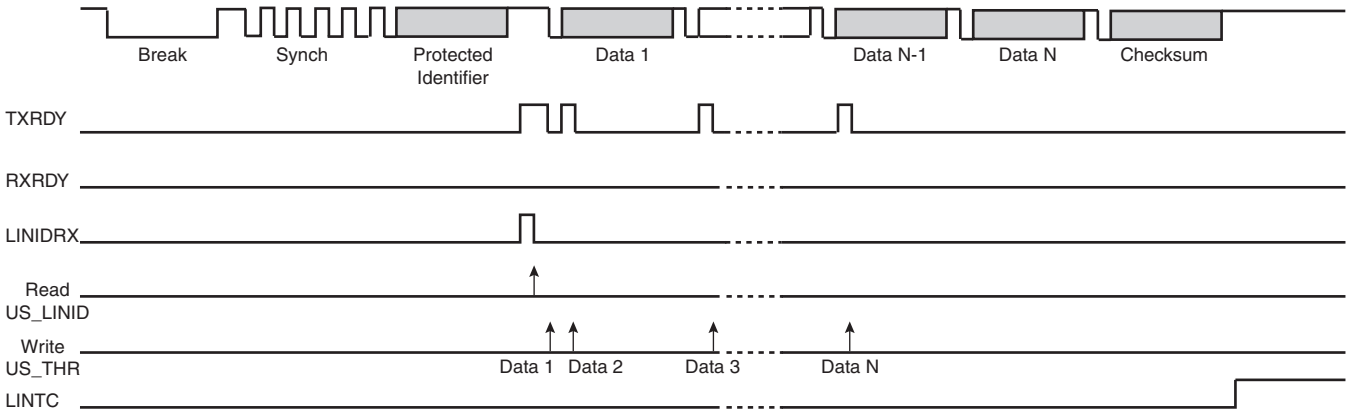


Figure 31-50. Slave Node Configuration, NACT = SUBSCRIBE

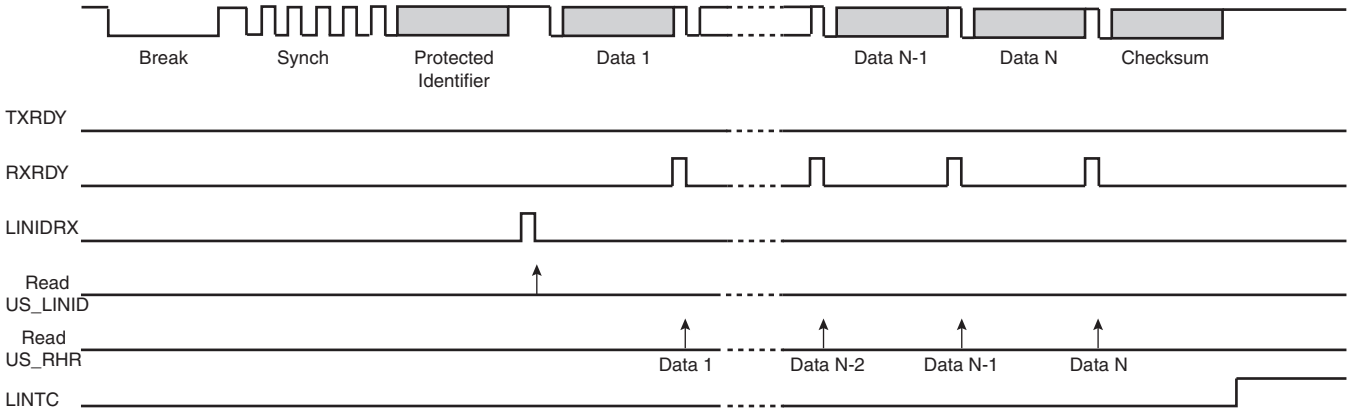
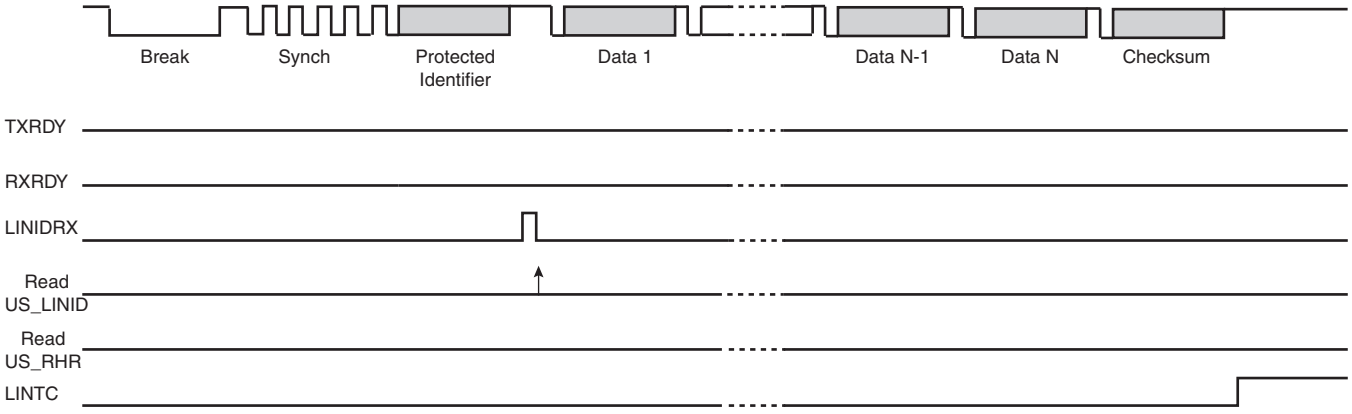


Figure 31-51. Slave Node Configuration, NACT = IGNORE



31.7.8.22 LIN Frame Handling With The Peripheral DMA Controller

The USART can be used in association with the Peripheral DMA Controller (PDC) in order to transfer data directly into/from the on- and off-chip memories without any processor intervention.

31.8.10 USART Receiver Time-out Register

Name: US_RTOR

Addresses: 0xFFF8C024 (0), 0xFFF90024 (1), 0xFFF94024 (2), 0xFFF98024 (3)

Access: Read-write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	TO
15	14	13	12	11	10	9	8
TO							
7	6	5	4	3	2	1	0
TO							

- **TO: Time-out Value**

0: The Receiver Time-out is disabled.

1 - 131071: The Receiver Time-out is enabled and the Time-out delay is TO x Bit Period.

33.9.6 SSC Transmit Frame Mode Register

Name: SSC_TFMR

Addresses: 0xFFF9C01C (0), 0xFFFA001C (1)

Access: Read-write

31	30	29	28	27	26	25	24
FSLEN_EXT	FSLEN_EXT	FSLEN_EXT	FSLEN_EXT	–	–	–	FSEDGE
23	22	21	20	19	18	17	16
FSDEN	FSOS			FSLEN			
15	14	13	12	11	10	9	8
–	–	–	–	DATNB			
7	6	5	4	3	2	1	0
MSBF	–	DATDEF	DATLEN				

- **DATLEN: Data Length**

0 = Forbidden value (1-bit data length not supported).

Any other value: The bit stream contains DATLEN + 1 data bits. Moreover, it defines the transfer size performed by the PDC assigned to the Transmit. If DATLEN is lower or equal to 7, data transfers are bytes, if DATLEN is between 8 and 15 (included), half-words are transferred, and for any other value, 32-bit words are transferred.

- **DATDEF: Data Default Value**

This bit defines the level driven on the TD pin while out of transmission. Note that if the pin is defined as multi-drive by the PIO Controller, the pin is enabled only if the SCC TD output is 1.

- **MSBF: Most Significant Bit First**

0 = The lowest significant bit of the data register is shifted out first in the bit stream.

1 = The most significant bit of the data register is shifted out first in the bit stream.

- **DATNB: Data Number per frame**

This field defines the number of data words to be transferred after each transfer start, which is equal to (DATNB +1).

- **FSLEN: Transmit Frame Syn Length**

This field defines the length of the Transmit Frame Sync signal and the number of bits shifted out from the Transmit Sync Data Register if FSDEN is 1.

This field is used with FSLEN_EXT to determine the pulse length of the Transmit Frame Sync signal.

Pulse length is equal to FSLEN + (FSLEN_EXT * 16) + 1 Transmit Clock period.

36.6.16 Specific Address 1 Bottom Register

Name: EMAC_SA1B

Address: 0xFFFBC098

Access: Read-write

31	30	29	28	27	26	25	24
ADDR							

23	22	21	20	19	18	17	16
ADDR							

15	14	13	12	11	10	9	8
ADDR							

7	6	5	4	3	2	1	0
ADDR							

- **ADDR**

Least significant bits of the destination address. Bit zero indicates whether the address is multicast or unicast and corresponds to the least significant bit of the first byte received.

36.6.17 Specific Address 1 Top Register

Name: EMAC_SA1T

Address: 0xFFFBC09C

Access: Read-write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
ADDR							

7	6	5	4	3	2	1	0
ADDR							

- **ADDR**

The most significant bits of the destination address, that is bits 47 to 32.

Table 38-1. UDPHS Endpoint Description

Endpoint #	Mnemonic	Nb Bank	DMA	High BandWidth	Max. Endpoint Size	Endpoint Type
0	EPT_0	1	N	N	64	Control
1	EPT_1	2	Y	Y	1024	Ctrl/Bulk/Iso(1)/Interrupt
2	EPT_2	2	Y	Y	1024	Ctrl/Bulk/Iso(1)/Interrupt
3	EPT_3	3	Y	N	1024	Ctrl/Bulk/Iso(1)/Interrupt
4	EPT_4	3	Y	N	1024	Ctrl/Bulk/Iso(1)/Interrupt
5	EPT_5	3	Y	Y	1024	Ctrl/Bulk/Iso(1)/Interrupt
6	EPT_6	3	Y	Y	1024	Ctrl/Bulk/Iso(1)/Interrupt

Note: 1. In Isochronous Mode (Iso), it is preferable that High Band Width capability is available.

The size of internal DPRAM is 4 KB.

Suspend and resume are automatically detected by the UDPHS device, which notifies the processor by raising an interrupt.

38.6.22 UDPHS DMA Channel Status Register

Name: UDPHS_DMASTATUSx [x = 1..5]

Addresses: 0xFFF7832C [1], 0xFFF7833C [2], 0xFFF7834C [3], 0xFFF7835C [4], 0xFFF7836C [5]

Access: Read-write

31	30	29	28	27	26	25	24
BUFF_COUNT							
23	22	21	20	19	18	17	16
BUFF_COUNT							
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	DESC_LDST	END_BF_ST	END_TR_ST	–	–	CHANN_ACT	CHANN_ENB

- **CHANN_ENB: Channel Enable Status**

0 = if cleared, the DMA channel no longer transfers data, and may load the next descriptor if the UDPHS_DMACONTROLx register LDNXT_DSC bit is set.

When any transfer is ended either due to an elapsed byte count or a UDPHS device initiated transfer end, this bit is automatically reset.

1 = if set, the DMA channel is currently enabled and transfers data upon request.

This bit is normally set or cleared by writing into the UDPHS_DMACONTROLx register CHANN_ENB bit field either by software or descriptor loading.

If a channel request is currently serviced when the UDPHS_DMACONTROLx register CHANN_ENB bit is cleared, the DMA FIFO buffer is drained until it is empty, then this status bit is cleared.

- **CHANN_ACT: Channel Active Status**

0 = the DMA channel is no longer trying to source the packet data.

When a packet transfer is ended this bit is automatically reset.

1 = the DMA channel is currently trying to source packet data, i.e. selected as the highest-priority requesting channel.

When a packet transfer cannot be completed due to an END_BF_ST, this flag stays set during the next channel descriptor load (if any) and potentially until UDPHS packet transfer completion, if allowed by the new descriptor.

- **END_TR_ST: End of Channel Transfer Status**

0 = cleared automatically when read by software.

1 = set by hardware when the last packet transfer is complete, if the UDPHS device has ended the transfer.

Valid until the CHANN_ENB flag is cleared at the end of the next buffer transfer.

- **END_BF_ST: End of Channel Buffer Status**

0 = cleared automatically when read by software.

1 = set by hardware when the BUFF_COUNT downcount reach zero.

Valid until the CHANN_ENB flag is cleared at the end of the next buffer transfer.

39.5.16 DMA Channel Disable Register

Name: DMA_CHDR

Access: Write

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	C_CH_DIS	P_CH_DIS

- **P_CH_DIS**

Write one to this field to disable the channel. Poll P_CH_S in DMA_CHSR to verify that the preview channel status has been successfully modified.

- **C_CH_DIS**

Write one to this field to disabled the channel. Poll C_CH_S in DMA_CHSR to verify that the codec channel status has been successfully modified.

40.11.10 TSADCC Last Converted Data Register

Name: TSADCC_LCDR

Address: 0xFFFB0020

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	LDATA	
7	6	5	4	3	2	1	0
LDATA							

- **LDATA: Last Data Converted**

The analog-to-digital conversion data is placed into this register at the end of a conversion on any analog channel and remains until a new conversion on any analog channel is completed.

43.8.12 AC97 Controller Channel B Mode Register

Name: AC97C_CBMR

Address: 0xFFFAC03C

Access: Read-write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	PDCEN	CEN	–	–	CEM	SIZE	
15	14	13	12	11	10	9	8
RXBUFF	ENDRX	–	–	TXBUFE	ENDTX	–	–
7	6	5	4	3	2	1	0
–	–	OVRUN	RXRDY	–	UNRUN	TXEMPTY	TXRDY

- **TXRDY: Channel Transmit Ready Interrupt Enable**
- **TXEMPTY: Channel Transmit Empty Interrupt Enable**
- **UNRUN: Transmit Underrun Interrupt Enable**
- **RXRDY: Channel Receive Ready Interrupt Enable**
- **OVRUN: Receive Overrun Interrupt Enable**
- **ENDTX: End of Transmission for Channel B Interrupt Enable**
- **TXBUFE: Transmit Buffer Empty for Channel B Interrupt Enable**

0: Read: the corresponding interrupt is disabled. Write: disables the corresponding interrupt.

1: Read: the corresponding interrupt is enabled. Write: enables the corresponding interrupt.

- **ENDRX: End of Reception for Channel B Interrupt Enable**

0: Read: the corresponding interrupt is disabled. Write: disables the corresponding interrupt.

1: Read: the corresponding interrupt is enabled. Write: enables the corresponding interrupt.

- **RXBUFF: Receive Buffer Full for Channel B Interrupt Enable**

0: Read: the corresponding interrupt is disabled. Write: disables the corresponding interrupt.

1: Read: the corresponding interrupt is enabled. Write: enables the corresponding interrupt.

- **SIZE: Channel B Data Size**

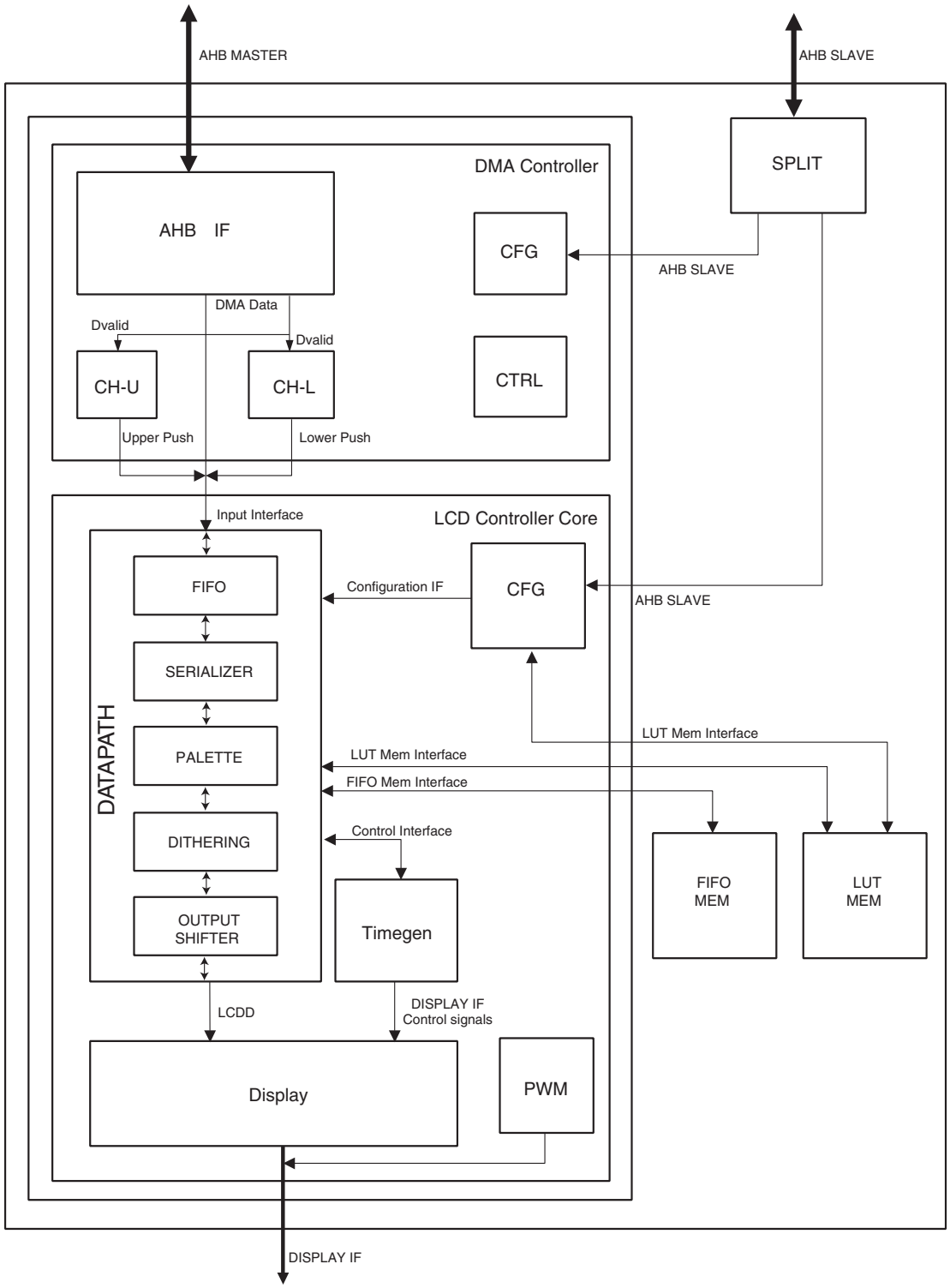
SIZE Encoding

SIZE	Selected Data Size
0x0	20 bits
0x1	18 bits
0x2	16 bits
0x3	10 bits

Note: Each time slot in the data phase is 20 bit long. For example, if a 16-bit sample stream is being played to an AC 97 DAC, the first 16 bit positions are presented to the DAC MSB-justified. They are followed by the next four bit positions that the AC97 Controller

45.3 Block Diagram

Figure 45-1. LCD Macrocell Block Diagram



45.12.11 LCD Control Register 2

Name: LCDCON2

Address:0x00500804

Access: Read-write

Reset value: 0x0000000

31	30	29	28	27	26	25	24
MEMOR		–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
CLKMOD	–	–	INVDVAL	INVCLK	INVLINE	INVFRAME	INVVD
7	6	5	4	3	2	1	0
PIXELSIZE			IFWIDTH		SCANMOD	DISTYPE	

- **DISTYPE: Display Type**

DISTYPE		
0	0	STN Monochrome
0	1	STN Color
1	0	TFT
1	1	Reserved

- **SCANMOD: Scan Mode**

0: Single Scan

1: Dual Scan

- **IFWIDTH: Interface width (STN)**

IFWIDTH		
0	0	4-bit (Only valid in single scan STN mono or color)
0	1	8-bit (Only valid in STN mono or Color)
1	0	16-bit (Only valid in dual scan STN mono or color)
1	1	Reserved

46.10 Video Decoder Register Mapping (MPEG-2/MPEG-1)

Table 46-14. Video Decoder Register Mapping (MPEG-2/MPEG-1)

Offset	Register	Name	Access	Reset
0x0000	ID Register	VDEC_IDR	Read-only	0x81700880
0x0004	Decoder Interrupt Register	VDEC_DIR	Read-write	0x00000000
0x0008	Decoder Device Configuration Register	VDEC_DDCR	Read-write	0x00000400
0x000C	Decoder Control Register 0	VDEC_CTLR0	Read-write	0x00000000
0x0010	Decoder Control Register 1	VDEC_CTLR1	Read-write	0x00000000
0x0014	Decoder Control Register 2	VDEC_CTLR2	Read-write	0x00000000
0x0018	Decoder Control Register 3	VDEC_CTLR3	Read-write	0x00000000
0x001C - 0x002C	Reserved	–	–	–
0x0030	RLC/VLC Data Base Address	VDEC_RLCVLCBA	Read-write	0x00000000
0x0034	Decoded Picture Base Address	VDEC_PICTBA	Read-write	0x00000000
0x0038	Reference Picture Index 0 Base Address	VDEC_PIDXBA0	Read-write	0x00000000
0x003C	Reference Picture Index 1 Base Address	VDEC_PIDXBA1	Read-write	0x00000000
0x0040	Reference Picture Index 2 Base Address	VDEC_PIDXBA2	Read-write	0x00000000
0x0044	Reference Picture Index 3 Base Address	VDEC_PIDXBA3	Read-write	0x00000000
0x0048	Reference Picture Index 4 Base Address	VDEC_PIDXBA4	Read-write	0x00000000
0x004C - 0x009C	Reserved	–	–	–
0x00A0	Standard Dependent Tables Base Address	VDEC_SDTBA	Read-write	0x00000000
0x00A4	Direct Mode Motion Vector Base Address	VDEC_DMMVBA	Read-write	0x00000000
0x00A8 - 0x00BC	Reserved	–	–	–
0x00C0	Error Concealment Register	VDEC_ECR	Read-write	0x00000000
0x00C4	Reserved	–	–	–
0x00C8	Reserved	–	–	0xF9019500

Figure 47-9. SPI Slave Mode - NPCS Timings

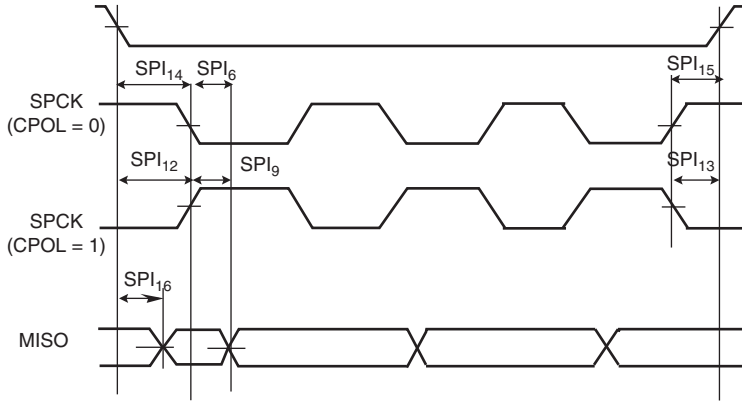
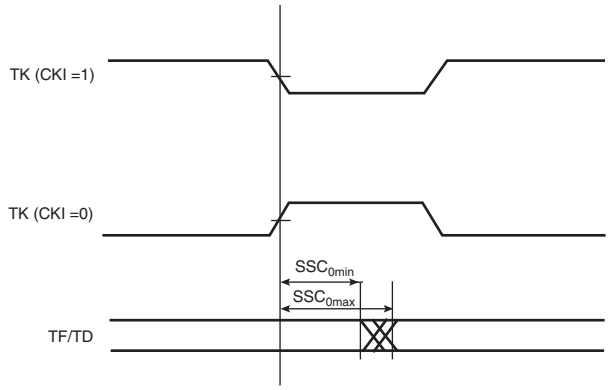


Table 47-33. SPI Timings with 3.3V Peripheral Supply

Symbol	Parameter	Cond	Min	Max	Units
Master Mode					
SPI_{SPCK}	SPI Clock			66	MHz
SPI_0	MISO Setup time before SPCK rises		14.6		ns
SPI_1	MISO Hold time after SPCK rises		0		ns
SPI_2	SPCK rising to MOSI		0	0.2	ns
SPI_3	MISO Setup time before SPCK falls		14.3		ns
SPI_4	MISO Hold time after SPCK falls		0		ns
SPI_5	SPCK falling to MOSI		0	0.6	ns
Slave Mode					
SPI_6	SPCK falling to MISO		4.6	15.1	ns
SPI_7	MOSI Setup time before SPCK rises		0.7		ns
SPI_8	MOSI Hold time after SPCK rises		1.9		ns
SPI_9	SPCK rising to MISO		4.6	15.2	ns
SPI_{10}	MOSI Setup time before SPCK falls		0.9		ns
SPI_{11}	MOSI Hold time after SPCK falls		1.4		ns
SPI_{12}	NPCS0 setup to SPCK rising		17.3		ns
SPI_{13}	NPCS0 hold after SPCK falling		15.1		ns
SPI_{14}	NPCS0 setup to SPCK falling		18		ns
SPI_{15}	NPCS0 hold after SPCK rising		15.0		ns
SPI_{16}	NPCS0 falling to MISO valid		4.4	14.5	ns

Figure 47-18. Min and Max Access Time of Output Signals



47.15.3 ISI

47.15.3.1 Timing Conditions

Timings are given assuming capacitance loads on Table 47-38.

Table 47-38. Capacitance Load

	Corner	
Supply	MAX	MIN
3.3V	30pF	0 pF
1.8V	20pF	0 pF

47.15.3.2 Timing Extraction

Figure 47-19. ISI Timing Diagram

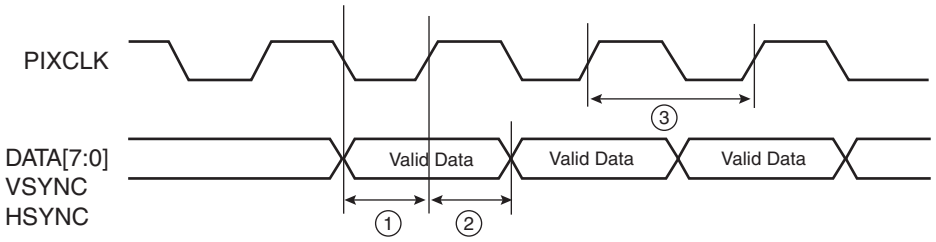


Table 47-39. ISI Timings with 3.3V Peripheral Supply

Symbol	Parameter	Min	Max	Units
ISI_1	DATA/VSYNC/HSYNC setup time	1.1		ns
ISI_2	DATA/VSYNC/HSYNC hold time	2.0		ns
ISI_3	PIXCLK frequency		80	MHz

Problem Fix/Workaround

None

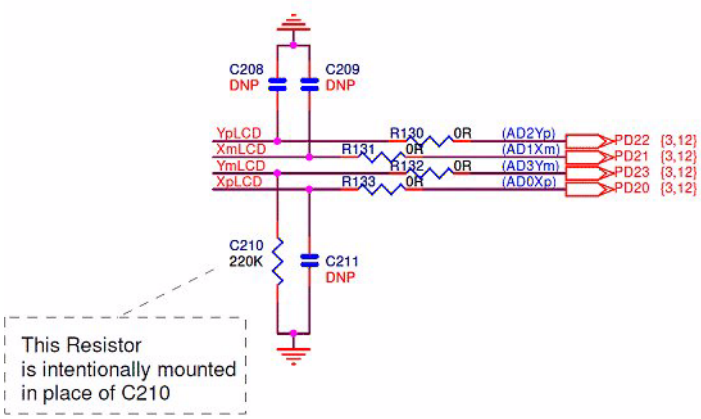
50.1.7 Touch Screen (TSADCC)

50.1.7.1 TSADCC: Pen detect accuracy is not good

Depending on LCD panels, the pen detect is noisy, leading to an unpredictable behavior.

Problem Fix/Workaround

An additional resistor solves the problem. Its value (between 100 kOhm and 250 kOhm) is to be tuned for the LCD panel.



50.1.8 USB High Speed Host Port (UHPHS)

50.1.8.1 UHPHS: Packet Loss Issue in the UTMI Transceivers

High-Speed USB Host may lose incoming packets when connected to an external USB Hub.

A high data transfer error rate has been observed on the High-Speed USB Host interface when connected to an external USB Hub. The USB remains functional but the errors may require a reset of the USB interface to recover.

The Full-Speed USB Host operation is not affected by this problem.

Problem Fix/Workaround

A workaround consists of implementing a timeout on the USB communication using one of the timers in the device and trigger a reset of the USB Host interface via software and restart the communication. The impact of the workaround on the data rate is dependent on the error rate observed in the application but can be such that streaming data at high rates becomes impractical.

50.1.9 USB High Speed Host Port (UHPHS) and Device Port (UDPHS)

50.1.9.1 UHPHS/UDPHS: USB does not start after power-up

The USB may not start properly at first use after power-up.

Booting out of the internal ROM fixes this issue because the workaround below is applied in the ROM Code.