# Analog Devices Inc./Maxim Integrated - 73S1210F-44IMR/F/P Datasheet

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | 80515 |
| Core Size | 8-Bit |
| Speed | 24MHz |
| Connectivity | I²C, SmartCard, UART/USART |
| Peripherals | LED, POR, WDT |
| Number of I/O | 8 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 6.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-VFQFN Exposed Pad |
| Supplier Device Package | 44-QFN (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/73s1210f-44imr-f-p |

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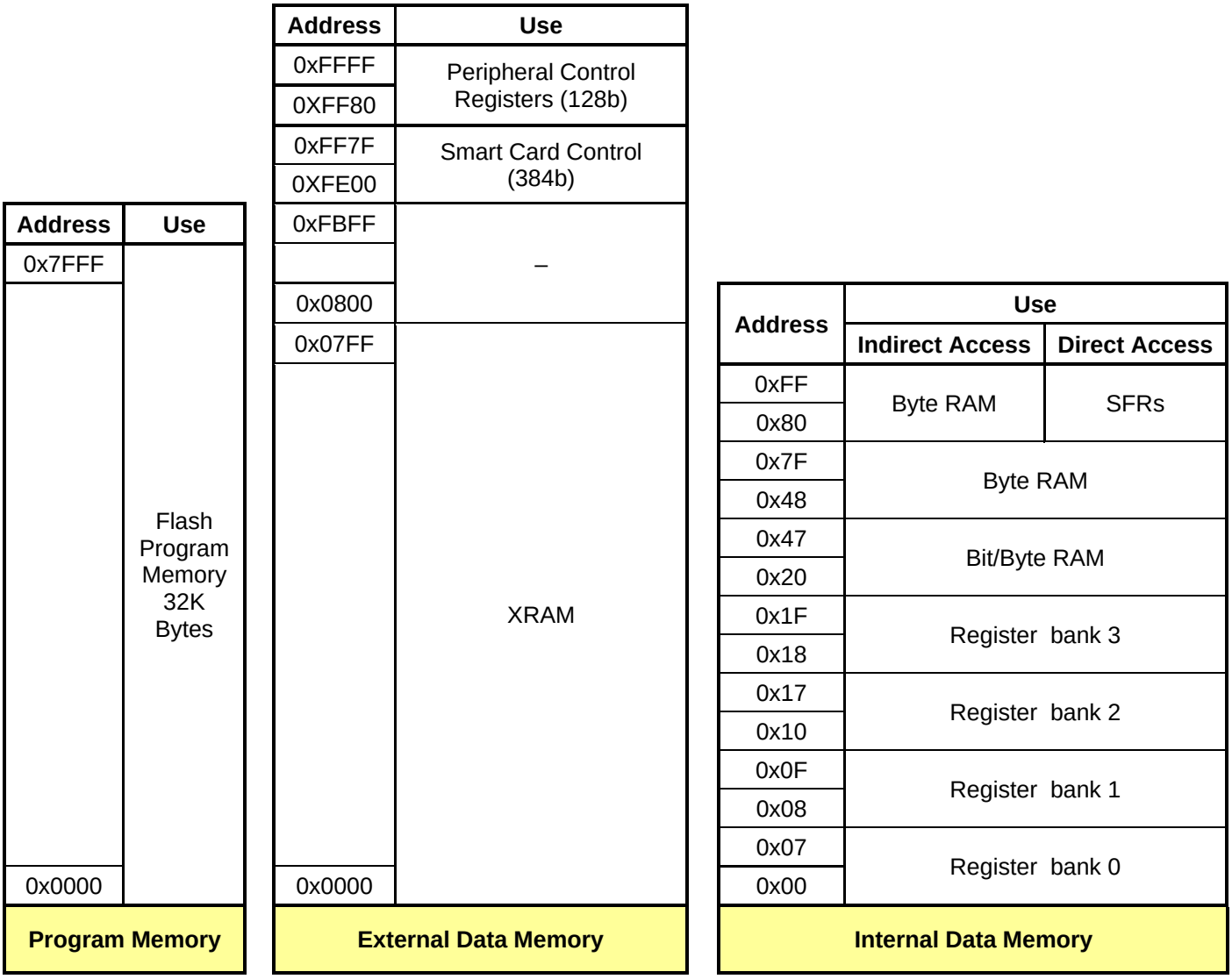
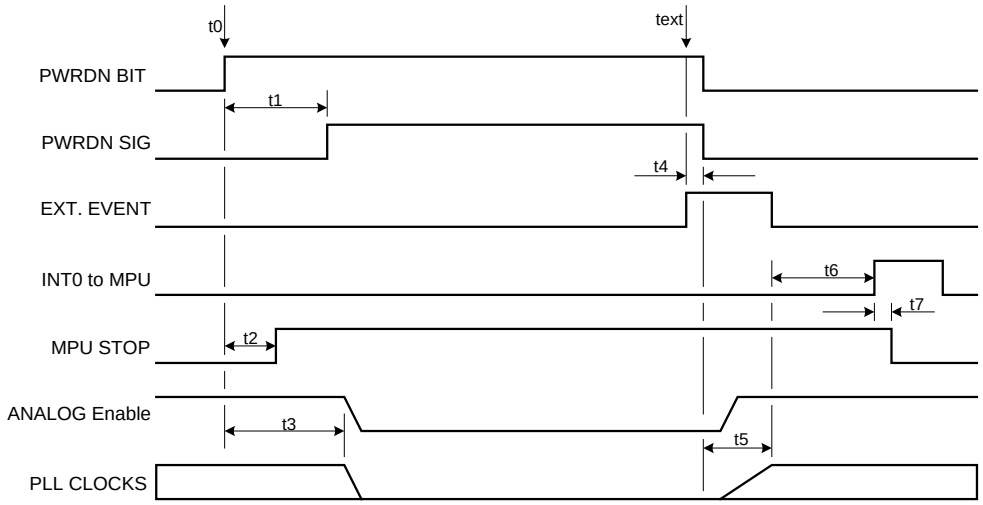



**Figure 2: Memory Map**

**Dual Data Pointer:** The Dual Data Pointer accelerates the block moves of data. The standard DPTR is a 16-bit register that is used to address external memory. In the 80515 core, the standard data pointer is called DPTR, the second data pointer is called DPTR1. The data pointer select bit chooses the active pointer. The data pointer select bit is located at the LSB of the DPS IRAM special function register (DPS.0). DPTR is selected when DPS.0 = 0 and DPTR1 is selected when DPS.0 = 1.

The user switches between pointers by toggling the LSB of the DPS register. All DPTR-related instructions use the currently selected DPTR for any activity.

**The second data pointer may not be supported by certain compilers.**




**t0**: MPU sets PWRDN bit.

**t1**: 32 MPU clock cycles after t0, the PWRDN SIG is asserted, turning all analog functions OFF.

**t2**: MPU executes STOP instruction, must be done prior to t1.

**t3**: Analog functions go to OFF condition. No Vref, PLL/VCO, Ibias, etc.

**text**: An external event (RTC, Keypad, Card event, USB) occurs.

**t4**: PWRDN bit and PWRDN signal are cleared by external event.

**t5**: High-speed oscillator/PLL/VCO operating.

**t6**: After 512 MPU clock cycles, INT0 to MPU is asserted.

**t7**: INT0 causes MPU to exit STOP condition.

**Figure 8: Power Down Sequencing**

**Interrupt Enable 1 Register (IEN1): 0xB8 ← 0x00**

**Table 20: The IEN1 Register**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| – | SWDT | EX6 | EX5 | EX4 | EX3 | EX2 | – |

| Bit | Symbol | Function |
|---|---|---|
| IEN1.7 | – | |
| IEN1.6 | SWDT | Not used for interrupt control. |
| IEN1.5 | EX6 | EX6 = 0 – disable external interrupt 6. |
| IEN1.4 | EX5 | EX5 = 0 – disable external interrupt 5. |
| IEN1.3 | EX4 | EX4 = 0 – disable external interrupt 4. |
| IEN1.2 | EX3 | EX3 = 0 – disable external interrupt 3. |
| IEN1.1 | EX2 | EX2 = 0 – disable external interrupt 2. |
| IEN1.0 | – | |

**Interrupt Enable 2 Register (IEN2): 0x9A ← 0x00**

**Table 21: The IEN2 Register**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | – | ES1 |

| Bit | Symbol | Function |
|---|---|---|
| IEN2.0 | ES1 | ES1 = 0 – disable serial channel interrupt. |

**Table 26: Control Bits for External Interrupts**

| Enable Bit | Description |
|---|---|
| EX0 | Enable external interrupt 0 |
| EX1 | Enable external interrupt 1 |
| EX2 | Enable external interrupt 2 |
| EX3 | Enable external interrupt 3 |
| EX4 | Enable external interrupt 4 |
| EX5 | Enable external interrupt 5 |
| EX6 | Enable external interrupt 6 |

| Flag Bit | Description |
|---|---|
| IE0 | External interrupt 0 flag |
| IE1 | External interrupt 1 flag |
| IEX2 | External interrupt 2 flag |
| IEX3 | External interrupt 3 flag |
| IEX4 | External interrupt 4 flag |
| IEX5 | External interrupt 5 flag |
| IEX6 | External interrupt 6 flag |

#### 1.7.5.4 Power Down Interrupt Logic

The 73S1210F contains special interrupt logic to allow INT0 to wake up the CPU from a power down (CPU STOP) state. See the Power Control Modes section for details.

#### 1.7.5.5 Interrupt Priority Level Structure

All interrupt sources are combined in groups, as shown in Table 27.

**Table 27: Priority Level Groups**

| Group | | | |
|---|---|---|---|
| 0 | External interrupt 0 | Serial channel 1 interrupt | |
| 1 | Timer 0 interrupt | – | External interrupt 2 |
| 2 | External interrupt 1 | – | External interrupt 3 |
| 3 | Timer 1 interrupt | – | External interrupt 4 |
| 4 | Serial channel 0 interrupt | – | External interrupt 5 |
| 5 | – | – | External interrupt 6 |

Each group of interrupt sources can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1. If requests of the same priority level are received simultaneously, an internal polling sequence as per Table 31 determines which request is serviced first.

IEN enable bits must be set to permit any of these interrupts to occur. Likewise, each interrupt has its own flag bit that is set by the interrupt hardware and is reset automatically by the MPU interrupt handler.

**Interrupt Priority 0 Register (IP0): 0xA9 ← 0x00**

**Table 28: The IP0 Register**

MSB LSB

| – | WDTS | IP0.5 | IP0.4 | IP0.3 | IP0.2 | IP0.1 | IP0.0 |
|---|---|---|---|---|---|---|---|

Note: WDTS is not used for interrupt controls.

**Interrupt Priority 1 Register (IP1): 0xB9 ← 0x00**

**Table 29: The IP1 Register**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| – | – | IP1.5 | IP1.4 | IP1.3 | IP1.2 | IP1.1 | IP1.0 |

**Table 30: Priority Levels**

| IP1.x | IP0.x | Priority Level |
|---|---|---|
| 0 | 0 | Level0 (lowest) |
| 0 | 1 | Level1 |
| 1 | 0 | Level2 |
| 1 | 1 | Level3 (highest) |

**Table 31: Interrupt Polling Sequence**

| | |
|---|---|
| External interrupt 0 | Polling sequence |
| Serial channel 1 interrupt | |
| Timer 0 interrupt | |
| External interrupt 2 | |
| External interrupt 1 | |
| External interrupt 3 | |
| Timer 1 interrupt | |
| Serial channel 0 interrupt | |
| External interrupt 4 | |
| External interrupt 5 | |
| External interrupt 6 | |

#### 1.7.5.6 Interrupt Sources and Vectors

Table 32 shows the interrupts with their associated flags and vector addresses.

**Table 32: Interrupt Vectors**

| Interrupt Request Flag | Description | Interrupt Vector Address |
|---|---|---|
| N/A | Chip Reset | 0x0000 |
| IE0 | External interrupt 0 | 0x0003 |
| TF0 | Timer 0 interrupt | 0x000B |
| IE1 | External interrupt 1 | 0x0013 |
| TF1 | Timer 1 interrupt | 0x001B |
| RI0/TI0 | Serial channel 0 interrupt | 0x0023 |
| RI1/TI1 | Serial channel 1 interrupt | 0x0083 |
| IEX2 | External interrupt 2 | 0x004B |
| IEX3 | External interrupt 3 | 0x0053 |
| IEX4 | External interrupt 4 | 0x005B |
| IEX5 | External interrupt 5 | 0x0063 |
| IEX6 | External interrupt 6 | 0x006B |

**Miscellaneous Control Register 0 (MISCtl0): 0xFFF1 ← 0x00**

Transmit and receive (TX and RX) pin selection and loop back test configuration are setup via this register.

**Table 37: The MISCtl0 Register**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| PWRDN | – | – | – | – | – | SLPBK | SSEL |

| Bit | Symbol | Function |
|---|---|---|
| MISCtl0.7 | PWRDN | This bit places the 73S1210F into a power down state. |
| MISCtl0.6 | – | |
| MISCtl0.5 | – | |
| MISCtl0.4 | – | |
| MISCtl0.3 | – | |
| MISCtl0.2 | – | |
| MISCtl0.1 | SLPBK | 1 = UART loop back testing mode. The pins TXD and RXD are to be connected together externally (with SLPBK =1) and therefore:<br>SLPBK SSEL Mode<br>0 0 normal using Serial_0<br>0 1 normal using Serial_1<br>1 0 Serial_0 TX feeds Serial_1 RX<br>1 1 Serial_1 TX feeds Serial_0 RX |
| MISCtl0.0 | SSEL | Selects either Serial_1 if set =1 or Serial_0 if set = 0 to be connected to RXD and TXD pins. |

#### 1.7.6.1 Serial Interface 0

The Serial Interface 0 can operate in 4 modes:

- **Mode 0**

  Pin RX serves as input and output. TX outputs the shift clock. 8 bits are transmitted with LSB first. The baud rate is fixed at 1/12 of the crystal frequency. Reception is initialized in Mode 0 by setting the flags in S0CON as follows: RI0 = 0 and REN0 = 1. In other modes, a start bit when REN0 = 1 starts receiving serial data.

- **Mode 1**

  Pin RX serves as input, and TX serves as serial output. No external shift clock is used, 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the transmission, 8 data bits are available by reading S0BUF, and stop bit sets the flag RB80 in the Special Function Register S0CON. In mode 1 either internal baud rate generator or timer 1 can be use to specify baud rate.

- **Mode 2**

  This mode is similar to Mode 1, with two differences. The baud rate is fixed at 1/32 or 1/64 of oscillator frequency and 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the serial interface: at transmission, bit TB80 in S0CON is output as the 9th bit, and at receive, the 9th bit affects RB80 in Special Function Register S0CON.

### 1.7.10 Analog Voltage Comparator

The 73S1210F includes a programmable comparator that is connected to the ANA_IN pin. The comparator can be configured to trigger an interrupt if the input voltage rises above or falls below a selectable threshold voltage. The comparator control register should not be modified when the analog interrupt (ANAIEN bit in the INT6Ctl register) is enabled to guard against any false interrupt that might be generated when modifying the threshold. The comparator has a built-in hysteresis to prevent the comparator from repeatedly responding to low-amplitude noise. This hysteresis is approximately 20mV. Interrupt control is handled in the INT6Ctl register.

**Analog Compare Control Register (ACOMP): 0xFFD0 ← 0x00**

**Table 54: The ACOMP Register**

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ANALVL | – | ONCHG | CPOL | CMPEN | TSEL.2 | TSEL.1 | TSEL.0 |

| Bit | Symbol | Function |
|---|---|---|
| ACOMP.7 | ANALVL | When read, indicates whether the input level is above or below the threshold. This is a real time value and is not latched, so it may change from the time of the interrupt trigger until read. |
| ACOMP.6 | – | |
| ACOMP.5 | ONCHG | If set, the Ana_interrupt is invoked on any change above or below the threshold, bit 4 is ignored. |
| ACOMP.4 | CPOL | If set = 1, Ana_interrupt is invoked when signal rises above selected threshold. If set = 0, Ana_interrupt is invoked when signal goes below selected threshold (default). |
| ACOMP.3 | CMPEN | Enables power to the analog comparator. 1 = Enabled. 0 = Disabled (default). |
| ACOMP.2 | TSEL.2 | Sets the voltage threshold for comparison to the voltage on pin ANA_IN. Thresholds are as follows:<br>TSEL.2 TSEL.1 TSEL.0 Voltage Threshold<br>0 0 0 1.00V<br>0 0 1 1.24V<br>0 1 0 1.40V<br>0 1 1 1.50V<br>1 0 0 1.75V<br>1 0 1 2.00V<br>1 1 0 2.30V<br>1 1 1 2.50V |
| ACOMP.1 | TSEL.1 | |
| ACOMP.0 | TSEL.0 | |

### 1.7.11 LED Driver

The 73S1210F provides a single dedicated output pin for driving an LED. The LED driver pin can be configured as a current source that will pull to ground to drive an LED that is connected to VDD without the need for an external current limiting resistor. This pin may be used as general purpose output with the programmed pull-down current and a strong (CMOS) pull-up, if enabled. The analog block must be enabled when this output is being used to drive the selected output current.

This pin may be used as an input with consideration of the programmed output current and level. The register bit when read, indicates the state of the pin.

**LED Control Register (LEDCtl): 0xFFF3 ← 0xFF**

**Table 56: The LEDCtl Register**

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| – | LPUEN | ISET.1 | ISET.0 | – | – | – | LEDD0 |

| Bit | Symbol | Function |
|---|---|---|
| LEDCtl.7 | – | |
| LEDCtl.6 | LPUEN | 0 = Pull-ups are enabled for all of the LED pins. |
| LEDCtl.5 | ISET.1 | These two bits control the drive current (to ground) for the LED driver pin. Current levels are:<br>00 = 0ma(off)<br>01 = 2ma<br>10 = 4ma<br>11 = 10ma |
| LEDCtl.4 | ISET.0 | |
| LEDCtl.3 | – | |
| LEDCtl.2 | – | |
| LEDCtl.1 | – | |
| LEDCtl.0 | LEDD0 | Write data controls output level of pin LED0. Read will report level of pin LED0. |

Figure 11 shows the timing of the I²C read mode:

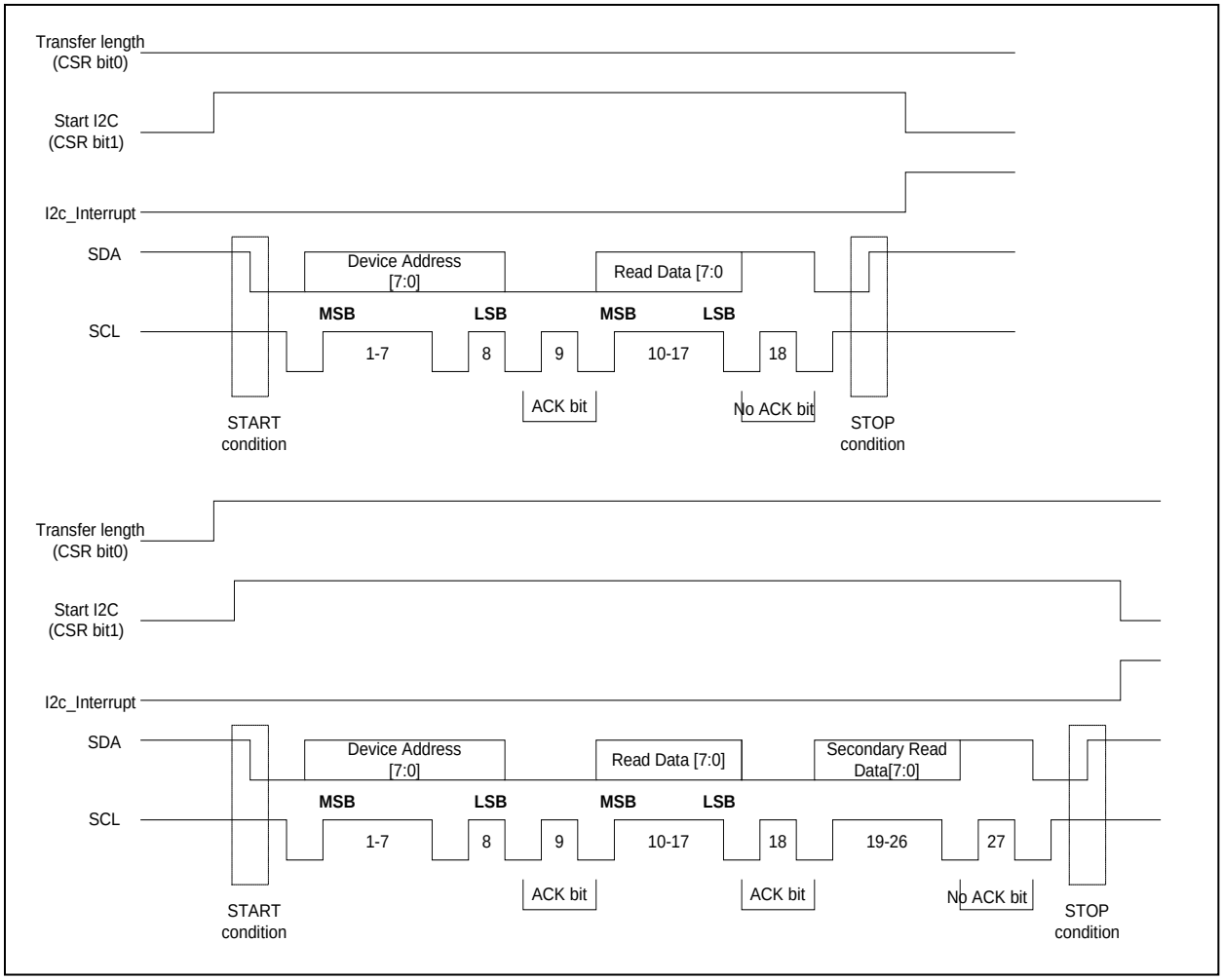



**Figure 11: I²C Read Operation**

### I2C Secondary Read Data Register (SRDR): 0XFF84 ← 0x00

**Table 61: The SRDR Register**

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| SRDR.7 | SRDR.6 | SRDR.5 | SRDR.4 | SRDR.3 | SRDR.2 | SRDR.1 | SRDR.0 |

| Bit | Function |
|---|---|
| SRDR.7 | Second Data byte to be read from the $I^2C$ slave device if bit 0 (I2CLEN) of the Control and Status register (CSR) is set = 1. |
| SRDR.6 | |
| SRDR.5 | |
| SRDR.4 | |
| SRDR.3 | |
| SRDR.2 | |
| SRDR.1 | |
| SRDR.0 | |

### I2C Control and Status Register (CSR): 0xFF85 ← 0x00

**Table 62: The CSR Register**

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | AKERR | I2CST | I2CLEN |

| Bit | Symbol | Function |
|---|---|---|
| CSR.7 | – | |
| CSR.6 | – | |
| CSR.5 | – | |
| CSR.4 | – | |
| CSR.3 | – | |
| CSR.2 | AKERR | Set to 1 if acknowledge bit from Slave Device is not 0. Automatically reset when the new bus transaction is started. |
| CSR.1 | I2CST | Write a 1 to start $I^2C$ transaction. Automatically reset to 0 when the bus transaction is done. This bit should be treated as a “busy” indicator on reading. If it is high, the serial read/write operations are not completed and no new address or data should be written. |
| CSR.0 | I2CLEN | Set to 1 for 2 byte read or write operations. Set to 0 for 1-byte operations. |

on a card insertion / removal to allow power saving modes. Card insertion / removal is generated from the respective card switch detection inputs (whose polarity is programmable).

The built-in ICC Interface has a linear regulator ($V_{CC}$ generator) capable of driving 1.8, 3.0 and 5.0V smart cards in accordance with the ISO 7816-3 and EMV4.1 standards. This converter uses the $V_P$ (5.5V nominal) input supply source. See the power supply management section above for more detail. Auxiliary I/O lines C4 and C8 are only provided for the built-in interface. If support for the auxiliary lines is necessary for the external smart card interface, they need to be handled manually through the USR GPIO pins. The external 73S8010x devices directly connect the I/O (SIO) and clock (SCLK) signals and control is handled via the $I^2C$ interface.

Figure 15 shows how multiple 8010 devices can be connected to the 73S1210F.

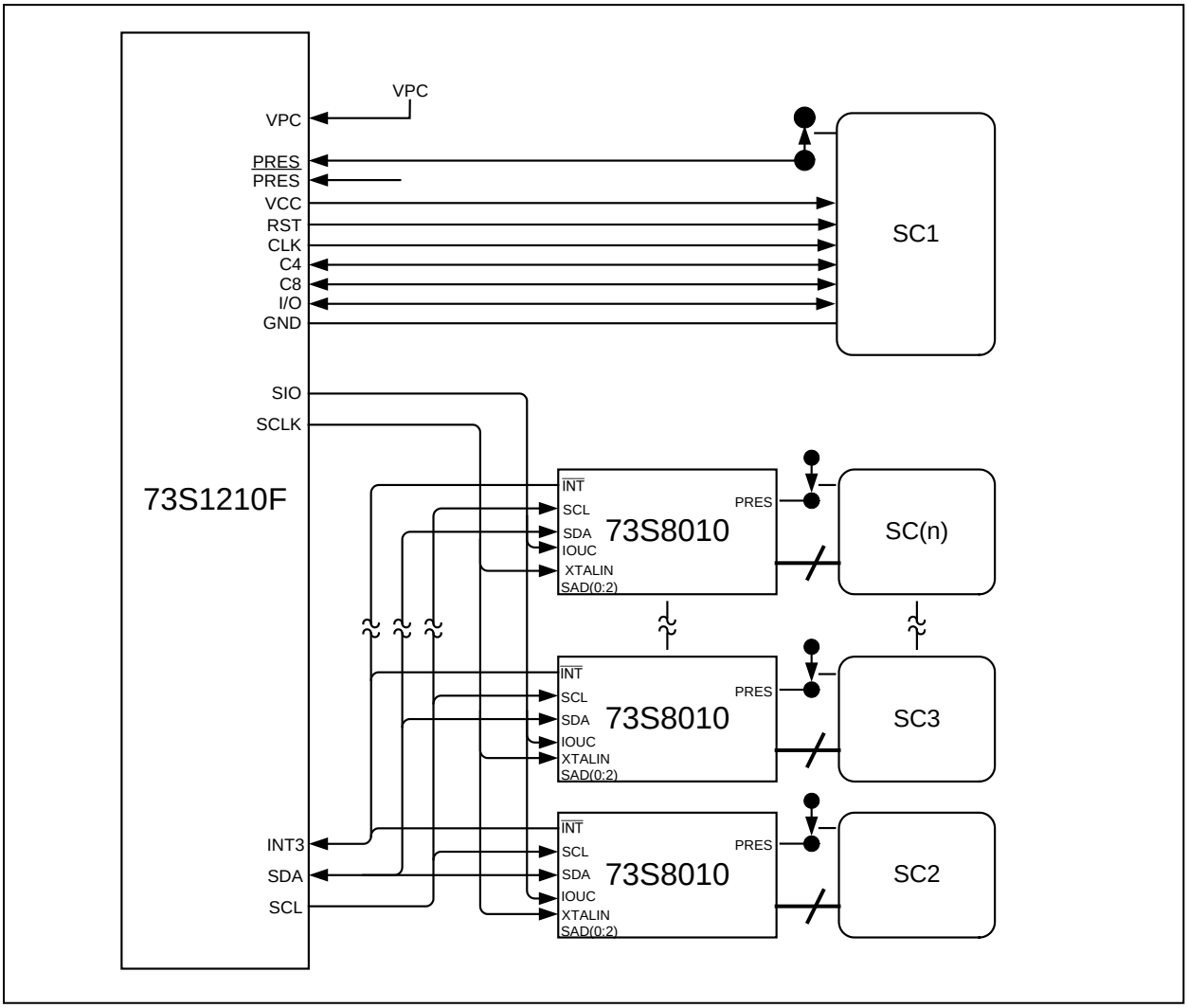



**Figure 15: External Smart Card Interface Block Diagram**

Special Notes Regarding Synchronous Mode Operation

When the SCISYN or SCESNC bits (SPrtcol, bit 7, bit 5, respectively) are set, the selected smart card interface operates in synchronous mode and there are changes in the definition and behavior of pertinent register bits and associated circuitry. The following requirements are to be noted:

1. The source for the smart card clock (CLK or SCLK) is the ETU counter. Only the actively selected interface can have a running synchronous clock. In contrast, an unselected interface may have a running clock in the asynchronous mode of operation.

2. The control bits CLKLVL, SCLKLVL, CLKOFF, and SCLKOFF are functional in synchronous mode. When the CLKOFF bit is set, it will not truncate either the logic low or logic high period when the (stop at) level is of opposite polarity. The CLK/SCLK signal will complete a correct logic low or logic high duty cycle before stopping at the selected level. The CLK "start" is a result of the falling edge of the CLKOFF bit. Setting clock to run when it is stopped low will result in a half period of low before going high. Setting clock to run when it is stopped high will result in the clock going low immediately and then running at the selected rate with 50% duty cycle (within the limitations of the ETU divisor value).

3. The Rlen(7:0) is configured to count the falling edges of the ETU clock (CLK or SCLK) after it has been loaded with a value from 1 to 255. A value of 0 disables the counting function and RLen functions such as I/O source selection (I/O signal bypasses the FIFOs and is controlled by the SCCLK/SCECLK SFRs). When the RLen counter reaches the "max" (loaded) value, it sets the WAITTO interrupt (SCInt, bit 7), which is maskable via WTOIEN (SCIE, bit 7). It must be reloaded in order to start the counting/clocking process again. This allows the processor to select the number of CLK cycles and hence, the number of bits to be read or written to/from the card.

4. The FIFO is not clocked by the first CLK (falling) edge resulting from a CLKOFF de-assertion (a clock start event) when the CLK was stopped in the high state and RLen has been loaded but not yet clocked.

5. The state of the pin IO or SIO is sampled on the rising edge of CLK/SCLK and stored in bit 5 of the SCCtl/SCECtl register.

6. When Rlen = max or 0 and I2CMODE= 1 (STXCtl, b7), the IO or SIO signal is directly controlled by the data and direction bits in the respective SCCtl and SCECtl register. The state of the data in the TX FIFO is bypassed.

7. In the SPrtcol register, bit 6 (MODE9/8B) becomes active. When set, the RXData FIFO will read nine-bit words with the state of the ninth bit being readable in SRXCtl, bit 7 (B9DAT). The RXDAV interrupt will occur when the ninth bit has been clocked in (rising edge of CLK or SCLK).

8. Care must be taken to clear the RX and TX FIFOs at the start of any transaction. The user shall read the RX FIFO until it indicates empty status. Reading the TX FIFO twice will reset the input byte pointer and the next write to the TX FIFO will load the byte to the "first out" position. Note that the bit pointer (serializer/deserializer) is reset to bit 0 on any change of the TX/RXD bit.

Special bits that are only active for sync mode include: SRXCtl, b7 "BIT9DAT", SPrtcol, b6 "MODE9/8B", STXCtl, b7 "I2CMODE", and the definition of SCInt, b7, which was "WAITTO", becomes RLenINT interrupt, and SCIE, b7, which was "WTOIEN", becomes RLenIEN.

### C4/C8 Data Direction Register (SCDIR): 0xFE0C ← 0x00

This register determines the direction of the internal interface C4/C8 lines. After reset, all signals are tri-stated.

**Table 84: The SCDIR Register**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| – | – | – | – | C8D | C4D | – | – |

| Bit | Symbol | Function |
|---|---|---|
| SCDIR.7 | – | |
| SCDIR.6 | – | |
| SCDIR.5 | – | |
| SCDIR.4 | – | |
| SCDIR.3 | C8D | 1 = input, 0 = output. Smart Card C8 direction. |
| SCDIR.2 | C4D | 1 = input, 0 = output. Smart Card C4 direction. |
| SCDIR.1 | – | |
| SCDIR.0 | – | |

**FD Control Register (FDReg): 0xFE13 ← 0x11**

This register uses the transmission factors F and D to set the ETU (baud) rate. The values in this register are mapped to the ISO 7816 conversion factors as described below. The CLK signal for each interface is created by dividing a high-frequency, intermediate signal (MSCLK) by 2. The ETU baud rate is created by dividing MSCLK by 2 times the Fi/Di ratio specified by the codes below. For example, if FI = 0001 and DI = 0001, the ratio of Fi/Di is 372/1. Thus the ETU divider is configured to divide by 2 * 372 = 744. The maximum supported F/D ratio is 4096.

**Table 90: The FDReg Register**

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FVAL.3 | FVAL.2 | FVAL.1 | FVAL.0 | DVAL.3 | DVAL.2 | DVAL.1 | DVAL.0 |

**Table 91: The FDReg Bit Functions**

| Bit | Symbol | Function |
|---|---|---|
| FDReg.7 | FVAL.3 | Refer to the Table 93 above. This value is converted per the table to set the divide ratio used to generate the baud rate (ETU). Default, also used for ATR, is 0001 (Fi = 372). This value is used by the selected interface. |
| FDReg.6 | FVAL.2 | |
| FDReg.5 | FVAL.1 | |
| FDReg.4 | FVAL.0 | |
| FDReg.3 | DVAL.3 | Refer to Table 93 above. This value is used to set the divide ratio used to generate the smart card CLK. Default, also used for ATR, is 0001 (Di = 1). |
| FDReg.2 | DVAL.2 | |
| FDReg.1 | DVAL.1 | |
| FDReg.0 | DVAL.0 | |

**Table 92: Divider Ratios Provided by the ETU Counter**

| FI (code) | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 |
|---|---|---|---|---|---|---|---|---|
| Fi (ratio) | 372 | 372 | 558 | 744 | 1116 | 1488 | 1860 | 1860⊕ |
| FCLK max | 4 | 5 | 6 | 8 | 12 | 16 | 20 | 20⊕ |

| FI(code) | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|---|---|---|---|---|---|---|---|---|
| Fi(ratio) | 512⊕ | 512 | 768 | 1024 | 1536 | 2048 | 2048⊕ | 2048⊕ |
| FCLK max | 5⊕ | 5 | 7.5 | 10 | 15 | 20 | 20⊕ | 20⊕ |

| DI(code) | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 |
|---|---|---|---|---|---|---|---|---|
| Di(ratio) | 1⊕ | 1 | 2 | 4 | 8 | 16 | 32 | 32⊕ |

| DI(code) | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|---|---|---|---|---|---|---|---|---|
| Di(ratio) | 12 | 20 | 16⊕ | 16⊕ | 16⊕ | 16⊕ | 16⊕ | 16⊕ |

Note: values marked with ⊕ are not included in the ISO definition and arbitrary values have been assigned.

The values given below are used by the ETU divider to create the ETU clock. The entries that are not shaded will result in precise CLK/ETU per ISO requirements. Shaded areas are not precise but are within 1% of the target value.

**ATR Timeout Registers (ATRLsB): 0xFE20 ← 0x00, (ATRMsB): 0xFE1F ← 0x00**

These registers form the ATR timeout (ATRTO [15:0]) parameter. Time in ETU between the leading edge of the first character and leading edge of the last character of the ATR response. Timer is enabled when the RCVATR is set and starts when leading edge of the first start bit is received and disabled when the RCVATR is cleared. An ATR timeout is generated if this time is exceeded.

**Table 103: The ATRLsB Register**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| ATRTO.7 | ATRTO.6 | ATRTO.5 | ATRTO.4 | ATRTO.3 | ATRTO.1 | ATRTO.2 | ATRTO.0 |

**Table 104: The ATRMsB Register**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| ATRTO.15 | ATRTO.14 | ATRTO.13 | ATRTO.12 | ATRTO.11 | ATRTO.10 | ATRTO.9 | ATRTO.8 |

**TS Timeout Register (STSTO): 0xFE21 ← 0x00**

The TS timeout is the time in ETU between the de-assertion of smart card reset and the leading edge of the TS character in the ATR (when DETTS is set). The timer is started when smart card reset is de-asserted. An ATR timeout is generated if this time is exceeded (MUTE card).

**Table 105: The STSTO Register**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| TST0.7 | TST0.6 | TST0.5 | TST0.4 | TST0.3 | TST0.1 | TST0.2 | TST0.0 |

**Reset Time Register (RLength): 0xFE22 ← 0x70**

Time in ETUs that the hardware delays the de-assertion of RST. If set to 0 and RSTCRD = 0, the hardware adds no extra delay and the hardware will release RST after VCCOK is asserted during power-up. If set to 1, it will delay the release of RST by the time in this register. When the firmware sets the RSTCRD bit, the hardware will assert reset (RST = 0 on pin). When firmware clears the bit, the hardware will release RST after the delay specified in Rlen. If firmware sets the RSTCRD bit prior to instructing the power to be applied to the smart card, the hardware will not release RST after power-up until RLen after the firmware clears the RSTCRD bit. This provides a means to power up the smart card and hold it in reset until the firmware wants to release the RST to the selected smart card. Works with the selected smart card interface.

**Table 106: The RLength Register**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| RLen.7 | RLen.6 | RLen.5 | RLen.4 | RLen.3 | RLen.1 | RLen.2 | RLen.0 |

Shaded locations indicate functions that are not provided in the synchronous mode.

**Table 107: Smart Card SFR Table**

| Name | Address | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| SCSel | FE00 | | | | | SelSC(1:0) | | BYPASS | |
| SCInt | FE01 | WAITTO/ RLIEN | CRDEVT | VCCTMR | RXDAVl | TXEVNT | TXSENT | TXERR | RXERR |
| SCIE | FE02 | WTOI/ RLIEN | CDEVNT | VTMREN | RXDAEN | TXEVEN | TXSNTEN | TXERR | RXERR |
| VccCtl | FE03 | VCCSEL.1 | VCCSEL.0 | VDDFLT | RDYST | VCCOK | | | SCPWRDN |
| VCCTmr | FE04 | OFFTMR(3:0) | | | | VCCTMR(3:0) | | | |
| CRDCtl | FE05 | DEBOUN | CDETEN | | | DETPOL | PUENB | PDEN | CARDIN |
| STXCtl | FE06 | I2CMODE | | TXFULL | TXEMTY | TXUNDR | LASTTX | TX/RXB | BREAKD |
| STXData | FE07 | TXDATA(7:0) | | | | | | | |
| SRXCtl | FE08 | BIT9DAT | | LASTRX | CRCERR | RXFULL | RXEMTY | RXOVRR | PARITYE |
| SRXData | FE09 | RXDATA(7:0) | | | | | | | |
| SCCtl | FE0A | RSTCRD | | IO | IOD | C8 | C4 | CLKLVL | CLKOFF |
| SCECtl | FE0B | | | SIO | SIOD | | | SCLKLVL | SCLKOFF |
| SCDIR | FE0C | | | | | C8D | C4D | | |
| SPrtcol | FE0D | SCISYN | MOD9/8B | SCESYN | 0 | TMODE | CRCEN | CRCMS | RCVATR |
| SCCLK | FE0F | | | ICLKFS(5:0) | | | | | |
| SCECLK | FE10 | | | ECLKFS(5:0) | | | | | |
| SParCtl | FE11 | | DISPAR | BRKGEN | BRKDET | RTRAN | DISCRX | INSPE | FORCPE |
| SByteCtl | FE12 | | DETTS | DIRTS | BRKDUR (1:0) | | | | |
| FDReg | FE13 | FVAL(3:0) | | | | DVAL (3:0) | | | |
| CRCMsB | FE14 | CRC(15:8) | | | | | | | |
| CRCLsB | FE15 | CRC(7:0) | | | | | | | |
| BGT | FE16 | EGT8 | | | | BGT(4:0) | | | |
| EGT | FE17 | EGT(7:0) | | | | | | | |
| BWTB3 | FE18 | | | | | BWT(27:24) | | | |
| BWTB2 | FE19 | BWT(23:16) | | | | | | | |
| BWTB1 | FE1A | BWT(15:8) | | | | | | | |
| BWTB0 | FE1B | BWT(7:0) | | | | | | | |
| CWTB1 | FE1C | CWT(15:8) | | | | | | | |
| CWTB0 | FE1D | CWT(7:0) | | | | | | | |
| ATRMsB | FE1F | ATRTO(15:8) | | | | | | | |
| ATRLsB | FE20 | ATRTO(7:0) | | | | | | | |
| STSTO | FE21 | TSTO(7:0) | | | | | | | |
| RLength | FE22 | RLen(7:0) | | | | | | | |

## 3.3 Digital IO Characteristics

These requirements pertain to digital I/O pin types with consideration of the specific pin function and configuration. The LED(1:0) pins have pull-ups that may be enabled. The Row pins have 100kΩ pull-ups.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Voh | Output level, high | Ioh = -2mA | 0.8 * $V_{DD}$ | | $V_{DD}$ | V |
| | | OFF_REQ pin - $I_{OH}$ = -1mA | $V_{DD}$ - 0.45 | | | V |
| Vol | Output level, low | Iol = 2mA | 0 | | 0.3 | V |
| | | OFF_REQ pin - Iol = 2mA | | | 0.45 | V |
| Vih | Input voltage, high | 2.7v < VDD <3.6v | 1.8 | | $V_{DD}$ +0.3 | V |
| Vil | Input voltage, low | 2.7v < VDD <3.6v | -0.3 | | 0.6 | V |
| | | RESET, ON_OFF,PRES pins | -0.3 | | 0.8 | V |
| Ileak | Leakage current | 0 < Vin < VDD<br>All output modes disabled, pull-up/downs disabled | -5 | | 5 | µA |
| Ipu | Pull-up current | If provided and enabled,<br>Vout < 0.1v | -5 | | | µA |
| Ipd | Pull-down current | If provided and enabled,<br>Vout > VDD – 0.1v | | | 5 | µA |

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Iled | LED drive current | Vout = 1.3V,<br>2.7v < VDD < 3.6v | | 2<br>4<br>10 | | mA |
| Iolkrow | Keypad row output low current | 0.0v < Voh < 0.1v<br>when pull-up R is enabled | | 40 | 100 | µA |
| Iolkcol | Keypad column output high current | 0.0v < Voh < 0.1v<br>when col. is pulled low | | 1.5 | 3 | mA |

| | | | | | | |
|---|---|---|---|---|---|---|
| $I_{DD\_IN}$ | Supply Current – pins 28 + 40 (internal consumption – digital core) | CPU clock @ 24MHz | | 29 | 33.5 | mA |
| | | CPU clock @ 12MHz | | 21 | 24 | mA |
| | | CPU clock @ 6MHz | | 15.5 | 18 | mA |
| | | CPU clock @ 3.69MHz | | 13.5 | 15.5 | mA |
| | | Power down (-40° to 85°C) | | 8 | 50 | µA |
| | | Power down (25°C) | | 6 | 15 | µA |
| $I_{DD\_OUT}$ | Supply Current – pin 68 (available to external circuitry) | Circuit ON | | | 20 | mA |
| $I_{VBUS}$ | Supply Current from $V_{BUS}$ | $V_{CC}$ off, $I_{DDINTERNAL}$ < 20µA | | 0.2 | 0.4 | mA |
| $I_{VBAT}$ $I_{VPC}$ | Supply Current from $V_{BAT}$ or $V_{PC}$ | Circuit OFF | | 0.01 | 1 | µA |
| $VBUS_{ON}$ | $V_{BUS}$ detection threshold | | | 3.5 | | V |
| $VBUS_{IDIS}$ | $V_{BUS}$ discharge current | | | 50 | | µA |
| | | | | | | |
| **External Capacitor Values** | | | | | | |
| $C_{VPC}$ | External filter capacitor for $V_{PC}$ | | 8.0 | 10.0 | 12.0 | µF |
| $C_{VP}$ | External filter capacitor for $V_P$ | | 2.0 | 4.7 | 10.0 | µF |
| $C_{VDD}$* | External filter capacitors for $V_{DD}$ | | 0.2 | | 1.0 | µF |
| $C_{VCC}$ | External filter capacitor for $V_{CC}$ | $C_{VCC}$ should be ceramic with low ESR (<100MΩ). | 0.2 | 0.47 | 1.0 | µF |

*Note: Recommend on 0.1µF for each $V_{DD}$ pin.

## 3.8 Current Fault Detection Circuits

| Symbol | Parameter | Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $IV_{Pmax}$ | $V_P$ over current fault | | | | 150 | mA |
| $I_{DDmax}$ | VDD over-current limit | | 40 | | 100 | mA |
| $I_{CCF}$ | Card overcurrent fault | | 80 | | 150 | mA |
| $I_{CCF1P8}$ | Card overcurrent fault | $V_{CC}$ = 1.8V | 60 | | 130 | mA |

# 6 Packaging Information

## 6.1 68-Pin QFN Package Outline

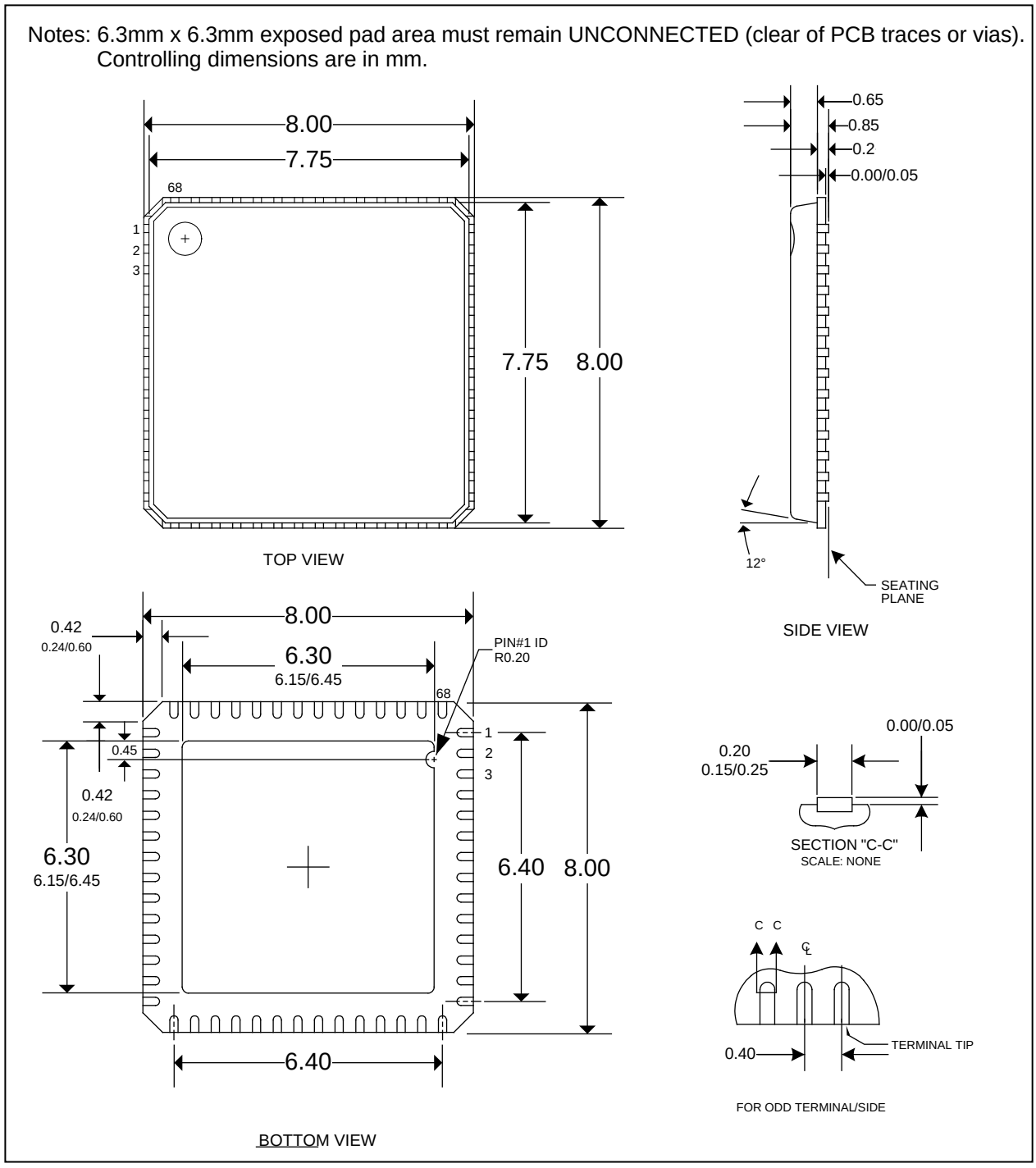



**Figure 46: 73S1210F 68 QFN Mechanical Drawing**