Analog Devices Inc./Maxim Integrated - 73S1210F-44IMR/F Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80515
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SmartCard, UART/USART
Peripherals	LED, POR, WDT
Number of I/O	8
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/73s1210f-44imr-f

FEATURES

80515 Core:

- 1 clock cycle per instruction (most instructions)
- CPU clocked up to 24MHz
- 32KB Flash memory (lockable)
- 2kB XRAM (User Data Memory)
- 256 byte IRAM
- Hardware watchdog timer

Oscillators:

- Single low-cost 6MHz to 12MHz crystal
- An Internal PLL provides all the necessary clocks to each block of the system

Interrupts:

- Standard 80C515 4-priority level structure
- 9 different sources of interrupt to the core

Power Down Modes:

- 2 standard 80C515 Power Down and IDLE modes
- Sub-μA OFF mode
- ON/OFF Main System Power Switch:
- Input for an SPST momentary switch to ground

Timers:

- (2) Standard 80C52 timers T0 and T1
- (1) 16-bit timer

Built-in ISO-7816 Card Interface:

- Linear regulator produces VCC for the card (1.8V, 3V or 5V)
- Full compliance with EMV 4.1
- Activation/Deactivation sequencers
- Auxiliary I/O lines (C4 and C8 signals)
- 7kV ESD protection on all interface pins

Communication with Smart Cards:

- ISO 7816 UART 9600 to 115kbps for T=0, T=1
- (2) 2-Byte FIFOs for transmit and receive
- Configured to drive multiple external Teridian 73S8010x interfaces (for multi-SAM architectures)

Voltage Detection:

- Analog Input (detection range: 1.0V to 2.5V)

Communication Interfaces:

- Full-duplex serial interface (1200 to 115kbps UART)
- I^2C Master Interface (400kbps)
- Man-Machine Interface and I/Os:
- 6x5 Keyboard (hardware scanning, debouncing and scrambling)
- (8) User I/Os
- Single programmable current output (LED)
- Operating Voltage:
- Single supply 2.7V to 6.5V operation (VPC)
- 5V supply (VBUS 4.4V to 5.5V) with or without battery back up operation (VBAT 4.0V to 6.5V)
- Automated detection of voltage presence - Priority on VBUS over VBAT

DC-DC Converter:

- Requires a single 10μH Inductor
- 3.3V / 20mA supply available for external circuits

Operating Temperature:

- -40°C to 85°C

Package:

- 68-pin QFN, 44 pin QFN

Turnkey Firmware:

- Compliant with PC/SC, ISO7816 and EMV4.1 specifications
- Features a Power Down mode accessible from the host
- Supports Plug & Play over serial interface
- Windows® XP driver available (*)
- Windows CE / Mobile driver available (*)
- Linux and other OS: Upon request
- Or for custom developments:
  - A complete set of ISO-7816, EMV4.1 and low-level libraries are available for T=0 / T=1
  - Two-level Application Programming Interface (ANSI C-language libraries)

(*) Contact Teridian Semiconductor for conditions and availability.

Program Status Word (PSW):

Table 9: PSW Register

MSB							LSB
CV	AC	F0	RS1	RS	OV	–	P

Bit	Symbol	Function
PSW.7	CV	Carry flag.
PSW.6	AC	Auxiliary Carry flag for BCD operations.
PSW.5	F0	General purpose Flag 0 available for user.
PSW.4	RS1	Register bank select control bits. The contents of RS1 and RS0 select the working register bank:
PSW.3	RS0	
PSW.2	OV	Overflow flag.
PSW.1	F1	General purpose Flag 1 available for user.
PSW.0	P	Parity flag, affected by hardware to indicate odd / even number of “one” bits in the Accumulator, i.e. even parity.

RS1/RS0	Bank Selected	Location
00	Bank 0	(0x00 – 0x07)
01	Bank 1	(0x08 – 0x0F)
10	Bank 2	(0x10 – 0x17)
11	Bank 3	(0x18 – 0x1F)

Stack Pointer: The stack pointer (SP) is a 1-byte register initialized to 0x07 after reset. This register is incremented before PUSH and CALL instructions, causing the stack to begin at location 0x08.

Data Pointer: The data pointer (DPTR) is 2 bytes wide. The lower part is DPL, and the highest is DPH. It can be loaded as a 2-byte register (MOV DPTR,#data16) or as two registers (e.g. MOV DPL,#data8). It is generally used to access external code or data space (e.g. MOVC A,@A+DPTR or MOVX A,@DPTR respectively).

Program Counter: The program counter (PC) is 2 bytes wide initialized to 0x0000 after reset. This register is incremented during the fetching operation code or when operating on data from program memory. Note: The program counter is not mapped to the SFR area.

Port Registers: The I/O ports are controlled by Special Function Register USR70. The contents of the SFR can be observed on corresponding pins on the chip. Writing a 1 to any of the ports (see Table 10) causes the corresponding pin to be at high level (3.3V), and writing a 0 causes the corresponding pin to be held at low level (GND). The data direction register UDIR70 define individual pins as input or output pins (see the User (USR) Ports section for details).

Table 10: Port Registers

Register	SFR Address	R/W	Description
USR70	0x90	R/W	Register for User port bit 7:0 read and write operations (pins USR0… USR7).
UDIR70	0x91	R/W	Data direction register for User port bits 0:7. Setting a bit to 0 means that the corresponding pin is an output.

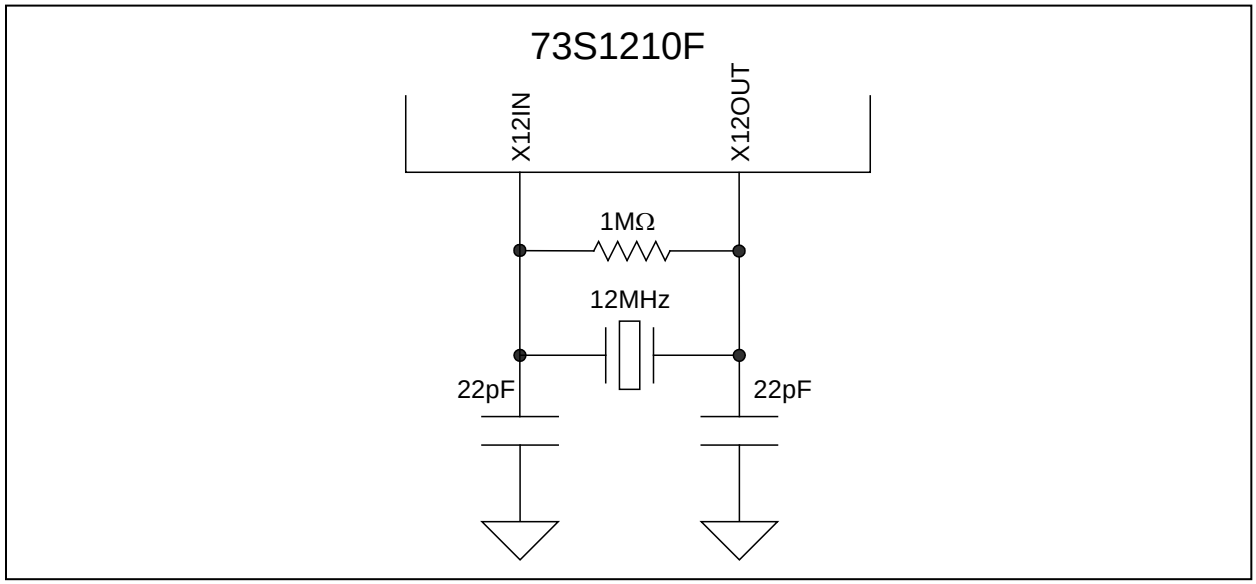
MPU Clock Control Register (MPUCKCtl): 0xFFA1 ← 0x0C

Table 13: The TCON Register

MSB							LSB
–	–	MDIV.5	MDIV.4	MDIV.3	MDIV.2	MDIV.1	MDIV.0

Bit	Symbol	Function
MPUCKCtl.7	–	
MPUCKCtl.6	–	
MPUCKCtl.5	MDIV.5	This value determines the ratio of the MPU master clock frequency to the VCO frequency (MCLK) such that MPUClk = MCLK/(2 * (MPUCKDiv(5:0) + 1)). Do not use values of 0 or 1 for MPUCKDiv(n). Default is 0Ch to set CPCLK = 3.6923MHz.
MPUCKCtl.4	MDIV.4	
MPUCKCtl.3	MDIV.3	
MPUCKCtl.2	MDIV.2	
MPUCKCtl.1	MDIV.1	
MPUCKCtl.0	MDIV.0	

The oscillator circuits are designed to connect directly to standard parallel resonant crystal in a Pierce oscillator configuration. Each side of the crystal should include a 22pF capacitor to ground for both oscillator circuits and a 1MΩ resistor is required across the 12MHz crystal.



Note: The crystal should be placed as close as possible to the IC, and vias should be avoided.

Figure 4: Oscillator Circuit

External Interrupt Control Register (INT5Ctl): 0xFF94 ← 0x00

Table 14: The INT5Ctl Register

MSB							LSB
PDMUX	–	–	–	–	–	KPIEN	KPINT

Bit	Symbol	Function
INT5Ctl.7	PDMUX	When set = 1, enables interrupts from Keypad (normally going to int5), Smart Card interrupts (normally going to int4), or USR(7:0) pins (int0) to cause interrupt on int0. The assertion of the interrupt to int0 is delayed by 512 MPU clocks to allow the analog circuits, including the clock system, to stabilize. This bit must be set prior to asserting the PWRDN bit in order to properly configure the interrupts that will wake up the circuit. This bit is reset = 0 when this register is read.
INT5Ctl.6	–	
INT5Ctl.5	–	
INT5Ctl.4	–	
INT5Ctl.3	–	
INT5Ctl.2	–	
INT5Ctl.1	KPIEN	Keypad interrupt enable.
INT5Ctl.0	KPINT	Keypad interrupt flag.

Miscellaneous Control Register 0 (MISCtl0): 0xFFF1 ← 0x00

Table 15: The MISCtl0 Register

MSB							LSB
PWRDN	–	–	–	–	–	SLPBK	SSEL

Bit	Symbol	Function
MISCtl0.7	PWRDN	This bit sets the circuit into a low-power condition. All analog (high-speed oscillator and VCO/PLL) functions are disabled 32 MPU clock cycles after this bit is set = 1. This allows time for the next instruction to set the STOP bit in the PCON register to stop the CPU core. The MPU is not operative in this mode. When set, this bit overrides the individual control bits that otherwise control power consumption.
MISCtl0.6	–	
MISCtl0.5	–	
MISCtl0.4	–	
MISCtl0.3	–	
MISCtl0.2	–	
MISCtl0.1	SLPBK	UART loop back testing mode.
MISCtl0.0	SSEL	Serial port pins select.

Miscellaneous Control Register 1 (MISCtl1): 0xFFF2 ← 0x10

Table 16: The MISCtl1 Register

MSB							LSB
–	–	FRPEN	FLSH66	–	–	–	–

Bit	Symbol	Function
MISCtl1.7	–	
MISCtl1.6	–	
MISCtl1.5	FRPEN	Flash Read Pulse enable (low). If FRPEN = 1, the Flash Read signal is passed through with no change. When FRPEN = 0 a one-shot circuit that shortens the Flash Read signal is enabled to save power. The Flash Read pulse will shorten to 40 or 66ns (approximate based on the setting of the FLSH66 bit) in duration, regardless of the MPU clock rate. For MPU clock frequencies greater than 10MHz, this bit should be set high.
MISCtl1.4	FLSH66	When high, creates a 66ns Flash read pulse, otherwise creates a 40ns read pulse when FRPEN is set.
MISCtl1.3	–	
MISCtl1.2	–	
MISCtl1.1	–	
MISCtl1.0	–	

Master Clock Control Register (MCLKCtl): 0x8F ← 0x0A

Table 17: The MCLKCtl Register

MSB							LSB
HSOEN	KBEN	SCEN	–	–	MCT.2	MCT.1	MCT.0

Bit	Symbol	Function
MCLKCtl.7	HSOEN*	High-speed oscillator enable. When set = 1, disables the high-speed crystal oscillator and VCO/PLL system. This bit is not changed when the PWRDN bit is set but the oscillator/VCO/PLL is disabled.
MCLKCtl.6	KBEN	1 = Disable the keypad logic clock. This bit is not changed in PWRDN mode but the function is disabled.
MCLKCtl.5	SCEN	1 = Disable the smart card logic clock. This bit is not changed in PWRDN mode but the function is disabled. Interrupt logic for card insertion/removal remains operable even with smart card clock disabled.
MCLKCtl.4	–	
MCLKCtl.3	–	
MCLKCtl.2	MCT.2	This value determines the ratio of the VCO frequency (MCLK) to the high-speed crystal oscillator frequency such that: MCLK = (MCount*2 + 4)*Fxtal. The default value is MCount = 2h such that MCLK = (2*2 + 4)*12.00MHz = 96MHz.
MCLKCtl.1	MCT.1	
MCLKCtl.0	MCT.0	

*Note: The HSOEN bit should never be set under normal circumstances. Power down control should only be initiated via use of the PWRDN bit in MISCtl0.

Interrupt Enable 1 Register (IEN1): 0xB8 ← 0x00

Table 20: The IEN1 Register

MSB							LSB
–	SWDT	EX6	EX5	EX4	EX3	EX2	–

Bit	Symbol	Function
IEN1.7	–	
IEN1.6	SWDT	Not used for interrupt control.
IEN1.5	EX6	EX6 = 0 – disable external interrupt 6.
IEN1.4	EX5	EX5 = 0 – disable external interrupt 5.
IEN1.3	EX4	EX4 = 0 – disable external interrupt 4.
IEN1.2	EX3	EX3 = 0 – disable external interrupt 3.
IEN1.1	EX2	EX2 = 0 – disable external interrupt 2.
IEN1.0	–	

Interrupt Enable 2 Register (IEN2): 0x9A ← 0x00

Table 21: The IEN2 Register

MSB							LSB
–	–	–	–	–	–	–	ES1

Bit	Symbol	Function
IEN2.0	ES1	ES1 = 0 – disable serial channel interrupt.

1.7.6 UART

The 80515 core of the 73S1210F includes two separate UARTs that can be programmed to communicate with a host. The 73S1210F can only connect one UART at a time since there is only one set of TX and Rx pins. The MISCtl0 register is used to select which UART is connected to the TX and RX pins. Each UART has a different set of operating modes that the user can select according to their needs. The UART is a dedicated 2-wire serial interface, which can communicate with an external host processor at up to 115,200 bits/s. The TX and RX pins operate at the V_{DD} supply voltage levels and should never exceed 3.6V. The operation of each pin is as follows:

RX: Serial input data is applied at this pin. Conforming to RS-232 standard, the bytes are input LSB first. The voltage applied at RX must not exceed 3.6V.

TX: This pin is used to output the serial data. The bytes are output LSB first.

The 73S1210F has several UART-related read/write registers. All UART transfers are programmable for parity enable, parity select, 2 stop bits/1 stop bit and XON/XOFF options for variable communication baud rates from 300 to 115200 bps. Table 33 shows the selectable UART operation modes and Table 34 shows how the baud rates are calculated.

Table 33: UART Modes

	UART 0	UART 1
Mode 0	N/A	Start bit, 8 data bits, parity, stop bit, variable baud rate (internal baud rate generator).
Mode 1	Start bit, 8 data bits, stop bit, variable baud rate (internal baud rate generator or timer 1).	Start bit, 8 data bits, stop bit, variable baud rate (internal baud rate generator).
Mode 2	Start bit, 8 data bits, parity, stop bit, fixed baud rate 1/32 or 1/64 of $f_{CKMPU.}$	N/A
Mode 3	Start bit, 8 data bits, parity, stop bit, variable baud rate (internal baud rate generator or timer 1).	N/A

Note: Parity of serial data is available through the P flag of the accumulator. Seven-bit serial modes with parity, such as those used by the FLAG protocol, can be simulated by setting and reading bit 7 of 8-bit output data. Seven-bit serial modes without parity can be simulated by setting bit 7 to a constant 1. 8-bit serial modes with parity can be simulated by setting and reading the 9th bit, using the control bits S0CON3 and S1CON3 in the S0COn and S1CON SFRs.

Table 34: Baud Rate Generation

	Using Timer 1	Using Internal Baud Rate Generator
Serial Interface 0	$2^{smod} * f_{CKMPU}/ (384 * (256-TH1))$	$2^{smod} * f_{CKMPU}/(64 * (2^{10}-S0REL))$
Serial Interface 1	N/A	$f_{CKMPU}/(32 * (2^{10}-S1REL))$

Note: S0REL (9:0) and S1REL (9:0) are 10-bit values derived by combining bits from the respective timer reload registers SxRELH (bits 1:0) and SxRELL (bits 7:0). TH1 is the high byte of timer 1. The SMOD bit is located in the PCON SFR.

- **Mode 3**
  The only difference between Mode 2 and Mode 3 is that in Mode 3 either internal baud rate generator or timer 1 can be use to specify baud rate.

The S0BUF register is used to read/write data to/from the serial 0 interface.

Serial Interface 0 Control Register (S0CON): 0x9B ← 0x00

Transmit and receive data are transferred via this register.

Table 38: The S0CON Register

MSB LSB

SM0	SM1	SM20	REN0	TB80	RB80	TI0	RI0

Bit	Symbol	Function
S0CON.7	SM0	These two bits set the UART0 mode:
S0CON.6	SM1	
S0CON.5	SM20	Enables the inter-processor communication feature.
S0CON.4	REN0	If set, enables serial reception. Cleared by software to disable reception.
S0CON.3	TB80	The 9th transmitted data bit in Modes 2 and 3. Set or cleared by the MPU, depending on the function it performs (parity check, multiprocessor communication etc.).
S0CON.2	RB80	In Modes 2 and 3 it is the 9th data bit received. In Mode 1, if SM20 is 0, RB80 is the stop bit. In Mode 0 this bit is not used. Must be cleared by software.
S0CON.1	TI0	Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software.
S0CON.0	RI0	Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software.

Mode	Description	SM0	SM1
0	N/A	0	0
1	8-bit UART	0	1
2	9-bit UART	1	0
3	9-bit UART	1	1

Mode 0

Putting either timer/counter into mode 0 configures it as an 8-bit timer/counter with a divide-by-32 prescaler. In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1's to all 0's, it sets the timer overflow flag TF0. The overflow flag TF0 then can be used to request an interrupt. The counted input is enabled to the timer when TRx = 1 and either GATE = 0 or TX = 1 (setting GATE = 1 allows the timer to be controlled by external input TX, to facilitate pulse width measurements). TRx are control bits in the special function register TCON; GATE is in TMOD. The 13-bit register consists of all 8 bits of TH1 and the lower 5 bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Setting the run flag (TRx) does not clear the registers. Mode 0 operation is the same for timer 0 as for timer 1.

Mode 1

Mode 1 is the same as mode 0, except that the timer register is run with all 16 bits.

Mode 2

Mode 2 configures the timer register as an 8-bit counter (TLx) with automatic reload. The overflow from TLx not only sets TFx, but also reloads TLx with the contents of THx, which is preset by software. The reload leaves THx unchanged.

Mode 3

Mode 3 has different effects on timer 0 and timer 1. Timer 1 in mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in mode 3 establishes TL0 and TH0 as two separate counters. TL0 uses the timer 0 control bits: C/T, GATE, TR0, INT0, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from timer 1. Thus, TH0 now controls the "timer 1" interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer or counter. When timer 0 is in mode 3, timer 1 can be turned on and off by switching it out of and into its own mode 3, or can still be used by the serial channel as a baud rate generator, or in fact, in any application not requiring an interrupt from timer 1 itself.

Timer/Counter Control Register (TCON): 0x88 ← 0x00

Table 42: The TCON Register

MSB LSB

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Bit	Symbol	Function
TCON.7	TF1	Timer 1 overflow flag.
TCON.6	TR1	Not used for interrupt control.
TCON.5	TF0	Timer 0 overflow flag.
TCON.4	TR0	Not used for interrupt control.
TCON.3	IE1	Interrupt 1 edge flag is set by hardware when the falling edge on external interrupt int1 is observed. Cleared when an interrupt is processed.
TCON.2	IT1	Interrupt 1 type control bit. 1 selects falling edge and 0 selects low level for input pin to cause an interrupt.
TCON.1	IE0	Interrupt 0 edge flag is set by hardware when the falling edge on external interrupt int0 is observed. Cleared when an interrupt is processed.
TCON.0	IT0	Interrupt 0 type control bit. 1 selects falling edge and 0 sets low level for input pin to cause interrupt.

1.7.10 Analog Voltage Comparator

The 73S1210F includes a programmable comparator that is connected to the ANA_IN pin. The comparator can be configured to trigger an interrupt if the input voltage rises above or falls below a selectable threshold voltage. The comparator control register should not be modified when the analog interrupt (ANAIEN bit in the INT6Ctl register) is enabled to guard against any false interrupt that might be generated when modifying the threshold. The comparator has a built-in hysteresis to prevent the comparator from repeatedly responding to low-amplitude noise. This hysteresis is approximately 20mV. Interrupt control is handled in the INT6Ctl register.

Analog Compare Control Register (ACOMP): 0xFFD0 ← 0x00

Table 54: The ACOMP Register

MSB LSB

ANALVL	–	ONCHG	CPOL	CMPEN	TSEL.2	TSEL.1	TSEL.0

Bit	Symbol	Function
ACOMP.7	ANALVL	When read, indicates whether the input level is above or below the threshold. This is a real time value and is not latched, so it may change from the time of the interrupt trigger until read.
ACOMP.6	–	
ACOMP.5	ONCHG	If set, the Ana_interrupt is invoked on any change above or below the threshold, bit 4 is ignored.
ACOMP.4	CPOL	If set = 1, Ana_interrupt is invoked when signal rises above selected threshold. If set = 0, Ana_interrupt is invoked when signal goes below selected threshold (default).
ACOMP.3	CMPEN	Enables power to the analog comparator. 1 = Enabled. 0 = Disabled (default).
ACOMP.2	TSEL.2	Sets the voltage threshold for comparison to the voltage on pin ANA_IN. Thresholds are as follows: TSEL.2 TSEL.1 TSEL.0 Voltage Threshold 0 0 0 1.00V 0 0 1 1.24V 0 1 0 1.40V 0 1 1 1.50V 1 0 0 1.75V 1 0 1 2.00V 1 1 0 2.30V 1 1 1 2.50V
ACOMP.1	TSEL.1	
ACOMP.0	TSEL.0	

I2C Secondary Read Data Register (SRDR): 0XFF84 ← 0x00

Table 61: The SRDR Register

MSB LSB

SRDR.7	SRDR.6	SRDR.5	SRDR.4	SRDR.3	SRDR.2	SRDR.1	SRDR.0

Bit	Function
SRDR.7	Second Data byte to be read from the I^2C slave device if bit 0 (I2CLEN) of the Control and Status register (CSR) is set = 1.
SRDR.6	
SRDR.5	
SRDR.4	
SRDR.3	
SRDR.2	
SRDR.1	
SRDR.0	

I2C Control and Status Register (CSR): 0xFF85 ← 0x00

Table 62: The CSR Register

MSB LSB

–	–	–	–	–	AKERR	I2CST	I2CLEN

Bit	Symbol	Function
CSR.7	–	
CSR.6	–	
CSR.5	–	
CSR.4	–	
CSR.3	–	
CSR.2	AKERR	Set to 1 if acknowledge bit from Slave Device is not 0. Automatically reset when the new bus transaction is started.
CSR.1	I2CST	Write a 1 to start I^2C transaction. Automatically reset to 0 when the bus transaction is done. This bit should be treated as a “busy” indicator on reading. If it is high, the serial read/write operations are not completed and no new address or data should be written.
CSR.0	I2CLEN	Set to 1 for 2 byte read or write operations. Set to 0 for 1-byte operations.

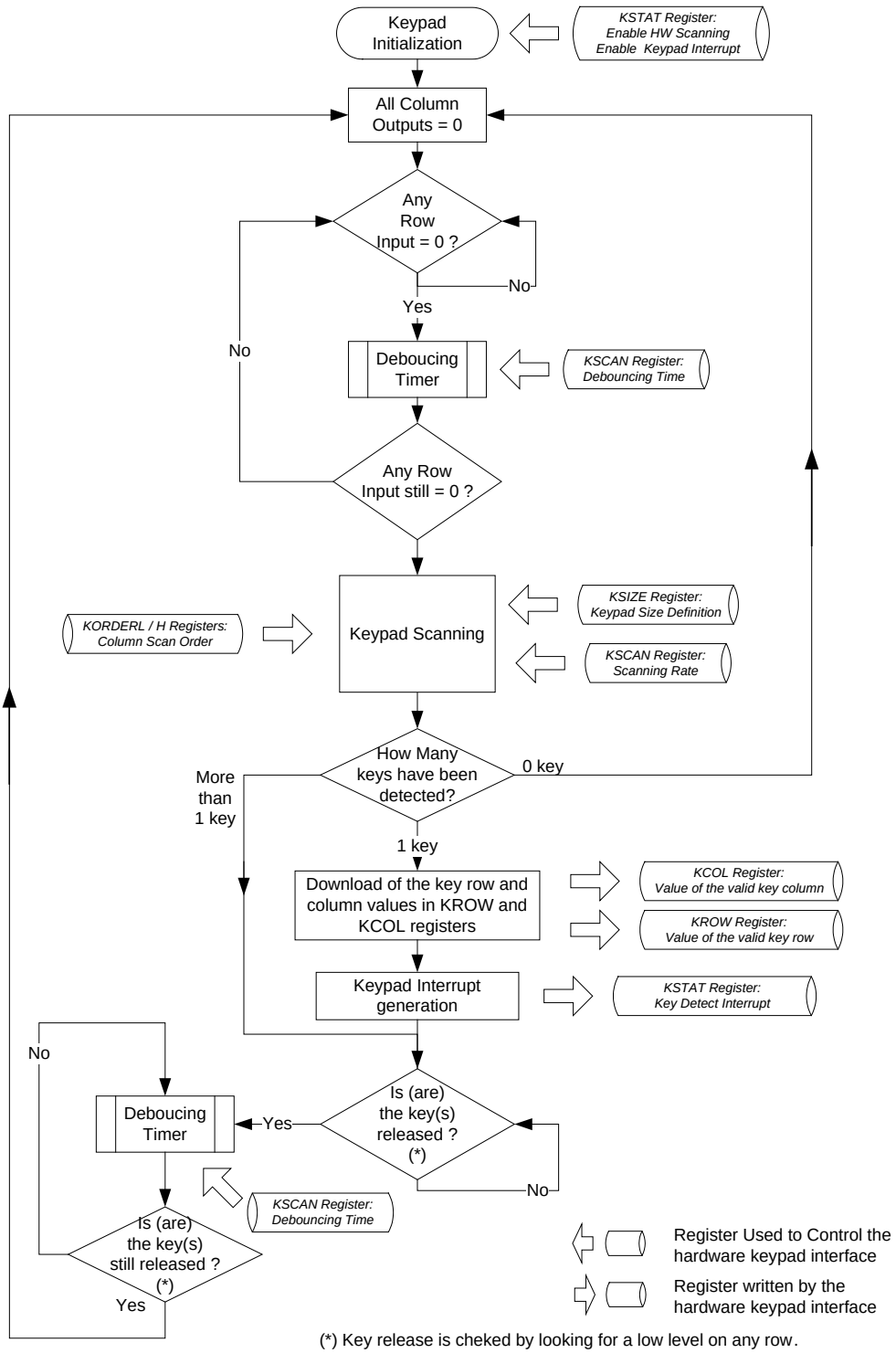


Figure 13: Keypad Interface Flow Chart

SRX Data Register (SRXData): 0xFE09 ← 0x00

Table 81: The SRXData Register

MSB LSB

SRXDAT.7	SRXDAT.6	SRXDAT.5	SRXDAT.4	SRXDAT.3	SRXDAT.2	SRXDAT.1	SRXDAT.0

Bit	Function
SRXData.7	(Read only) Data received from the smart card. Data received from the smart card gets stored in a FIFO that is read by the firmware.
SRXData.6	
SRXData.5	
SRXData.4	
SRXData.3	
SRXData.2	
SRXData.1	
SRXData.0	

Table 93: Divider Values for the ETU Clock

	Fi code	0000	0001	0010	0011	0100	0101
Di code	F→ D↓	372	372	558	744	1116	1488
0001	1	744	744	1116	1488	2232	2976
0010	2	372	372	558	744	1116	1488
0011	4	186	186	279	372	558	744
0100	8	93	93	138	186	279	372
1000	12	62	62	93	124	186	248
0101	16	47	47	70	93	140	186
1001	20	37	37	56	74	112	149
0110	32	23	23	35	47	70	93

	Fi code	0110	1001	1010	1011	1100	1101
Di code	F→ D↓	1860	512	768	1024	1536	2048
0001	1	3720	1024	1536	2048	3072	4096
0010	2	1860	512	768	1024	1536	2048
0011	4	930	256	384	512	768	1024
0100	8	465	128	192	256	384	512
1000	12	310	85	128	171	256	341
0101	16	233	64	96	128	192	256
1001	20	186	51	77	102	154	205
0110	32	116	32	48	64	96	128

Block Guard Time Register (BGT): 0xFE16 ← 0x10

This register contains the Extra Guard Time Value (EGT) most-significant bit. The Extra Guard Time indicates the minimum time between the leading edges of the start bit of consecutive characters. The delay is depends on the T=0/T=1 mode. Used in transmit mode. This register also contains the Block Guard Time (BGT) value. Block Guard Time is the minimum time between the leading edge of the start bit of the last character received and the leading edge of the start bit of the first character transmitted. This should not be set less than the character length. The transmission of the first character will be held off until BGT has elapsed regardless of the TX data and TX/RX control bit timing.

Table 95: The BGT Register

MSB							LSB
EGT.8	–	–	BGT.4	BGT.3	BGT.1	BGT.2	BGT.0

Bit	Symbol	Function
BGT.7	EGT.8	Most-significant bit for 9-bit EGT timer. See the EGT register.
BGT.6	–	
BGT.5	–	
BGT.4	BGT.4	Time in ETUs between the start bit of the last received character to start bit of the first character transmitted to the smart card. Default value is 22.
BGT.3	BGT.3	
BGT.2	BGT.2	
BGT.1	BGT.1	
BGT.0	BGT.0	

Extra Guard Time Register (EGT): 0xFE17 ← 0x0C

This register contains the Extra Guard Time Value (EGT) least-significant byte. The Extra Guard Time indicates the minimum time between the leading edges of the start bit of consecutive characters. The delay depends on the T=0/T=1 mode. Used in transmit mode.

Table 96: The EGT Register

MSB							LSB
EGT.7	EGT.6	EGT.5	EGT.4	EGT.3	EGT.1	EGT.2	EGT.0

Bit	Function
EGT.7	Time in ETUs between start bits of consecutive characters. In T=0 mode, the minimum is 1. In T=0, the leading edge of the next start bit may be delayed if there is a break detected from the smart card. Default value is 12. In T=0 mode, regardless of the value loaded, the minimum value is 12, and for T=1 mode, the minimum value is 11.
EGT.6	
EGT.5	
EGT.4	
EGT.3	
EGT.2	
EGT.1	
EGT.0	

1.7.16 VDD Fault Detect Function

The 73S1210F contains a circuit to detect a low-voltage condition on the supply voltage V_{DD}. If enabled, it will deactivate the active internal smart card interface when V_{DD} falls below the V_{DD} Fault threshold. The register configures the V_{DD} Fault threshold for the nominal default of 2.3V* or a user selectable threshold. The user's code may load a different value using the FOVRVDDF bit = 1 after the power-up cycle has completed.

VDDFault Control Register (VDDFCtl): 0xFFD4 ← 0x00

Table 108: The VDDFCtl Register

MSB LSB

–	FOVRVDDF	VDDFLTEN	–	STXDAT.3	VDDFTH.2	VDDFTH.1	VDDFTH.0

Bit	Symbol	Function
VDDFCtl.7	–	
VDDFCtl.6	FOVRVDDF	Setting this bit high will allow the VDDFLT(2:0) bits set in this register to control the VDDFault threshold. When this bit is set low, the VDDFault threshold will be set to the factory default setting of 2.3V*.
VDDFCtl.5	VDDFLTEN	Set = 1 will disable VDD Fault operation.
VDDFCtl.4	–	
VDDFCtl.3	–	
VDDFCtl.2	VDDFTH.2	VDD Fault Threshold. Bit Value(2:0) VDDFault Voltage 000 2.3 (nominal default) 001 2.4 010 2.5 011 2.6 100 2.7 101 2.8 110 2.9 111 3.0
VDDFCtl.1	VDDFTH.1	
VDDFCtl.0	VDDFTH.0	

* Note: The V_{DD} Fault factory default can be set to any threshold as defined by bits VDDFTH(2:0). The 73S1210F has the capability to burn fuses at the factory to set the factory default to any of these voltages. Contact Teridian for further details.

3.3 Digital IO Characteristics

These requirements pertain to digital I/O pin types with consideration of the specific pin function and configuration. The LED(1:0) pins have pull-ups that may be enabled. The Row pins have 100kΩ pull-ups.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Voh	Output level, high	Ioh = -2mA	0.8 * V_{DD}		V_{DD}	V
		OFF_REQ pin - I_{OH} = -1mA	V_{DD} - 0.45			V
Vol	Output level, low	Iol = 2mA	0		0.3	V
		OFF_REQ pin - Iol = 2mA			0.45	V
Vih	Input voltage, high	2.7v < VDD <3.6v	1.8		V_{DD} +0.3	V
Vil	Input voltage, low	2.7v < VDD <3.6v	-0.3		0.6	V
		RESET, ON_OFF,PRES pins	-0.3		0.8	V
Ileak	Leakage current	0 < Vin < VDD All output modes disabled, pull-up/downs disabled	-5		5	µA
Ipu	Pull-up current	If provided and enabled, Vout < 0.1v	-5			µA
Ipd	Pull-down current	If provided and enabled, Vout > VDD – 0.1v			5	µA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Iled	LED drive current	Vout = 1.3V, 2.7v < VDD < 3.6v		2 4 10		mA
Iolkrow	Keypad row output low current	0.0v < Voh < 0.1v when pull-up R is enabled		40	100	µA
Iolkcol	Keypad column output high current	0.0v < Voh < 0.1v when col. is pulled low		1.5	3	mA

I_{DD_IN}	Supply Current – pins 28 + 40 (internal consumption – digital core)	CPU clock @ 24MHz		29	33.5	mA
		CPU clock @ 12MHz		21	24	mA
		CPU clock @ 6MHz		15.5	18	mA
		CPU clock @ 3.69MHz		13.5	15.5	mA
		Power down (-40° to 85°C)		8	50	µA
		Power down (25°C)		6	15	µA
I_{DD_OUT}	Supply Current – pin 68 (available to external circuitry)	Circuit ON			20	mA
I_{VBUS}	Supply Current from V_{BUS}	V_{CC} off, $I_{DDINTERNAL}$ < 20µA		0.2	0.4	mA
I_{VBAT} I_{VPC}	Supply Current from V_{BAT} or V_{PC}	Circuit OFF		0.01	1	µA
$VBUS_{ON}$	V_{BUS} detection threshold			3.5		V
$VBUS_{IDIS}$	V_{BUS} discharge current			50		µA
External Capacitor Values						
C_{VPC}	External filter capacitor for V_{PC}		8.0	10.0	12.0	µF
C_{VP}	External filter capacitor for V_P		2.0	4.7	10.0	µF
C_{VDD}*	External filter capacitors for V_{DD}		0.2		1.0	µF
C_{VCC}	External filter capacitor for V_{CC}	C_{VCC} should be ceramic with low ESR (<100MΩ).	0.2	0.47	1.0	µF

*Note: Recommend on 0.1µF for each V_{DD} pin.

3.8 Current Fault Detection Circuits

Symbol	Parameter	Condition	Min	Typ.	Max	Unit
IV_{Pmax}	V_P over current fault				150	mA
I_{DDmax}	VDD over-current limit		40		100	mA
I_{CCF}	Card overcurrent fault		80		150	mA
I_{CCF1P8}	Card overcurrent fault	V_{CC} = 1.8V	60		130	mA

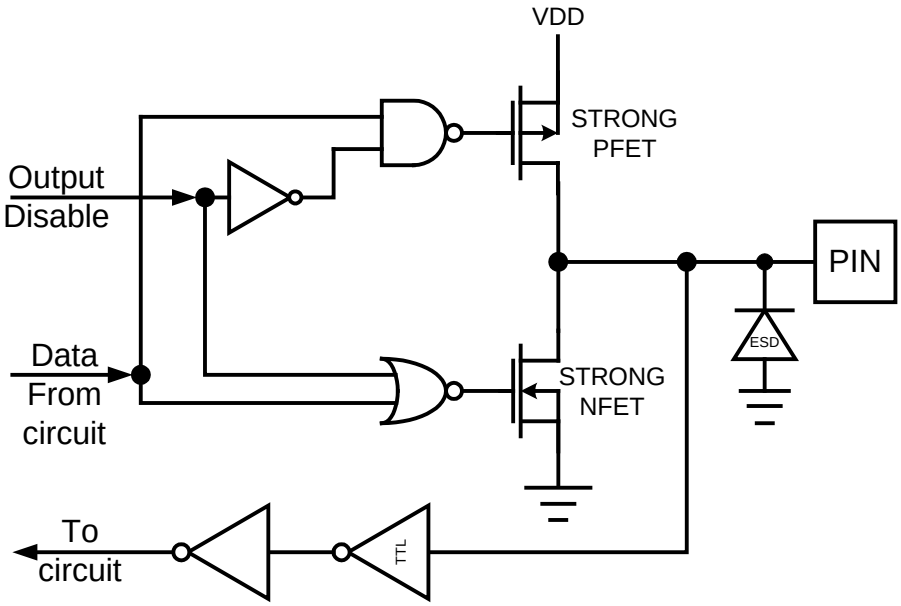


Figure 28: Digital I/O Circuit

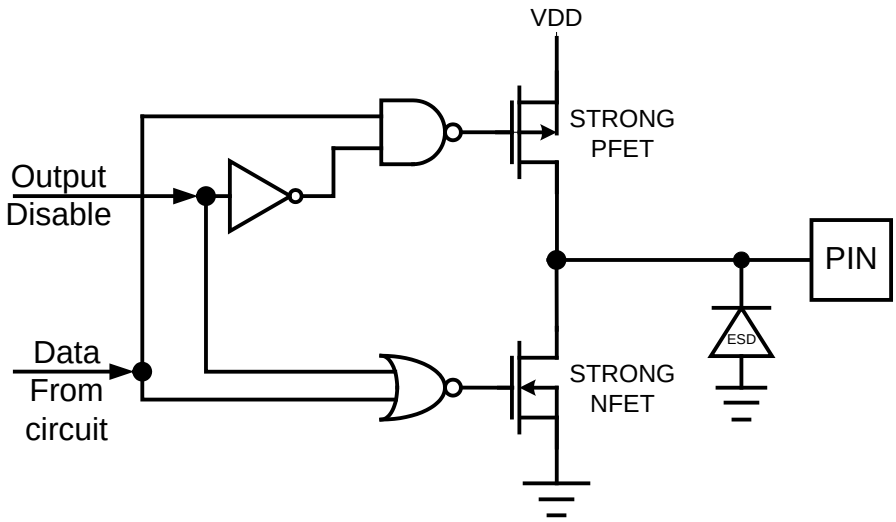


Figure 29: Digital Output Circuit