Analog Devices Inc./Maxim Integrated - 73S1210F-44M/F/PC Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80515
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SmartCard, UART/USART
Peripherals	LED, POR, WDT
Number of I/O	8
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/73s1210f-44m-f-pc

Table 4: Internal Data Memory Map

Address	Direct Addressing	Indirect Addressing
0xFF	Special Function Registers (SFRs)	RAM
0x80		
0x7F	Byte-addressable area	
0x30		
0x2F	Byte or bit-addressable area	
0x20		
0x1F	Register banks R0…R7 (x4)	
0x00		

External Data Memory: While the 80515 can address up to 64KB of external data memory in the space from 0x0000 to 0xFFFF, only the memory ranges shown in Figure 2 contain physical memory. The 80515 writes into external data memory when the MPU executes a MOVX @Ri,A or MOVX @DPTR,A instruction. The MPU reads external data memory by executing a MOVX A,@Ri or MOVX A,@DPTR instruction.

There are two types of instructions, differing in whether they provide an eight-bit or sixteen-bit indirect address to the external data RAM.

In the first type (MOVX A,@Ri), the contents of R0 or R1, in the current register bank, provide the eight lower-ordered bits of address. This method allows the user access to the first 256 bytes of the 2KB of external data RAM. In the second type of MOVX instruction (MOVX A,@DPTR), the data pointer generates a sixteen-bit address.

1.5.2 IRAM Special Function Registers (Generic 80515 SFRs)

Table 7 shows the location of the SFRs and the value they assume at reset or power-up.

Table 7: IRAM Special Function Registers Reset Values

Name	Location	Reset Value	Description
SP	0x81	0x07	Stack Pointer
DPL	0x82	0x00	Data Pointer Low 0
DPH	0x83	0x00	Data Pointer High 0
DPL1	0x84	0x00	Data Pointer Low 1
DPH1	0x85	0x00	Data Pointer High 1
WDTREL	0x86	0x00	Watchdog Timer Reload register
PCON	0x87	0x00	Power Control
TCON	0x88	0x00	Timer/Counter Control
TMOD	0x89	0x00	Timer Mode Control
TL0	0x8A	0x00	Timer 0, low byte
TL1	0x8B	0x00	Timer 1, high byte
TH0	0x8C	0x00	Timer 0, low byte
TH1	0x8D	0x00	Timer 1, high byte
MCLKCtl	0x8F	0x0A	Master Clock Control
USR70	0x90	0xFF	User Port Data (7:0)
UDIR70	0x91	0xFF	User Port Direction (7:0)
DPS	0x92	0x00	Data Pointer Select Register
ERASE	0x94	0x00	Flash Erase
S0CON	0x98	0x00	Serial Port 0, Control Register
S0BUF	0x99	0x00	Serial Port 0, Data Buffer
IEN2	0x9A	0x00	Interrupt Enable Register 2
S1CON	0x9B	0x00	Serial Port 1, Control Register
S1BUF	0x9C	0x00	Serial Port 1, Data Buffer
S1RELL	0x9D	0x00	Serial Port 1, Reload Register, low byte
IEN0	0xA8	0x00	Interrupt Enable Register 0
IP0	0xA9	0x00	Interrupt Priority Register 0
S0RELL	0xAA	0xD9	Serial Port 0, Reload Register, low byte
FLSHCTL	0xB2	0x00	Flash Control
PGADDR	0xB7	0x00	Flash Page Address
IEN1	0xB8	0x00	Interrupt Enable Register 1
IP1	0xB9	0x00	Interrupt Priority Register 1
S0RELH	0xBA	0x03	Serial Port 0, Reload Register, high byte
S1RELH	0xBB	0x03	Serial Port 1, Reload Register, high byte
IRCON	0xC0	0x00	Interrupt Request Control Register
T2CON	0xC8	0x00	Timer 2 Control
PSW	0xD0	0x00	Program Status Word
KCOL	0XD1	0x1F	Keypad Column

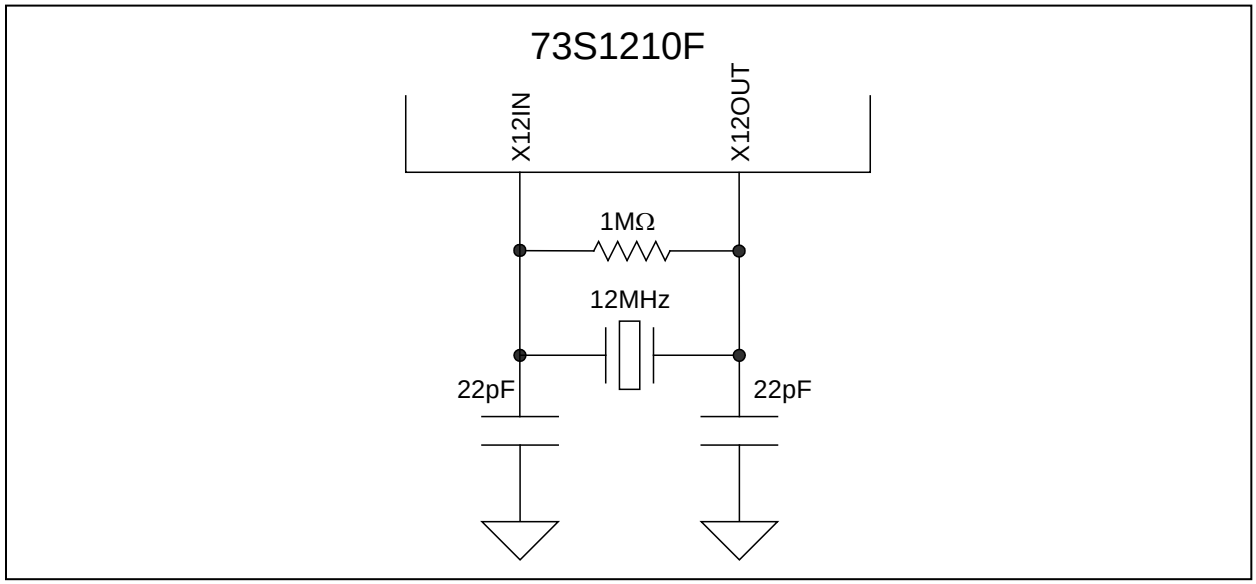
MPU Clock Control Register (MPUCKCtl): 0xFFA1 ← 0x0C

Table 13: The TCON Register

MSB							LSB
–	–	MDIV.5	MDIV.4	MDIV.3	MDIV.2	MDIV.1	MDIV.0

Bit	Symbol	Function
MPUCKCtl.7	–	
MPUCKCtl.6	–	
MPUCKCtl.5	MDIV.5	This value determines the ratio of the MPU master clock frequency to the VCO frequency (MCLK) such that MPUClk = MCLK/(2 * (MPUCKDiv(5:0) + 1)). Do not use values of 0 or 1 for MPUCKDiv(n). Default is 0Ch to set CPCLK = 3.6923MHz.
MPUCKCtl.4	MDIV.4	
MPUCKCtl.3	MDIV.3	
MPUCKCtl.2	MDIV.2	
MPUCKCtl.1	MDIV.1	
MPUCKCtl.0	MDIV.0	

The oscillator circuits are designed to connect directly to standard parallel resonant crystal in a Pierce oscillator configuration. Each side of the crystal should include a 22pF capacitor to ground for both oscillator circuits and a 1MΩ resistor is required across the 12MHz crystal.



Note: The crystal should be placed as close as possible to the IC, and vias should be avoided.

Figure 4: Oscillator Circuit

73S1210F will go into the "OFF" state (when V_{BUS} is not present). If the ON/OFF switch function is not desired and the application does not need to shut down power on VDD, the ON_OFF input can be permanently grounded which will automatically turn on VDD when power is supplied on any of the VPC, VBAT or VBUS power supply inputs.

If power is applied to both V_{BAT} and V_{BUS}, the circuit will automatically consume power from only the V_{BUS} source. The 73S1210F will be unconditionally "ON" when V_{BUS} is applied. If the V_{BUS} source is removed, the 73S1210F will switchover to the VBAT input supply and remain in the "ON" state. The firmware should assert SCPWRDN based on no activity or V_{BUS} removal to reduce battery power consumption. When operating from V_{BUS}, and not calling for V_{CC}, the step-up converter becomes a simple switch connecting V_{BUS} to V_P in order to save power.

Note: When the ON_OFF switch function is not needed, i.e. when the 73S1210F must be in an always-ON state when using another supply than VBUS (V_{PC} or V_{BAT}), some external discrete components are needed.

1.7.4 Power Control Modes

The 73S1210F contains circuitry to disable portions of the device and place it into a lower power standby mode or power down the 73S1210F into its "OFF" mode. The standby mode will stop the core, clock subsystem and the peripherals connected to it. This is accomplished by either shutting off the power or disabling the clock going to the block. The Miscellaneous Control registers MISCtl0, MISCtl1 and the Master Clock Control register (MCLKCtl) provide control over the power modes. The PWRDN bit in MISCtl0 will setup the 73S1210F for standby or "OFF" modes. Depending on the state of the ON/OFF circuitry and power applied to the VBUS input, the 73S1210F will go into either standby mode or power "OFF" mode. If system power is provided by, VBUS or the ON/OFF circuitry is in the "ON" state, the MPU core will placed into standby mode. If the VBUS input is not sourcing power and the ON/OFF circuitry is in the "OFF" state, setting the PWRDN bit will shut down the converter and VP will turn off. The power down mode should only be initiated by setting the PWRDN bit in the MISCtl0 register and not by manipulating individual control bits in various registers. Figure 6 shows how the PWRDN bit controls the various functions that comprise power down state.

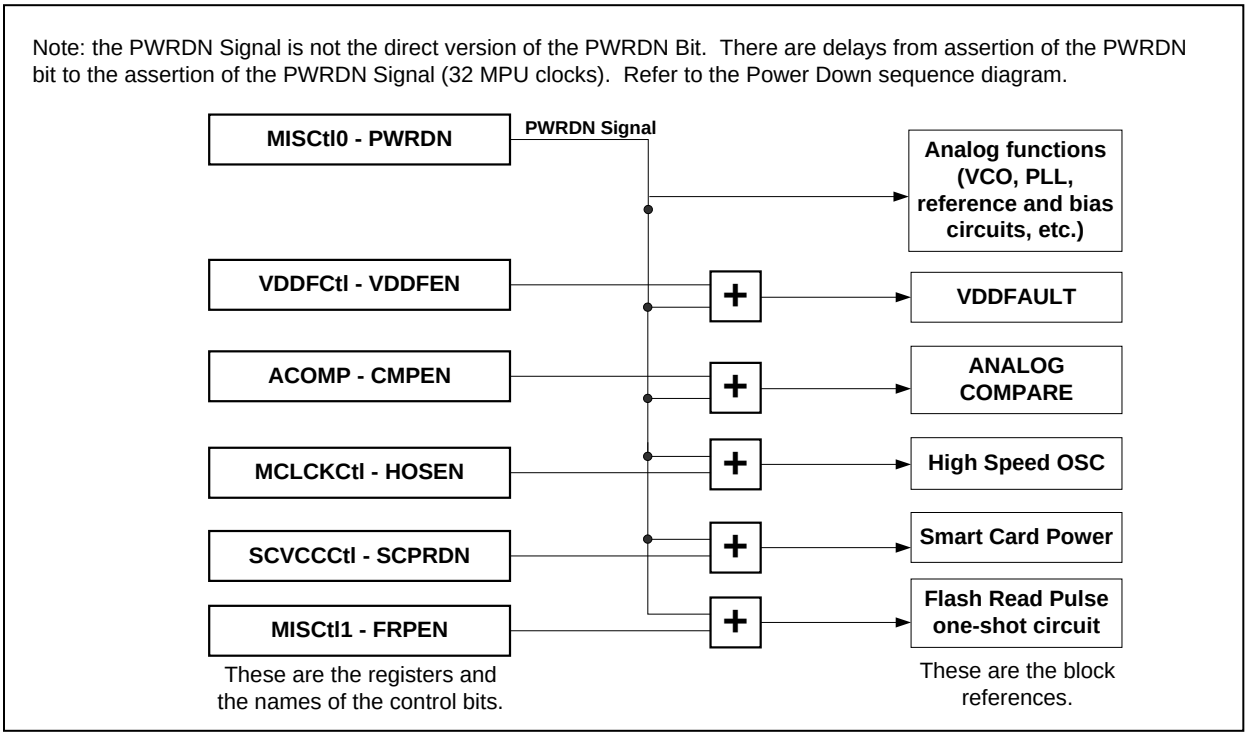


Figure 6: Power Down Control

1.7.5.1 Interrupt Overview

When an interrupt occurs, the MPU will vector to the predetermined address as shown in Table 32. Once the interrupt service has begun, it can only be interrupted by a higher priority interrupt. The interrupt service is terminated by a return from the RETI instruction. When a RETI is performed, the processor will return to the instruction that would have been next when the interrupt occurred.

When the interrupt condition occurs, the processor will also indicate this by setting a flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Each interrupt flag is sampled once per machine cycle, then samples are polled by the hardware. If the sample indicates a pending interrupt when the interrupt is enabled, then the interrupt request flag is set. On the next instruction cycle, the interrupt will be acknowledged by hardware forcing an LCALL to the appropriate vector address.

Interrupt response will require a varying amount of time depending on the state of the MPU when the interrupt occurs. If the MPU is performing an interrupt service with equal or greater priority, the new interrupt will not be invoked. In other cases, the response time depends on the current instruction. The fastest possible response to an interrupt is 7 machine cycles. This includes one machine cycle for detecting the interrupt and six cycles to perform the LCALL.

1.7.5.2 Special Function Registers for Interrupts

Interrupt Enable 0 Register (IEN0): 0xA8 ← 0x00

Table 19: The IEN0 Register

MSB							LSB
EAL	WDT	–	ES0	ET1	EX1	ET0	EX0

Bit	Symbol	Function
IEN0.7	EAL	EAL = 0 – disable all interrupts.
IEN0.6	WDT	Not used for interrupt control.
IEN0.5	–	
IEN0.4	ES0	ES0 = 0 – disable serial channel 0 interrupt.
IEN0.3	ET1	ET1 = 0 – disable timer 1 overflow interrupt.
IEN0.2	EX1	EX1 = 0 – disable external interrupt 1.
IEN0.1	ET0	ET0 = 0 – disable timer 0 overflow interrupt.
IEN0.0	EX0	EX0 = 0 – disable external interrupt 0.

Table 26: Control Bits for External Interrupts

Enable Bit	Description
EX0	Enable external interrupt 0
EX1	Enable external interrupt 1
EX2	Enable external interrupt 2
EX3	Enable external interrupt 3
EX4	Enable external interrupt 4
EX5	Enable external interrupt 5
EX6	Enable external interrupt 6

Flag Bit	Description
IE0	External interrupt 0 flag
IE1	External interrupt 1 flag
IEX2	External interrupt 2 flag
IEX3	External interrupt 3 flag
IEX4	External interrupt 4 flag
IEX5	External interrupt 5 flag
IEX6	External interrupt 6 flag

1.7.5.4 Power Down Interrupt Logic

The 73S1210F contains special interrupt logic to allow INT0 to wake up the CPU from a power down (CPU STOP) state. See the Power Control Modes section for details.

1.7.5.5 Interrupt Priority Level Structure

All interrupt sources are combined in groups, as shown in Table 27.

Table 27: Priority Level Groups

Group			
0	External interrupt 0	Serial channel 1 interrupt	
1	Timer 0 interrupt	–	External interrupt 2
2	External interrupt 1	–	External interrupt 3
3	Timer 1 interrupt	–	External interrupt 4
4	Serial channel 0 interrupt	–	External interrupt 5
5	–	–	External interrupt 6

Each group of interrupt sources can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1. If requests of the same priority level are received simultaneously, an internal polling sequence as per Table 31 determines which request is serviced first.

IEN enable bits must be set to permit any of these interrupts to occur. Likewise, each interrupt has its own flag bit that is set by the interrupt hardware and is reset automatically by the MPU interrupt handler.

Interrupt Priority 0 Register (IP0): 0xA9 ← 0x00

Table 28: The IP0 Register

MSB LSB

–	WDTS	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0

Note: WDTS is not used for interrupt controls.

Miscellaneous Control Register 0 (MISCtl0): 0xFFF1 ← 0x00

Transmit and receive (TX and RX) pin selection and loop back test configuration are setup via this register.

Table 37: The MISCtl0 Register

MSB							LSB
PWRDN	–	–	–	–	–	SLPBK	SSEL

Bit	Symbol	Function
MISCtl0.7	PWRDN	This bit places the 73S1210F into a power down state.
MISCtl0.6	–	
MISCtl0.5	–	
MISCtl0.4	–	
MISCtl0.3	–	
MISCtl0.2	–	
MISCtl0.1	SLPBK	1 = UART loop back testing mode. The pins TXD and RXD are to be connected together externally (with SLPBK =1) and therefore: SLPBK SSEL Mode 0 0 normal using Serial_0 0 1 normal using Serial_1 1 0 Serial_0 TX feeds Serial_1 RX 1 1 Serial_1 TX feeds Serial_0 RX
MISCtl0.0	SSEL	Selects either Serial_1 if set =1 or Serial_0 if set = 0 to be connected to RXD and TXD pins.

1.7.6.1 Serial Interface 0

The Serial Interface 0 can operate in 4 modes:

- **Mode 0**

  Pin RX serves as input and output. TX outputs the shift clock. 8 bits are transmitted with LSB first. The baud rate is fixed at 1/12 of the crystal frequency. Reception is initialized in Mode 0 by setting the flags in S0CON as follows: RI0 = 0 and REN0 = 1. In other modes, a start bit when REN0 = 1 starts receiving serial data.

- **Mode 1**

  Pin RX serves as input, and TX serves as serial output. No external shift clock is used, 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the transmission, 8 data bits are available by reading S0BUF, and stop bit sets the flag RB80 in the Special Function Register S0CON. In mode 1 either internal baud rate generator or timer 1 can be use to specify baud rate.

- **Mode 2**

  This mode is similar to Mode 1, with two differences. The baud rate is fixed at 1/32 or 1/64 of oscillator frequency and 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the serial interface: at transmission, bit TB80 in S0CON is output as the 9th bit, and at receive, the 9th bit affects RB80 in Special Function Register S0CON.

1.7.7 Timers and Counters

The 80515 has two 16-bit timer/counter registers: Timer 0 and Timer 1. These registers can be configured for counter or timer operations.

In timer mode, the register is incremented every machine cycle, meaning that it counts up after every 12 periods of the MPU clock signal.

In counter mode, the register is incremented when the falling edge is observed at the corresponding input signal T0 or T1 (T0 and T1 are the timer gating inputs derived from USR[0:7] pins, see the User (USR) Ports section). Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/2 of the oscillator frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least 1 machine cycle.

Four operating modes can be selected for Timer 0 and Timer 1. Two Special Function Registers (TMOD and TCON) are used to select the appropriate mode.

The Timer 0 load registers are designated as TL0 and TH0 and the Timer 1 load registers are designated as TL1 and TH1.

Timer/Counter Mode Control Register (TMOD): 0x89 ← 0x00

Table 40: The TMOD Register

MSB LSB

GATE	C/T	M1	M0	GATE	C/T	M1	M0
Timer 1				**Timer 0**			

Bits TR1 and TR0 in the TCON register start their associated timers when set.

Bit	Symbol	Function
TMOD.7 TMOD.3	Gate	If set, enables external gate control (USR pin(s) connected to T0 or T1 for Counter 0 or 1, respectively). When T0 or T1 is high, and TRx bit is set (see the TCON register), a counter is incremented every falling edge on T0 or T1 input pin. If not set, the TRx bit controls the corresponding timer.
TMOD.6 TMOD.2	C/T	Selects Timer or Counter operation. When set to 1, the counter operation is performed based on the falling edge of T0 or T1. When cleared to 0, the corresponding register will function as a timer.
TMOD.5 TMOD.1	M1	Selects the mode for Timer/Counter 0 or Timer/Counter 1, as shown in the TMOD description.
TMOD.4 TMOD.0	M0	Selects the mode for Timer/Counter 0 or Timer/Counter 1, as shown in the TMOD description.

Table 41: Timers/Counters Mode Description

M1	M0	Mode	Function
0	0	Mode 0	13-bit Counter/Timer.
0	1	Mode 1	16-bit Counter/Timer.
1	0	Mode 2	8-bit auto-reload Counter/Timer.
1	1	Mode 3	If Timer 1 M1 and M0 bits are set to '1', Timer 1 stops. If Timer 0 M1 and M0 bits are set to '1', Timer 0 acts as two independent 8-bit Timer/Counters.

Interrupt Enable 1 Register (IEN1): 0xB8 ← 0x00

Table 44: The IEN1 Register

MSB							LSB
–	SWDT	EX6	EX5	EX4	EX3	EX2	–

Bit	Symbol	Function
IEN1.7	–	
IEN1.6	SWDT	Watchdog timer start/refresh flag. Set to activate/refresh the watchdog timer. When directly set after setting WDT, a watchdog timer refresh is performed. Bit SWDT is reset by the hardware 12 clock cycles after it has been set.
IEN1.5	EX6	EX6 = 0 – disable external interrupt 6.
IEN1.4	EX5	EX5 = 0 – disable external interrupt 5.
IEN1.3	EX4	EX4 = 0 – disable external interrupt 4.
IEN1.2	EX3	EX3 = 0 – disable external interrupt 3.
IEN1.1	EX2	EX2 = 0 – disable external interrupt 2.
IEN1.0	–	

Interrupt Priority 0 Register (IP0): 0xA9 ← 0x00

Table 45: The IP0 Register

MSB							LSB
–	WDTS	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0

Bit	Symbol	Function
IP0.6	WDTS	Watchdog timer status flag. Set when the watchdog timer has expired. The internal reset will be generated, but this bit will not be cleared by the reset. This allows the user program to determine if the watchdog timer caused the reset to occur and respond accordingly. Can be read and cleared by software.

Note: The remaining bits in the IP0 register are not used for watchdog control.

Watchdog Timer Reload Register (WDTREL): 0x86 ← 0x00

Table 46: The WDTREL Register

MSB							LSB
WDPSEL	WDREL6	WDREL5	WDREL4	WDREL3	WDREL2	WDREL1	WDREL0

Bit	Symbol	Function
WDTREL.7	WDPSEL	Prescaler select bit. When set, the watchdog is clocked through an additional divide-by-16 prescaler.
WDTREL.6 to WDTREL.0	WDREL6-0	Seven bit reload value for the high-byte of the watchdog timer. This value is loaded to the WDT when a refresh is triggered by a consecutive setting of bits WDT and SWDT.

External Interrupt Control Register (USRIntCtl1) : 0xFF90 ← 0x00

Table 50: The USRIntCtl1 Register

MSB							LSB
–	U1IS.6	U1IS.5	U1IS.4	–	U0IS.2	U0IS.1	U0IS.0

External Interrupt Control Register (USRIntCtl2) : 0xFF91 ← 0x00

Table 51: The USRIntCtl2 Register

MSB							LSB
–	U3IS.6	U3IS.5	U3IS.4	–	U2IS.2	U2IS.1	U2IS.0

External Interrupt Control Register (USRIntCtl3) : 0xFF92 ← 0x00

Table 52: The USRIntCtl3 Register

MSB							LSB
–	U5IS.6	U5IS.5	U5IS.4	–	U4IS.2	U4IS.1	U4IS.0

External Interrupt Control Register (USRIntCtl4) : 0xFF93 ← 0x00

Table 53: The USRIntCtl4 Register

MSB							LSB
–	U7IS.6	U7IS.5	U7IS.4	–	U6IS.2	U6IS.1	U6IS.0

External Interrupt Control Register (INT6Ctl): 0xFF95 ← 0x00

Table 55: The INT6Ctl Register

MSB LSB

–	–	VFTIEN	VFTINT	I2CIEN	I2CINT	ANIEN	ANINT

Bit	Symbol	Function
INT6Ctl.7	–	
INT6Ctl.6	–	
INT6Ctl.5	VFTIEN	VDD fault interrupt enable.
INT6Ctl.4	VFTINT	VDD fault interrupt flag.
INT6Ctl.3	I2CIEN	I^2C interrupt enabled.
INT6Ctl.2	I2CINT	I^2C interrupt flag.
INT6Ctl.1	ANIEN	If ANIEN = 1 Analog Compare event interrupt is enabled. When masked (ANIEN = 0), ANINT (bit 0) may be set, but no interrupt is generated.
INT6Ctl.0	ANINT	(Read Only) Set when the selected ANA_IN signal changes with respect to the selected threshold if Compare_Enable is asserted. Cleared on read of register.

1.7.11 LED Driver

The 73S1210F provides a single dedicated output pin for driving an LED. The LED driver pin can be configured as a current source that will pull to ground to drive an LED that is connected to VDD without the need for an external current limiting resistor. This pin may be used as general purpose output with the programmed pull-down current and a strong (CMOS) pull-up, if enabled. The analog block must be enabled when this output is being used to drive the selected output current.

This pin may be used as an input with consideration of the programmed output current and level. The register bit when read, indicates the state of the pin.

LED Control Register (LEDCtl): 0xFFF3 ← 0xFF

Table 56: The LEDCtl Register

MSB LSB

–	LPUEN	ISET.1	ISET.0	–	–	–	LEDD0

Bit	Symbol	Function
LEDCtl.7	–	
LEDCtl.6	LPUEN	0 = Pull-ups are enabled for all of the LED pins.
LEDCtl.5	ISET.1	These two bits control the drive current (to ground) for the LED driver pin. Current levels are: 00 = 0ma(off) 01 = 2ma 10 = 4ma 11 = 10ma
LEDCtl.4	ISET.0	
LEDCtl.3	–	
LEDCtl.2	–	
LEDCtl.1	–	
LEDCtl.0	LEDD0	Write data controls output level of pin LED0. Read will report level of pin LED0.

Keypad Scan Time Register (KSIZE): 0xD5 ← 0x00

This register is not applicable when HWSCEN is not set. Unused row inputs should be connected to VDD.

Table 68: The KSIZE Register

MSB LSB

–	–	ROWSIZ.2	ROWSIZ.1	ROWSIZ.0	COLSIZ.2	COLSIZ.1	COLSIZ.0

Bit	Symbol	Function
KSIZE.7	–	
KSIZE.6	–	
KSIZE.5	ROWSIZ.2	Defines the number of rows in the keypad. Maximum number is 6 given the number of row pins on the package. Allows for a reduced keypad size for scanning.
KSIZE.4	ROWSIZ.1	
KSIZE.3	ROWSIZ.0	
KSIZE.2	COLSIZ.2	Defines the number of columns in the keypad. Maximum number is 5 given the number of column pins on the package. Allows for a reduced keypad size for scanning.
KSIZE.1	COLSIZ.1	
KSIZE.0	COLSIZ.0	

Special Notes Regarding Synchronous Mode Operation

When the SCISYN or SCESNC bits (SPrtcol, bit 7, bit 5, respectively) are set, the selected smart card interface operates in synchronous mode and there are changes in the definition and behavior of pertinent register bits and associated circuitry. The following requirements are to be noted:

1. The source for the smart card clock (CLK or SCLK) is the ETU counter. Only the actively selected interface can have a running synchronous clock. In contrast, an unselected interface may have a running clock in the asynchronous mode of operation.

2. The control bits CLKLVL, SCLKLVL, CLKOFF, and SCLKOFF are functional in synchronous mode. When the CLKOFF bit is set, it will not truncate either the logic low or logic high period when the (stop at) level is of opposite polarity. The CLK/SCLK signal will complete a correct logic low or logic high duty cycle before stopping at the selected level. The CLK "start" is a result of the falling edge of the CLKOFF bit. Setting clock to run when it is stopped low will result in a half period of low before going high. Setting clock to run when it is stopped high will result in the clock going low immediately and then running at the selected rate with 50% duty cycle (within the limitations of the ETU divisor value).

3. The Rlen(7:0) is configured to count the falling edges of the ETU clock (CLK or SCLK) after it has been loaded with a value from 1 to 255. A value of 0 disables the counting function and RLen functions such as I/O source selection (I/O signal bypasses the FIFOs and is controlled by the SCCLK/SCECLK SFRs). When the RLen counter reaches the "max" (loaded) value, it sets the WAITTO interrupt (SCInt, bit 7), which is maskable via WTOIEN (SCIE, bit 7). It must be reloaded in order to start the counting/clocking process again. This allows the processor to select the number of CLK cycles and hence, the number of bits to be read or written to/from the card.

4. The FIFO is not clocked by the first CLK (falling) edge resulting from a CLKOFF de-assertion (a clock start event) when the CLK was stopped in the high state and RLen has been loaded but not yet clocked.

5. The state of the pin IO or SIO is sampled on the rising edge of CLK/SCLK and stored in bit 5 of the SCCtl/SCECtl register.

6. When Rlen = max or 0 and I2CMODE= 1 (STXCtl, b7), the IO or SIO signal is directly controlled by the data and direction bits in the respective SCCtl and SCECtl register. The state of the data in the TX FIFO is bypassed.

7. In the SPrtcol register, bit 6 (MODE9/8B) becomes active. When set, the RXData FIFO will read nine-bit words with the state of the ninth bit being readable in SRXCtl, bit 7 (B9DAT). The RXDAV interrupt will occur when the ninth bit has been clocked in (rising edge of CLK or SCLK).

8. Care must be taken to clear the RX and TX FIFOs at the start of any transaction. The user shall read the RX FIFO until it indicates empty status. Reading the TX FIFO twice will reset the input byte pointer and the next write to the TX FIFO will load the byte to the "first out" position. Note that the bit pointer (serializer/deserializer) is reset to bit 0 on any change of the TX/RXD bit.

Special bits that are only active for sync mode include: SRXCtl, b7 "BIT9DAT", SPrtcol, b6 "MODE9/8B", STXCtl, b7 "I2CMODE", and the definition of SCInt, b7, which was "WAITTO", becomes RLenINT interrupt, and SCIE, b7, which was "WTOIEN", becomes RLenIEN.

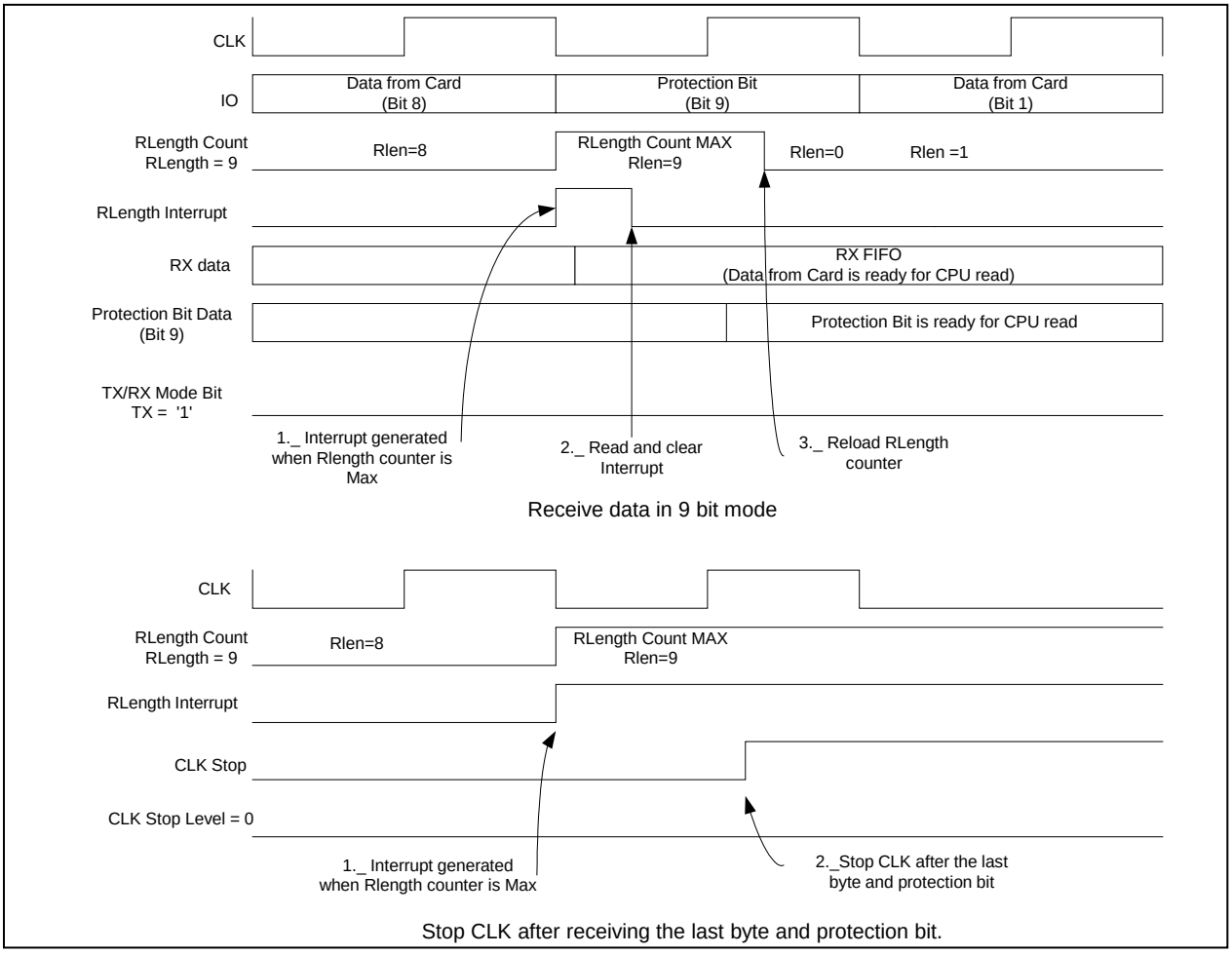


Figure 24: Operation of 9-bit Mode in Sync Mode

Synchronous card operation is broken down into three primary types. These are commonly referred to as 2-wire, 3-wire and I2C synchronous cards. Each card type requires different control and timing and therefore requires different algorithms to access. Teridian has created an application note to provide detailed algorithms for each card type. Refer to the application note titled "*73S12xxF Synchronous Card Design Application Note*".

1.7.16 VDD Fault Detect Function

The 73S1210F contains a circuit to detect a low-voltage condition on the supply voltage V_{DD}. If enabled, it will deactivate the active internal smart card interface when V_{DD} falls below the V_{DD} Fault threshold. The register configures the V_{DD} Fault threshold for the nominal default of 2.3V* or a user selectable threshold. The user's code may load a different value using the FOVRVDDF bit = 1 after the power-up cycle has completed.

VDDFault Control Register (VDDFCtl): 0xFFD4 ← 0x00

Table 108: The VDDFCtl Register

MSB LSB

–	FOVRVDDF	VDDFLTEN	–	STXDAT.3	VDDFTH.2	VDDFTH.1	VDDFTH.0

Bit	Symbol	Function
VDDFCtl.7	–	
VDDFCtl.6	FOVRVDDF	Setting this bit high will allow the VDDFLT(2:0) bits set in this register to control the VDDFault threshold. When this bit is set low, the VDDFault threshold will be set to the factory default setting of 2.3V*.
VDDFCtl.5	VDDFLTEN	Set = 1 will disable VDD Fault operation.
VDDFCtl.4	–	
VDDFCtl.3	–	
VDDFCtl.2	VDDFTH.2	VDD Fault Threshold. Bit Value(2:0) VDDFault Voltage 000 2.3 (nominal default) 001 2.4 010 2.5 011 2.6 100 2.7 101 2.8 110 2.9 111 3.0
VDDFCtl.1	VDDFTH.1	
VDDFCtl.0	VDDFTH.0	

* Note: The V_{DD} Fault factory default can be set to any threshold as defined by bits VDDFTH(2:0). The 73S1210F has the capability to burn fuses at the factory to set the factory default to any of these voltages. Contact Teridian for further details.

3.6 Smart Card Interface Requirements

Symbol	Parameter	Condition	Min	Typ.	Max	Unit
Card Power Supply (V_{CC}) Regulator General conditions, -40°C < T < 85°C, 4.75V < V_{PC} < 6.0V, 2.7V < V_{DD} < 3.6V						
V_{CC}	Card supply Voltage including ripple and noise	Inactive mode	-0.1		0.1	V
		Inactive mode, I_{CC} = 1mA	-0.1		0.4	V
		Active mode; I_{CC} <65mA; 5V	4.65		5.25	V
		Active mode; I_{CC} < 65mA; 3V	2.85		3.15	V
		Active mode; I_{CC} < 40mA; 1.8V	1.68		1.92	V
		Active mode; single pulse of 100mA for 2μs; 5V, fixed load = 25mA	4.6		5.25	V
		Active mode; single pulse of 100mA for 2μs; 3V, fixed load = 25mA	2.76		3.15	V
		Active mode; current pulses of 40nAs with peak $\|I_{CC}\|$ <200mA, t <400ns; 5V	4.6		5.25	V
		Active mode; current pulses of 40nAs with peak $\|I_{CC}\|$ <200mA,t <400ns; 3V	2.7		3.15	V
		Active mode; current pulses of 20nAs with peak $\|I_{CC}\|$ <100mA,t <400ns; 1.8V	1.62		1.92	V
V_{CCrip}	V_{CC} Ripple	f_{RIPPLE} = 20kHz – 200MHz			350	mV
I_{CCmax}	Card supply output current	Static load current, V_{CC}>1.65			40	mA
		Static load current, V_{CC}>4.6V or 2.7V as selected			65	mA
I_{CCF}	I_{CC} fault current	Class A, B (5V and 3V)	100		180	mA
		Class C (1.8V)	60		130	
Isc	Maximum current prior to shut-down	Load current limit prior to Vcc shut-down	80		150	mA.
		Load current limit prior to Vcc shut-down for Vcc = 1.8V	60		130	mA
V_{SR}	Vcc slew rate, rise	Rise rate on activate C = 0.47μF	0.12	.30	0.50	V/μs
V_{SF}	Vcc slew rate, fall	Fall rate on deactivate, C = 0.47μF	0.15	.30	1.20	V/μs
V_{rdy}	Vcc ready voltage (VCCOK = 1)	5V operation, Vcc rising	4.6			V
		3V operation, Vcc rising	2.75			V
		1.8V operation, Vcc rising	1.65			V

5 Package Pin Designation

5.1 68-pin QFN Pinout

CAUTION: Use handling procedures necessary for a static sensitive component

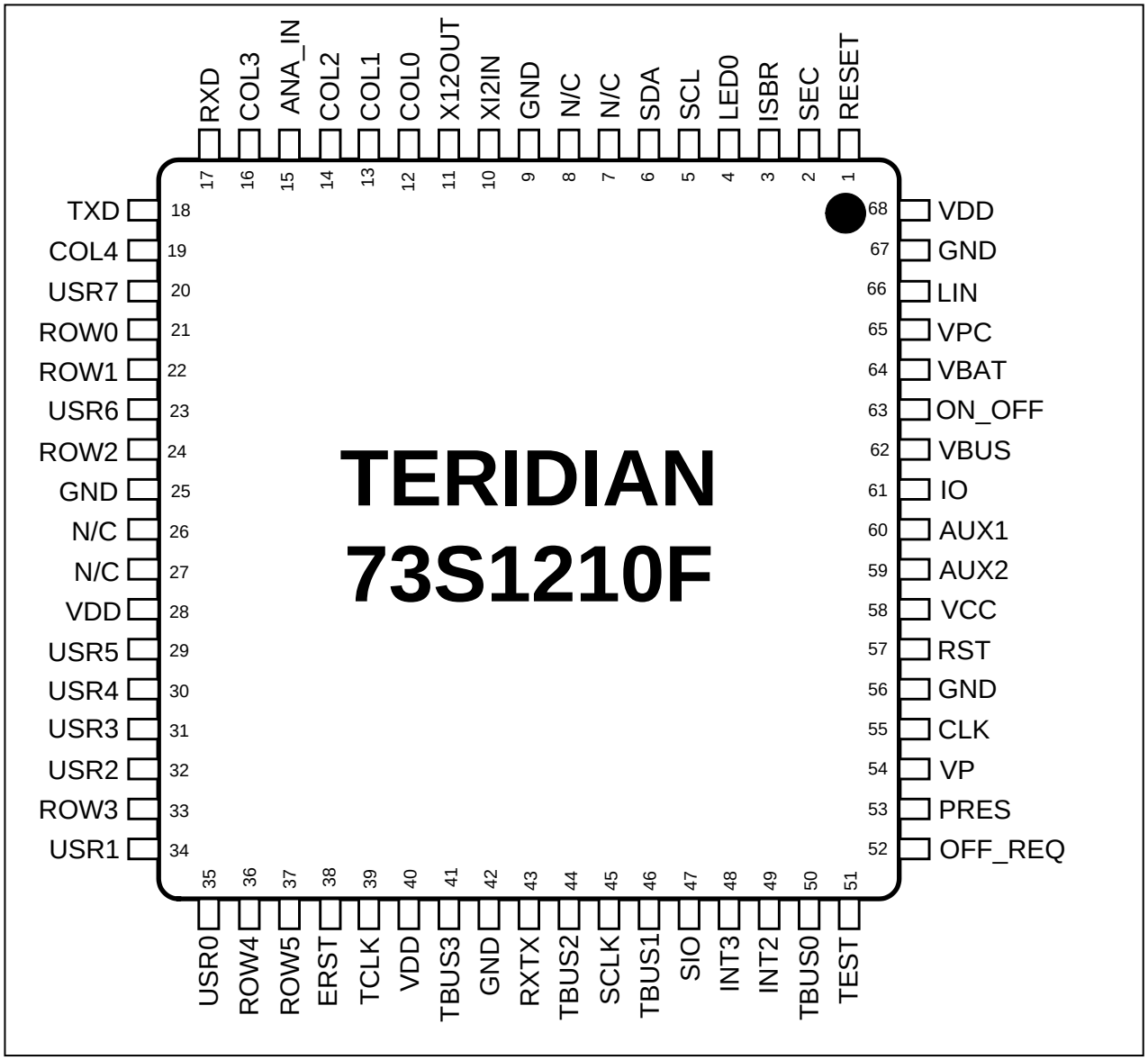


Figure 44: 73S1210F 68 QFN Pinout

5.2 44-pin QFN Pinout

CAUTION: Use handling procedures necessary for a static sensitive component.

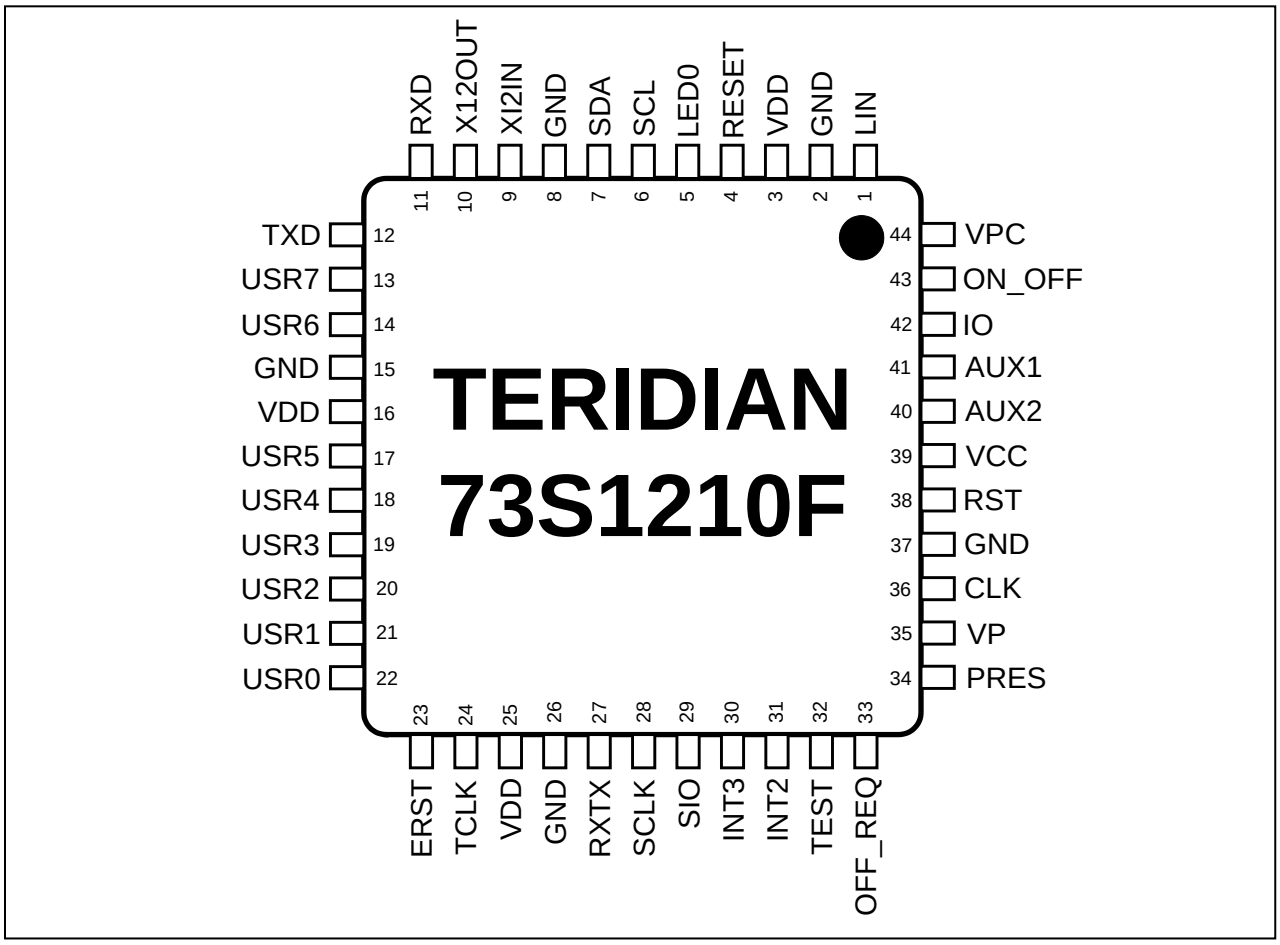


Figure 45: 73S1210F 44 QFN Pinout

		In Section 1.7.15.5, deleted "The ETU clock is held in reset condition until the activation sequence begins (either by VCCOK=1 or VCCTMR timeout) and will go high ½ the ETU period thereafter." In Section 1.7.15.5, added "Synchronous card operation is broken down into three primary types. These are commonly referred to as 2-wire, 3-wire and I2C synchronous cards. Each card type requires different control and timing and therefore requires different algorithms to access. Teridian has created an application note to provide detailed algorithms for each card type. Refer to the application note titled *73S12xxF Synchronous Card Design Application Note*." In Table 78 and Table 107, changed the SYCKST bit to I2CMODE. In Figure 25, replaced the schematic with a new schematic. In Section 3.4, changed the Fxtal Min from 4 to 6. Added 44-pin QFN package. Added Section 8, Related Documentation. Added Section 9, Contact Information. Formatted the document per new standard. Added section numbering.
1.3	1/22/2009	Changed the value for the I_{DD_IN} Power Down (25°C) parameter from 13 µA to 15 µA.
1.4	5/12/2009	In Table 1, corrected the 44 QFN GND pin from 37 to 26. Added the "with Programming" ordering numbers to Table 109.

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