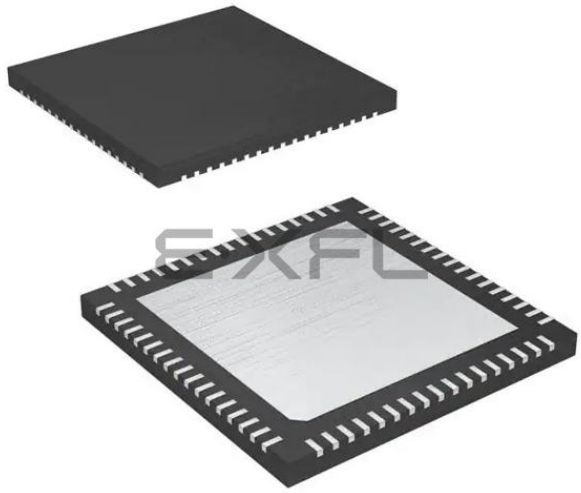
Analog Devices Inc./Maxim Integrated - 73S1210F-68IMR/F/P Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	80515
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SmartCard, UART/USART
Peripherals	LED, POR, WDT
Number of I/O	8
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/73s1210f-68imr-f-p

FEATURES

80515 Core:

- 1 clock cycle per instruction (most instructions)
- CPU clocked up to 24MHz
- 32KB Flash memory (lockable)
- 2kB XRAM (User Data Memory)
- 256 byte IRAM
- Hardware watchdog timer

Oscillators:

- Single low-cost 6MHz to 12MHz crystal
- An Internal PLL provides all the necessary clocks to each block of the system

Interrupts:

- Standard 80C515 4-priority level structure
- 9 different sources of interrupt to the core

Power Down Modes:

- 2 standard 80C515 Power Down and IDLE modes
- Sub-μA OFF mode
- ON/OFF Main System Power Switch:
- Input for an SPST momentary switch to ground

Timers:

- (2) Standard 80C52 timers T0 and T1
- (1) 16-bit timer

Built-in ISO-7816 Card Interface:

- Linear regulator produces VCC for the card (1.8V, 3V or 5V)
- Full compliance with EMV 4.1
- Activation/Deactivation sequencers
- Auxiliary I/O lines (C4 and C8 signals)
- 7kV ESD protection on all interface pins

Communication with Smart Cards:

- ISO 7816 UART 9600 to 115kbps for T=0, T=1
- (2) 2-Byte FIFOs for transmit and receive
- Configured to drive multiple external Teridian 73S8010x interfaces (for multi-SAM architectures)

Voltage Detection:

- Analog Input (detection range: 1.0V to 2.5V)

Communication Interfaces:

- Full-duplex serial interface (1200 to 115kbps UART)
- I^2C Master Interface (400kbps)
- Man-Machine Interface and I/Os:
- 6x5 Keyboard (hardware scanning, debouncing and scrambling)
- (8) User I/Os
- Single programmable current output (LED)
- Operating Voltage:
- Single supply 2.7V to 6.5V operation (VPC)
- 5V supply (VBUS 4.4V to 5.5V) with or without battery back up operation (VBAT 4.0V to 6.5V)
- Automated detection of voltage presence - Priority on VBUS over VBAT

DC-DC Converter:

- Requires a single 10μH Inductor
- 3.3V / 20mA supply available for external circuits

Operating Temperature:

- -40°C to 85°C

Package:

- 68-pin QFN, 44 pin QFN

Turnkey Firmware:

- Compliant with PC/SC, ISO7816 and EMV4.1 specifications
- Features a Power Down mode accessible from the host
- Supports Plug & Play over serial interface
- Windows® XP driver available (*)
- Windows CE / Mobile driver available (*)
- Linux and other OS: Upon request
- Or for custom developments:
  - A complete set of ISO-7816, EMV4.1 and low-level libraries are available for T=0 / T=1
  - Two-level Application Programming Interface (ANSI C-language libraries)

(*) Contact Teridian Semiconductor for conditions and availability.

1 Hardware Description

1.1 Pin Description

Table 1: 73S1210 Pinout Description

Pin Name	Pin (68 QFN)	Pin (44 QFN)	Type	Equivalent Circuit*	Description
X12IN	10	9	I	Figure 26	MPU clock crystal oscillator input pin. A 1MΩ resistor is required between pins X12IN and X12OUT.
X12OUT	11	10	O	Figure 26	MPU clock crystal oscillator output pin.
ROW(5:0) 0 1 2 3 4 5	 21 22 24 33 36 37		I	Figure 34	Keypad row input sense.
COL(4:0) 0 1 2 3 4	 12 13 14 16 19		O	Figure 35	Keypad column output scan pins.
USR(7:0) 0 1 2 3 4 5 6 7	 35 34 32 31 30 29 23 20	 22 21 20 19 18 17 14 13	IO	Figure 30	General-purpose user pins, individually configurable as inputs or outputs or as external input interrupt ports.
SCL	5	6	O	Figure 29	I^2C (master mode) compatible Clock signal. Note: the pin is configured as an open drain output. When the I2C interface is being used, an external pull up resistor is required. A value of 3K is recommended.
SDA	6	7	IO	Figure 28	I^2C (master mode) compatible data I/O. Note: this pin is bi-directional. When the pin is configured as output, it is an open drain output. When the I2C interface is being used, an external pull up resistor is required. A value of 3K is recommended.
RXD	17	11	I	Figure 32	Serial UART Receive data pin.
TXD	18	12	O	Figure 29	Serial UART Transmit data pin.
INT3	48	30	I	Figure 32	General purpose interrupt input.
INT2	49	31	I	Figure 32	General purpose interrupt input.
SIO	47	29	IO	Figure 28	IO data signal for use with external Smart Card interface circuit such as 73S8010.
SCLK	45	28	O	Figure 29	Clock signal for use with external Smart Card interface circuit.

Table 5: Program Security Registers

Register	SFR Address	R/W	Description
FLSHCTL	0xB2	R/W	Bit 0 (FLSH_PWE): Program Write Enable: 0 – MOVX commands refer to XRAM Space, normal operation (default). 1 – MOVX @DPTR,A moves A to Program Space (Flash) @ DPTR. This bit is automatically reset after each byte written to flash. Writes to this bit are inhibited when interrupts are enabled.
		W	Bit 1 (FLSH_MEEN): Mass Erase Enable: 0 – Mass Erase disabled (default). 1 – Mass Erase enabled. Must be re-written for each new Mass Erase cycle.
		R/W	Bit 6 (SECURE): Enables security provisions that prevent external reading of flash memory and CE program RAM. This bit is reset on chip reset and may only be set. Attempts to write zero are ignored.
TRIMPCtl	0xFFD1	W	0x54 value will set up for security fuse control. All other values are reserved and should not be used.
FUSECtl	0xFFD2	W	0xA6 value will cause the selected fuse to be blown. All other values will stop the burning process.
SECReg	0xFFD7	W	Bit 7 (PARAMSEC): 0 – Normal operation. 1 – Enable permanent programming of the security fuses.
		R	Bit 5 (SECPIN): Indicates the state of the SEC pin. The SEC pin is held low by a pull-down resistor. The user can force this pin high during boot sequence time to indicate to firmware that sec mode 1 is desired.
		R/W	Bit 1 (SECSET1): See the Program Security section.
		R/W	Bit 0 (SECSET0): See the Program Security section.

1.5.2 IRAM Special Function Registers (Generic 80515 SFRs)

Table 7 shows the location of the SFRs and the value they assume at reset or power-up.

Table 7: IRAM Special Function Registers Reset Values

Name	Location	Reset Value	Description
SP	0x81	0x07	Stack Pointer
DPL	0x82	0x00	Data Pointer Low 0
DPH	0x83	0x00	Data Pointer High 0
DPL1	0x84	0x00	Data Pointer Low 1
DPH1	0x85	0x00	Data Pointer High 1
WDTREL	0x86	0x00	Watchdog Timer Reload register
PCON	0x87	0x00	Power Control
TCON	0x88	0x00	Timer/Counter Control
TMOD	0x89	0x00	Timer Mode Control
TL0	0x8A	0x00	Timer 0, low byte
TL1	0x8B	0x00	Timer 1, high byte
TH0	0x8C	0x00	Timer 0, low byte
TH1	0x8D	0x00	Timer 1, high byte
MCLKCtl	0x8F	0x0A	Master Clock Control
USR70	0x90	0xFF	User Port Data (7:0)
UDIR70	0x91	0xFF	User Port Direction (7:0)
DPS	0x92	0x00	Data Pointer Select Register
ERASE	0x94	0x00	Flash Erase
S0CON	0x98	0x00	Serial Port 0, Control Register
S0BUF	0x99	0x00	Serial Port 0, Data Buffer
IEN2	0x9A	0x00	Interrupt Enable Register 2
S1CON	0x9B	0x00	Serial Port 1, Control Register
S1BUF	0x9C	0x00	Serial Port 1, Data Buffer
S1RELL	0x9D	0x00	Serial Port 1, Reload Register, low byte
IEN0	0xA8	0x00	Interrupt Enable Register 0
IP0	0xA9	0x00	Interrupt Priority Register 0
S0RELL	0xAA	0xD9	Serial Port 0, Reload Register, low byte
FLSHCTL	0xB2	0x00	Flash Control
PGADDR	0xB7	0x00	Flash Page Address
IEN1	0xB8	0x00	Interrupt Enable Register 1
IP1	0xB9	0x00	Interrupt Priority Register 1
S0RELH	0xBA	0x03	Serial Port 0, Reload Register, high byte
S1RELH	0xBB	0x03	Serial Port 1, Reload Register, high byte
IRCON	0xC0	0x00	Interrupt Request Control Register
T2CON	0xC8	0x00	Timer 2 Control
PSW	0xD0	0x00	Program Status Word
KCOL	0XD1	0x1F	Keypad Column

All ports on the chip are bi-directional. Each consists of a Latch (SFR 'USR70'), an output driver, and an input buffer, therefore the MPU can output or read data through any of these ports if they are not used for alternate purposes.

1.6 Instruction Set

All instructions of the generic 8051 microcontroller are supported. A complete list of the instruction set and of the associated op-codes is contained in the *73S12xxF Software User's Guide*.

1.7 Peripheral Descriptions

1.7.1 Oscillator and Clock Generation

The 73S1210F has one oscillator circuit for the main CPU clock. The main oscillator circuit is designed to operate with various crystal or external clock frequencies. An internal divider working in conjunction with a PLL and VCO provides a 96MHz internal clock within the 73S1210F. 96 MHz is the recommended frequency for proper operation of specific peripheral blocks such as the specific timers, ISO 7816 UART and interfaces, Step-up converter, and keypad. The clock generation and control circuits are shown in Figure 3.

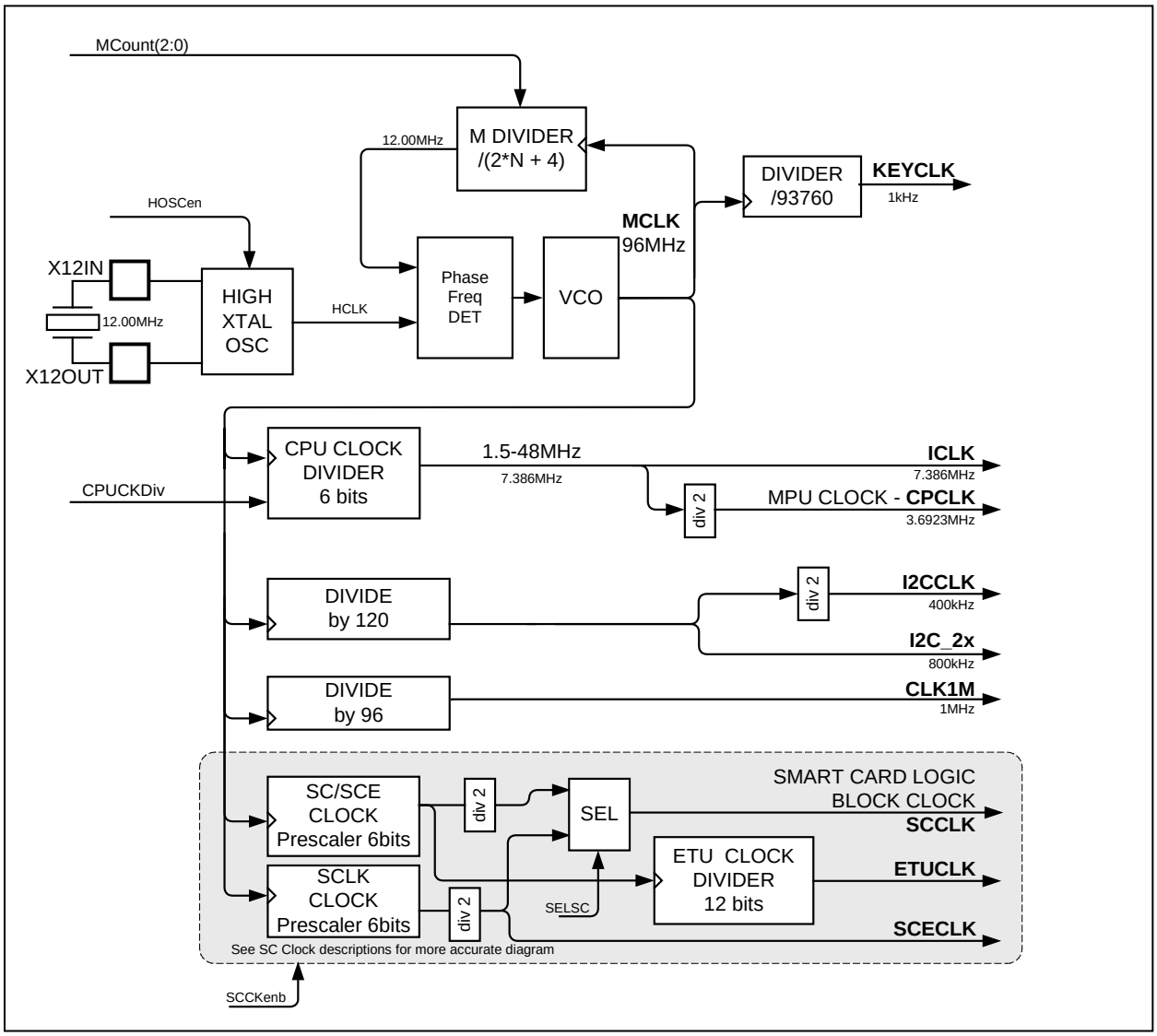


Figure 3: Clock Generation and Control Circuits

V_{BAT} is expected to be supplied from a battery of three to four series connected cells with a voltage value of 4.0 to 6.5 volts.

V_{BAT} and V_{BUS} are internally switched to V_{PC} by two separate FET switches configured as a SPDT switch (break-before-make). They will not be enabled at the same time. V_{BUS} is automatically selected in lieu of V_{BAT} when V_{BUS} is present (i.e. V_{BUS} always has the priority).

If V_{PC} is provided and either V_{BAT} or V_{BUS} is also used, the source of V_{PC} must be diode isolated from the V_{PC} pin to prevent current flow from V_{BAT} or V_{BUS} into the V_{PC} source.

The power that is supplied to the V_{PC} pin (externally or internally, i.e. through V_{BAT} or V_{BUS} – see above) is up-converted to the intermediate voltage V_P utilizing an inductive, step-up converter. A series power inductor (nominal value = 10 μH) must be connected from V_{PC} to the pin LIN, and a 10μF low ESR filter capacitor must be connected to V_{PC}.

V_P requires a 4.7μF filter capacitor and will have a nominal value of 5.5 volts during normal operation. V_P is used internally by the smart card electrical interface circuit and is regulated to the desired smart card supply V_{CC} voltage (can be programmed for values of 5V, 3V, or 1.8V).

V_P is also used internally to generate a 3.3V nominal, regulated power supply V_{DD}. V_{DD} is output on pin 68 and must be directly tied to all other V_{DD} pins on the 73S1210F (pins 28 and 40). V_{DD} powers all the digital logic, input/output buffering, and analog functions. It can also be used for external circuitry: up to 20mA current can be supplied to external devices simultaneously to the 73S1210F's digital core maximum consumption.

1.7.3 Power ON/OFF

The 73S1210F features an ON_OFF input pin for a momentary contact, main-system ON/OFF switch. The purpose of this switch is to place the circuit in a very low-power mode – the "OFF" mode – where all circuits are no longer powered, therefore allowing the lowest possible current consumption.

When in "OFF" mode, an action on the ON/OFF switch will turn-on the power supply of the digital core (V_{DD}) and apply a power-on-reset condition. Alternatively, entering the "OFF" mode from the "ON" mode requires firmware action.

When in "ON" mode, an action on the ON/OFF switch will send a request to the controller that will have to be acknowledged (firmware action required) in order to enter the "OFF" state.

When placed into the "OFF" state, the 73S1210F will consume minimum current from V_{PC} and V_{BAT}; V_P and V_{DD} will be unavailable (V_{DD} out = 0V and V_P = 0V).

When in "ON" mode, the 73S1210F will operate normally, with all the features described in this document available. V_P and V_{DD} will be available (V_{DD} out = 3.3V and V_P = 5.5V nominal).

Whenever V_{BUS} power is supplied, the circuit will be automatically in the "ON" state. The functions of the ON/OFF switch and circuitry are overridden and the 73S1210F is in the "ON" state with V_P and V_{DD} available.

Without V_{BUS} applied, the circuit is by default in the "OFF" state, and will respond only to the ON_OFF pin. The ON_OFF pin should be connected to an SPST switch to ground. If the circuit is OFF and the switch is closed for a debounce period of 50-100ms, the circuit will go into the "ON" state wherein all functions are operating in normal fashion. If the circuit is in the "ON" state and the ON/OFF pin is connected to ground for a period greater than the debounce period, OFF_REQ will be asserted high and held regardless of the state of ON/OFF. The OFF_REQ signal should be connected to one of the interrupt pins to signal the CPU core that a request to shutdown has been initiated. The firmware will acknowledge this request by setting the SCPWRDN bit in the Smart Card V_{CC} Control/Status Register (VccCtl) high after it has completed all shutdown activities. When SCPWRDN is set high, the circuit will deactivate the smart card interface if required and turn off all analog functions and the V_{DD} supply for the logic and companion circuits. The default state upon application of power is the "OFF" state unless power is supplied to the V_{BUS} supply. Note that at any time, the firmware may assert SCPWRDN and the

Miscellaneous Control Register 1 (MISCtl1): 0xFFF2 ← 0x10

Table 16: The MISCtl1 Register

MSB							LSB
–	–	FRPEN	FLSH66	–	–	–	–

Bit	Symbol	Function
MISCtl1.7	–	
MISCtl1.6	–	
MISCtl1.5	FRPEN	Flash Read Pulse enable (low). If FRPEN = 1, the Flash Read signal is passed through with no change. When FRPEN = 0 a one-shot circuit that shortens the Flash Read signal is enabled to save power. The Flash Read pulse will shorten to 40 or 66ns (approximate based on the setting of the FLSH66 bit) in duration, regardless of the MPU clock rate. For MPU clock frequencies greater than 10MHz, this bit should be set high.
MISCtl1.4	FLSH66	When high, creates a 66ns Flash read pulse, otherwise creates a 40ns read pulse when FRPEN is set.
MISCtl1.3	–	
MISCtl1.2	–	
MISCtl1.1	–	
MISCtl1.0	–	

Master Clock Control Register (MCLKCtl): 0x8F ← 0x0A

Table 17: The MCLKCtl Register

MSB							LSB
HSOEN	KBEN	SCEN	–	–	MCT.2	MCT.1	MCT.0

Bit	Symbol	Function
MCLKCtl.7	HSOEN*	High-speed oscillator enable. When set = 1, disables the high-speed crystal oscillator and VCO/PLL system. This bit is not changed when the PWRDN bit is set but the oscillator/VCO/PLL is disabled.
MCLKCtl.6	KBEN	1 = Disable the keypad logic clock. This bit is not changed in PWRDN mode but the function is disabled.
MCLKCtl.5	SCEN	1 = Disable the smart card logic clock. This bit is not changed in PWRDN mode but the function is disabled. Interrupt logic for card insertion/removal remains operable even with smart card clock disabled.
MCLKCtl.4	–	
MCLKCtl.3	–	
MCLKCtl.2	MCT.2	This value determines the ratio of the VCO frequency (MCLK) to the high-speed crystal oscillator frequency such that: MCLK = (MCount*2 + 4)*Fxtal. The default value is MCount = 2h such that MCLK = (2*2 + 4)*12.00MHz = 96MHz.
MCLKCtl.1	MCT.1	
MCLKCtl.0	MCT.0	

*Note: The HSOEN bit should never be set under normal circumstances. Power down control should only be initiated via use of the PWRDN bit in MISCtl0.

Interrupt Priority 1 Register (IP1): 0xB9 ← 0x00

Table 29: The IP1 Register

MSB							LSB
–	–	IP1.5	IP1.4	IP1.3	IP1.2	IP1.1	IP1.0

Table 30: Priority Levels

IP1.x	IP0.x	Priority Level
0	0	Level0 (lowest)
0	1	Level1
1	0	Level2
1	1	Level3 (highest)

Table 31: Interrupt Polling Sequence

External interrupt 0	Polling sequence
Serial channel 1 interrupt	
Timer 0 interrupt	
External interrupt 2	
External interrupt 1	
External interrupt 3	
Timer 1 interrupt	
Serial channel 0 interrupt	
External interrupt 4	
External interrupt 5	
External interrupt 6	

1.7.5.6 Interrupt Sources and Vectors

Table 32 shows the interrupts with their associated flags and vector addresses.

Table 32: Interrupt Vectors

Interrupt Request Flag	Description	Interrupt Vector Address
N/A	Chip Reset	0x0000
IE0	External interrupt 0	0x0003
TF0	Timer 0 interrupt	0x000B
IE1	External interrupt 1	0x0013
TF1	Timer 1 interrupt	0x001B
RI0/TI0	Serial channel 0 interrupt	0x0023
RI1/TI1	Serial channel 1 interrupt	0x0083
IEX2	External interrupt 2	0x004B
IEX3	External interrupt 3	0x0053
IEX4	External interrupt 4	0x005B
IEX5	External interrupt 5	0x0063
IEX6	External interrupt 6	0x006B

1.7.8 WD Timer (Software Watchdog Timer)

The software watchdog timer is a 16-bit counter that is incremented once every 24 or 384 clock cycles. After a reset, the watchdog timer is disabled and all registers are set to zero. The watchdog consists of a 16-bit counter (WDT), a reload register (WDTREL), prescalers (by 2 and by 16), and control logic. Once the watchdog starts, it cannot be stopped unless the internal reset signal becomes active.

WD Timer Start Procedure: The WDT is started by setting the SWDT flag. When the WDT register enters the state 0x7CFF, an asynchronous WDTS signal will become active. The signal WDTS sets bit 6 in the IP0 register and requests a reset state. WDTS is cleared either by the reset signal or by changing the state of the WDT timer.

Refreshing the WD Timer: The watchdog timer must be refreshed regularly to prevent the reset request signal from becoming active. This requirement imposes an obligation on the programmer to issue two instructions. The first instruction sets WDT and the second instruction sets SWDT. The maximum delay allowed between setting WDT and SWDT is 12 clock cycles. If this period has expired and SWDT has not been set, WDT is automatically reset, otherwise the watchdog timer is reloaded with the content of the WDTREL register and WDT is automatically reset.

Interrupt Enable 0 Register (IEN0): 0xA8 ← 0x00

Table 43: The IEN0 Register

MSB							LSB
EAL	WDT	ET2	ES0	ET1	EX1	ET0	EX0

Bit	Symbol	Function
IEN0.7	EAL	EAL = 0 – disable all interrupts.
IEN0.6	WDT	Watchdog timer refresh flag. Set to initiate a refresh of the watchdog timer. Must be set directly before SWDT is set to prevent an unintentional refresh of the watchdog timer. WDT is reset by hardware 12 clock cycles after it has been set.
IEN0.5	–	
IEN0.4	ES0	ES0 = 0 – disable serial channel 0 interrupt.
IEN0.3	ET1	ET1 = 0 – disable timer 1 overflow interrupt.
IEN0.2	EX1	EX1 = 0 – disable external interrupt 1.
IEN0.1	ET0	ET0 = 0 – disable timer 0 overflow interrupt.
IEN0.0	EX0	EX0 = 0 – disable external interrupt 0.

1.7.9 User (USR) Ports

The 73S1210F includes 8 pins of general purpose digital I/O (GPIO). On reset or power-up, all USR pins are inputs until they are configured for the desired direction. The pins are configured and controlled by the USR70 and UDIR70 SFRs. Each pin declared as USR can be configured independently as an input or output with the bits of the UDIR70 register. Table 47 lists the direction registers and configurability associated with each group of USR pins. USR pins 0 to 7 are multiple use pins that can be used for general purpose I/O, external interrupts and timer control. Table 48 shows the configuration for a USR pin through its associated bit in its UDIR register. Values read from and written into the GPIO ports use the data registers USR70. Note: After reset, all USR pins are defaulted as inputs and pulled up to VDD until any write to the corresponding UDIR register is performed. This insures all USR pins are set to a known value until set by the firmware. Unused USR pins can be set for output if unused and unconnected to prevent them from floating. Alternatively, unused USR pins can be set for input and tied to ground or V_{DD}.

Table 47: Direction Registers and Internal Resources for DIO Pin Groups

USR Pin Group	Type	Direction Register Name	Direction Register (SFR) Location	Data Register Name	Data Register (SFR) Location
USR_0…USR_7	Multi-use	UDIR70	0x91 [7:0]	USR70	0x90 [7:0]

Table 48: UDIR Control Bit

	UDIR Bit	
	0	1
USR Pin Function	output	input

Four XRAM SFR registers (USRIntTCtl0, USRIntTCtl1, USRIntTCtl2, and USRIntTCtl3) control the use of the USR [7:0] pins. Each of the USR [7:0] pins can be configured as GPIO or individually be assigned an internal resource such as an interrupt or a timer/counter control. Each of the four registers contains two 3-bit configuration words named UxIS (where x corresponds to the USR pin). The control resources selectable for the USR pins are listed in Table 50 through Table 53. If more than one input is connected to the same resource, the resources are combined using a logical OR.

Table 49: Selectable Controls Using the UxIS Bits

UxIS Value	Resource Selected for USRx Pin
0	None
1	None
2	T0 (counter0 gate/clock)
3	T1 (counter1 gate/clock)
4	Interrupt 0 rising edge/high level on USRx
5	Interrupt 1 rising edge/high level on USRx
6	Interrupt 0 falling edge/low level on USRx
7	Interrupt 1 falling edge/low level on USRx

Note: x denotes the corresponding USR pin. Interrupt edge or level control is assigned in the IT0 and IT1 bits in the TCON register.

Figure 11 shows the timing of the I²C read mode:

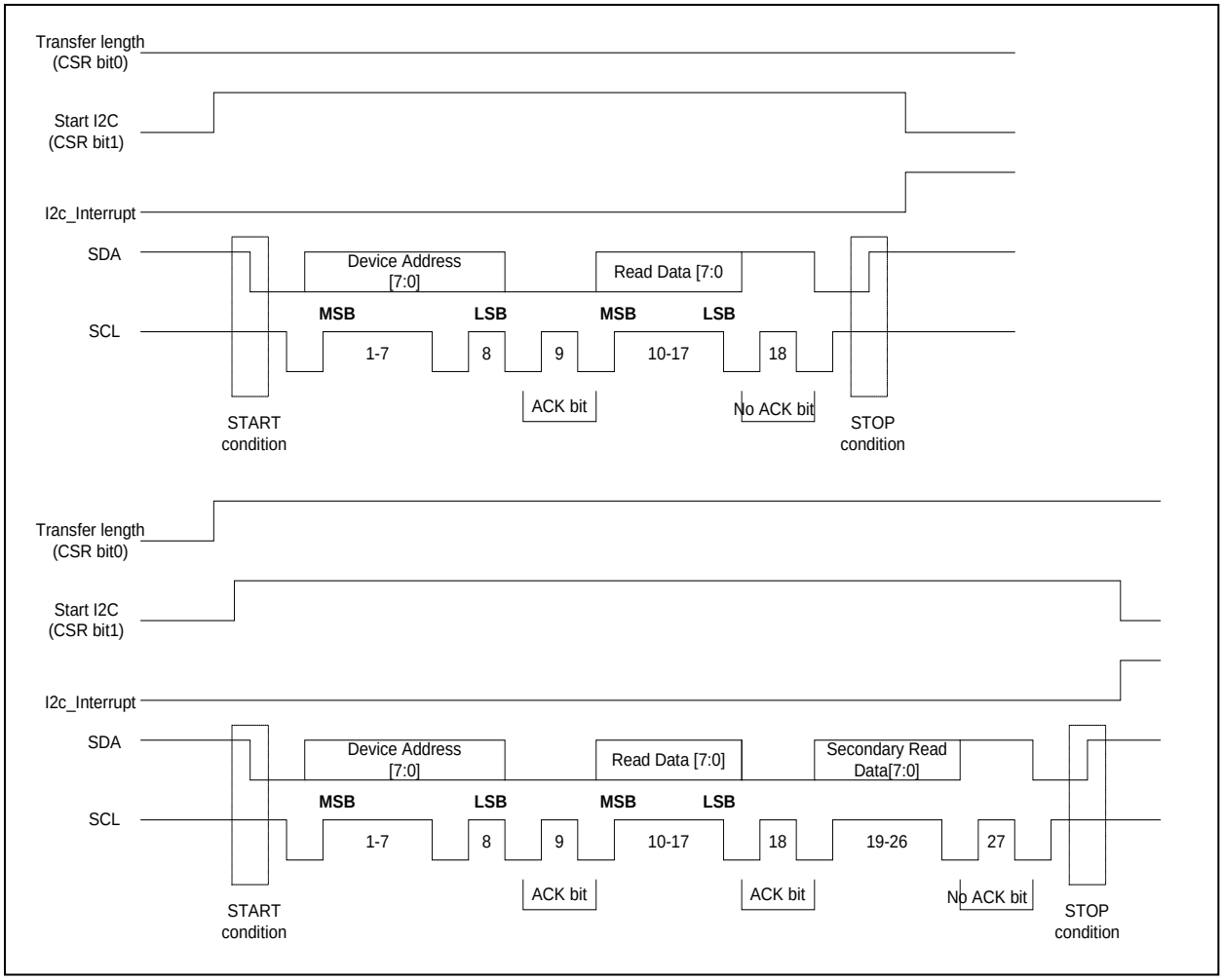


Figure 11: I²C Read Operation

Keypad Column LS Scan Order Register (KORDERL): 0xD6 ← 0x00

In the KORDERL and KORDERH registers, Column Scan Order(14:0) is grouped into 5 sets of 3 bits each. Each set determines which column (COL(4:0) pin) to activate by loading the column number into the 3 bits. When in HW_Scan_Enable mode, the hardware will step through the sets from 1Col to 5Col (up to the number of columns in Colsize) and scan the column defined in the 3 bits. To scan in sequential order, set a counting pattern with 0 in set 0, and 1 in set 1,and 2 in set 2, and 3 in set 3, and 4 in set 4. The firmware should update this as part of the interrupt service routine so that the new scan order is loaded prior to the next key being pressed. For example, to scan COL(0) first, 1Col(2:0) should be loaded with 000'b. To scan COL(4) fifth, 5Col(2:0) should be loaded with 100'b.

Table 69: The KORDERL Register

MSB							LSB
3COL.1	3COL.0	2COL.2	2COL.1	2COL.0	1COL.2	1COL.1	1COL.0

Bit	Symbol	Function
KORDERL.7	3COL.1	Column to scan 3rd (lsb's).
KORDERL.6	3COL.0	
KORDERL.5	2COL.2	Column to scan 2nd.
KORDERL.4	2COL.1	
KORDERL.3	2COL.0	
KORDERL.2	1COL.2	Column to scan 1st.
KORDERL.1	1COL.1	
KORDERL.0	1COL.0	

Keypad Column MS Scan Order Register (KORDERH): 0xD7 ← 0x00

Table 70: The KORDERH Register

MSB							LSB
–	5COL.2	5COL.1	5COL.0	4COL.2	4COL.1	4COL.0	3COL.2

Bit	Symbol	Function
KORDERH.7	–	
KORDERH.6	5COL.2	Column to scan 5th.
KORDERH.5	5COL.1	
KORDERH.4	5COL.0	
KORDERH.3	4COL.2	Column to scan 4th.
KORDERH.2	4COL.1	
KORDERH.1	4COL.0	
KORDERH.0	3COL.2	Column to scan 3rd (msb).

External Interrupt Control Register (INT5Ctl): 0xFF94 ← 0x00

Table 71: The INT5Ctl Register

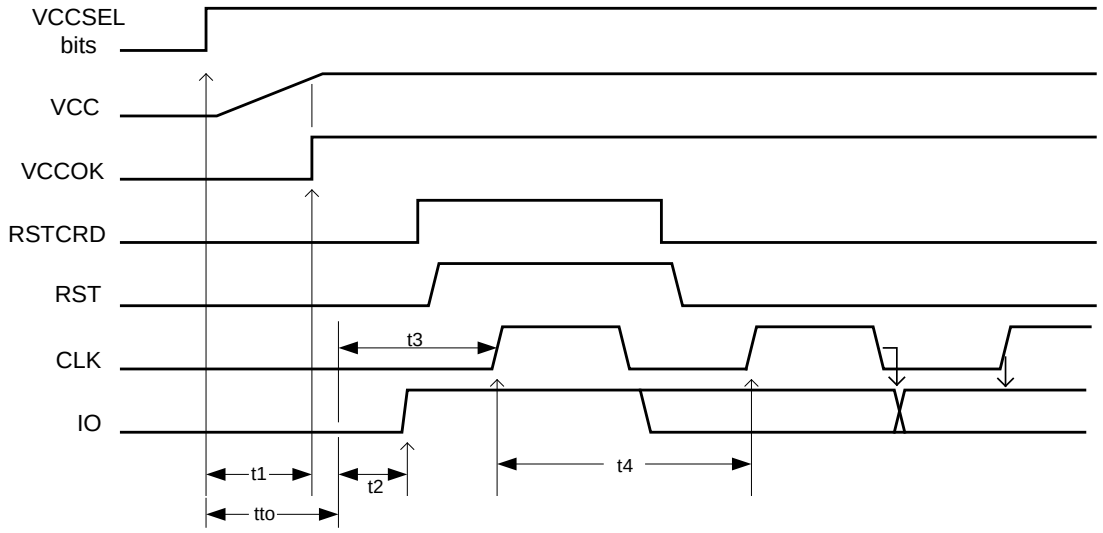
MSB							LSB
PDMUX	–	–	–	–	–	KPIEN	KPINT

Bit	Symbol	Function
INT5Ctl.7	PDMUX	Power down multiplexer control.
INT5Ctl.6	–	
INT5Ctl.5	–	
INT5Ctl.4	–	
INT5Ctl.3	–	
INT5Ctl.2	–	
INT5Ctl.1	KPIEN	Enables Keypad interrupt when set = 1.
INT5Ctl.0	KPINT	This bit indicates the Keypad logic has set Key_Detect bit and a key location may be read. Cleared on read of register.

1.7.14 Emulator Port

The emulator port, consisting of the pins E_RST, E_TCLK and E_RXTX, provides control of the MPU through an external in-circuit emulator. The E_TBUS[3:0] pins, together with the E_ISYNC/BRKRQ, add trace capability to the emulator. The emulator port is compatible with the ADM51 emulators manufactured by Signum Systems™.

The signals of the emulator port have weak pull-ups. Adding resistor footprints for signals E_RST, E_TCLK and E_RXTX on the PCB is recommended. If necessary, adding 10kΩ pull-up resistors on E_TCLK and E_RXTX and a 3kΩ on E_RST will help the emulator operate normally if a problem arises. If code trace capability is needed on this interface, 20pF capacitors ((to ground) need to be added to allow the trace function capability to run properly. These capacitors should be attached to the TBUS0:3 and ISBR signals.



t1: The time from setting VCCSEL bits until VCCOK = 1.

tto: The time from setting VCCSEL bits until VCCTMR times out. At t1 (if RDYST = 1) or tto (if RDYST = 0), activation starts. It is suggested to have RDYST = 0 and use the VCCTMR interrupt to let MPU know when sequence is starting.

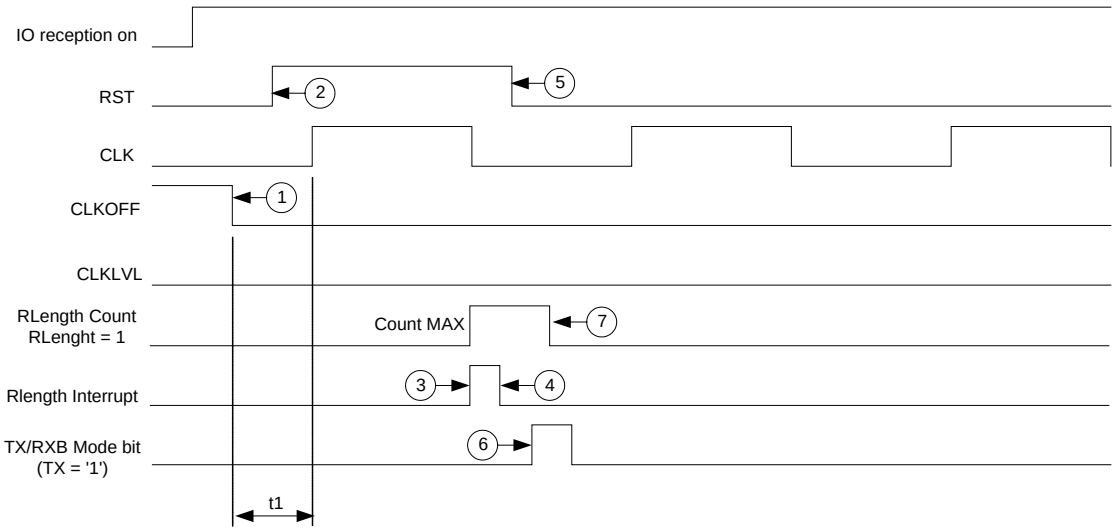
t2: time from start of activation (no external indication) until IO goes into reception mode (= 1). This is approximately 4 SCCLK (or SCECLK) clock cycles.

t3: minimum one half of ETU period.

t4: ETU period.

Note that in Sync mode, IO as input is sampled on the rising edge of CLK. IO changes on the falling edge of CLK, either from the card or from the 73S1210F. The RST signal to the card is directly controlled by the RSTCRD bit (non-inverted) via the MPU and is shown as an example of a possible RST pattern.

Figure 20: Synchronous Activation



1. Clear CLKOFF after Card is in reception mode.
2. Set RST bit.
3. Interrupt is generated when Rlength counter is MAX.
4. Read and clear Interrupt.
5. Clear RST bit.
6. Toggle TX/RXB to reset bit counter.
7. Reload RLength Counter.

t1. CLK wll start at least 1/2 ETU after CLKOFF is set low when CLKLVL = 0

Figure 21: Example of Sync Mode Operation: Generating/Reading ATR Signals

SC Clock Configuration Register (SCCLK): 0xFE0F ← 0x0C

This register controls the internal smart card (CLK) clock generation.

Table 86: The SCCLK Register

MSB							LSB
–	–	ICLKFS.5	ICLKFS.4	ICLKFS.3	ICLKFS.2	ICLKFS.1	ICLKFS.0

Bit	Symbol	Function
SCCLK.7	–	
SCCLK.6	–	
SCCLK.5	ICLKFS.5	Internal Smart Card CLK Frequency Select - Division factor to determine internal smart card CLK frequency. MCLK clock is divided by (register value + 1) to clock the ETU divider, and then by 2 to generate CLK. Default ratio is 13. The programmed value in this register is applied to the divider after this value is written, in such a manner as to produce a glitch-free output, regardless of the selection of active interface. A register value = 0 will default to the same effect as register value = 1.
SCCLK.4	ICLKFS.4	
SCCLK.3	ICLKFS.3	
SCCLK.2	ICLKFS.2	
SCCLK.1	ICLKFS.1	
SCCLK.0	ICLKFS.0	

External SC Clock Configuration Register (SCECLK): 0xFE10 ← 0x0C

This register controls the external smart card (SCLK) clock generation.

Table 87: The SCECLK Register

MSB							LSB
–	–	ECLKFS.5	ECLKFS.4	ECLKFS.3	ECLKFS.2	ECLKFS.1	ECLKFS.0

Bit	Symbol	Function
SCECLK.7	–	
SCECLK.6	–	
SCECLK.5	ECLKFS.5	External Smart Card CLK Frequency Select - Division factor to determine external smart card CLK frequency. MCLK clock is divided by (register value + 1) to clock the ETU divider, and then by 2 to generate SCLK. Default ratio is 13. The programmed value in this register is applied to the divider after this value is written, in such a manner as to produce a glitch-free output, regardless of the selection of active interface. A register value = 0 will default to the same effect as register value = 1.
SCECLK.4	ECLKFS.4	
SCECLK.3	ECLKFS.3	
SCECLK.2	ECLKFS.2	
SCECLK.1	ECLKFS.1	
SCECLK.0	ECLKFS.0	

Block Wait Time Registers (BWTB0): 0xFE1B ← 0x00, (BWTB1): 0xFE1A ← 0x00, (BWTB2): 0xFE19 ← 0x00, (BWTB3): 0xFE18 ← 0x00

These registers are used to set the Block Waiting Time(27:0) (BWT). All of these parameters define the maximum time the 73S1210F will have to wait for a character from the smart card. These registers serve a dual purpose. When T=1, these registers are used to set up the block wait time. The block wait time defines the time in ETUs between the beginning of the last character sent to smart card and the start bit of the first character received from smart card. It can be used to detect an unresponsive card and should be loaded by firmware prior to writing the last TX byte. When T=0, these registers are used to set up the work wait time. The work wait time is defined as the time between the leading edge of two consecutive characters being sent to or from the card. If a timeout occurs, an interrupt is generated to the firmware. The firmware can then take appropriate action. A Wait Time Extension (WTX) is supported with the 28-bit BWT.

Table 97: The BWTB0 Register

MSB							LSB
BWT.7	BWT.6	BWT.5	BWT.4	BWT.3	BWT.1	BWT.2	BWT.0

Table 98: The BWTB1 Register

MSB							LSB
BWT.15	BWT.14	BWT.13	BWT.12	BWT.11	BWT.10	BWT.9	BWT.8

Table 99: The BWTB2 Register

MSB							LSB
BWT.23	BWT.22	BWT.21	BWT.20	BWT.19	BWT.18	BWT.17	BWT.16

Table 100: The BWTB3 Register

MSB							LSB
–	–	–	–	BWT.27	BWT.26	BWT.25	BWT.24

Character Wait Time Registers (CWTB0): 0xFE1D ← 0x00, (CWTB1): 0xFE1C ← 0x00

These registers are used to hold the Character Wait Time(15:0) (CWT) or Initial Waiting Time(15:0) (IWT) depending on the situation. Both the IWT and the CWT measure the time in ETUs between the leading edge of the start of the current character received from the smart card and the leading edge of the start of the next character received from the smart card. The only difference is the mode in which the card is operating. When T=1 these registers are used to configure the CWT and these registers configure the IWT when the ATR is being received. These registers should be loaded prior to receiving characters from the smart card. Firmware must manage which time is stored in the register. If a timeout occurs, an interrupt is generated to the firmware. The firmware can then take appropriate action.

Table 101: The CWTB0 Register

MSB							LSB
CWT.7	CWT.6	CWT.5	CWT.4	CWT.3	CWT.1	CWT.2	CWT.0

Table 102: The CWTB1 Register

MSB							LSB
CWT.15	CWT.14	CWT.13	CWT.12	CWT.11	CWT.10	CWT.9	CWT.8

1.7.16 VDD Fault Detect Function

The 73S1210F contains a circuit to detect a low-voltage condition on the supply voltage V_{DD}. If enabled, it will deactivate the active internal smart card interface when V_{DD} falls below the V_{DD} Fault threshold. The register configures the V_{DD} Fault threshold for the nominal default of 2.3V* or a user selectable threshold. The user's code may load a different value using the FOVRVDDF bit = 1 after the power-up cycle has completed.

VDDFault Control Register (VDDFCtl): 0xFFD4 ← 0x00

Table 108: The VDDFCtl Register

MSB LSB

–	FOVRVDDF	VDDFLTEN	–	STXDAT.3	VDDFTH.2	VDDFTH.1	VDDFTH.0

Bit	Symbol	Function
VDDFCtl.7	–	
VDDFCtl.6	FOVRVDDF	Setting this bit high will allow the VDDFLT(2:0) bits set in this register to control the VDDFault threshold. When this bit is set low, the VDDFault threshold will be set to the factory default setting of 2.3V*.
VDDFCtl.5	VDDFLTEN	Set = 1 will disable VDD Fault operation.
VDDFCtl.4	–	
VDDFCtl.3	–	
VDDFCtl.2	VDDFTH.2	VDD Fault Threshold. Bit Value(2:0) VDDFault Voltage 000 2.3 (nominal default) 001 2.4 010 2.5 011 2.6 100 2.7 101 2.8 110 2.9 111 3.0
VDDFCtl.1	VDDFTH.1	
VDDFCtl.0	VDDFTH.0	

* Note: The V_{DD} Fault factory default can be set to any threshold as defined by bits VDDFTH(2:0). The 73S1210F has the capability to burn fuses at the factory to set the factory default to any of these voltages. Contact Teridian for further details.

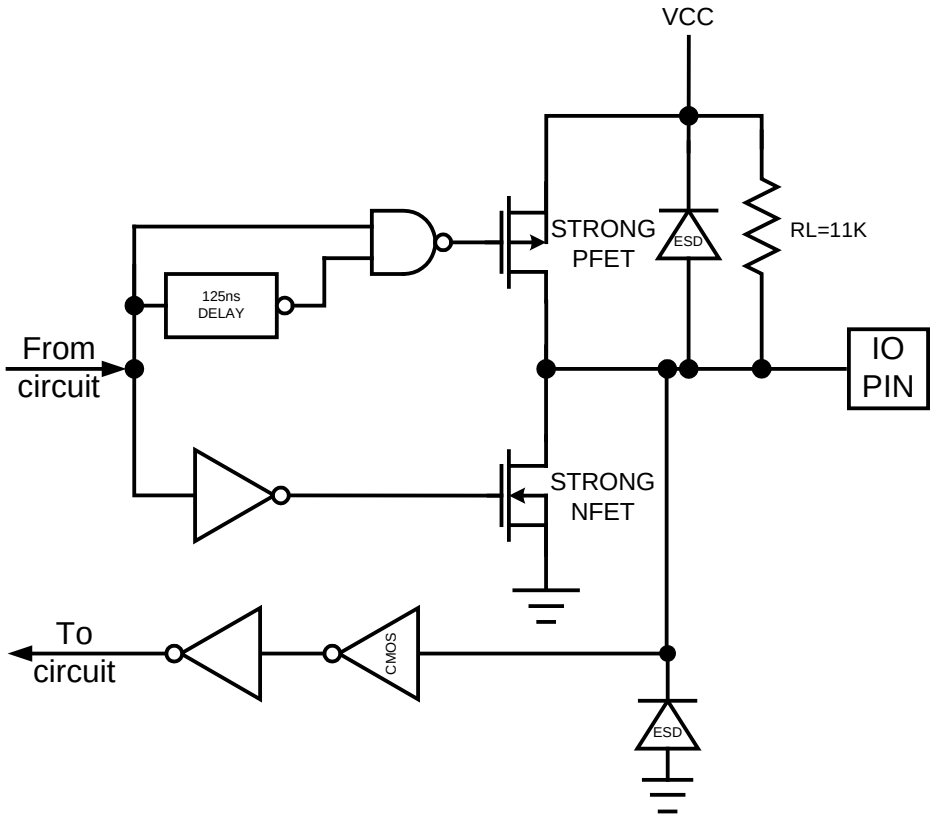


Figure 40: Smart Card I/O Circuit

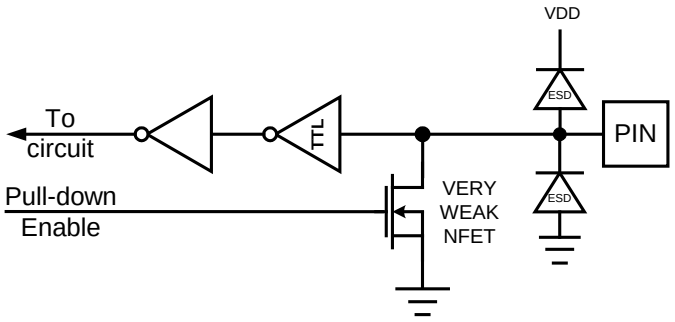


Figure 41: PRES Input Circuit

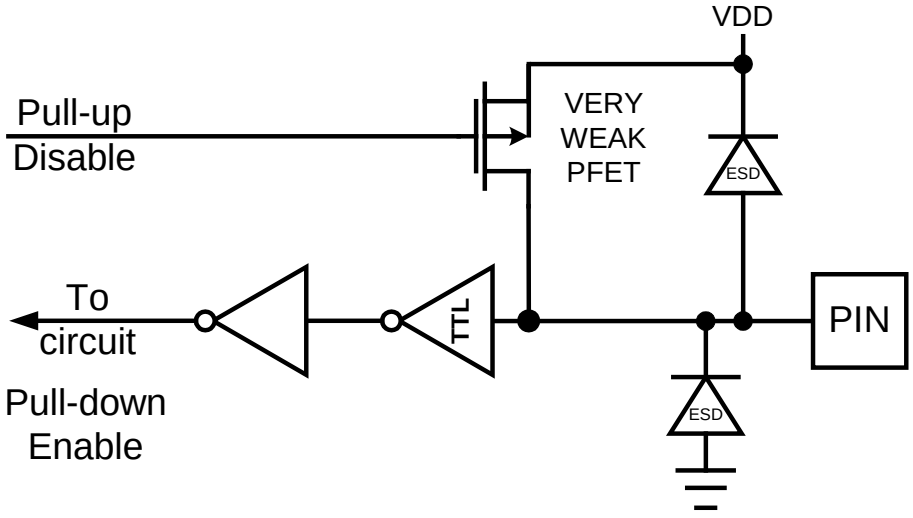


Figure 42: PRESB Input Circuit

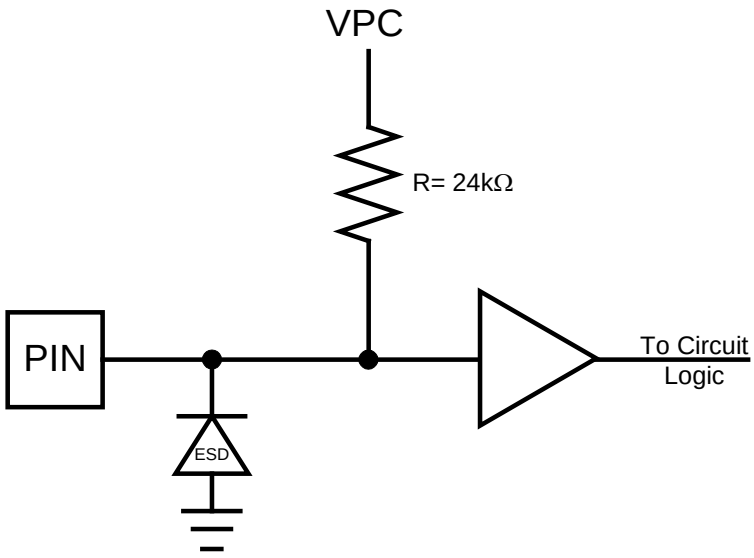


Figure 43: ON_OFF Input Circuit