$ %& ' ( )

$ # *% + *,

- - . *% +
*

- ,	.
$ -	%/ 0&0
$, #	%1
,	) 2 3#
$	4$, $ 5! 6 5, ! 6
-	7 8 -. 6 9 8
: .	%
- , #	( ) ; 1 <( ) ; * %=
-	>7! , 3
-6. , #	
6! , #	) ; * %
? , <? ? =	) @? A ' 0?
8 $	
.	
.	2/ B$ A %0B$ < ! =
	,
- $	' %?>C>: * -
, 8 -	' %C>: <%' %=
- 567	D * @(&) &/ ' % E

FEATURES

80515 Core:

- 1 clock cycle per instruction (most instructions)
- CPU clocked up to 24MHz
- 32KB Flash memory (lockable)
- 2kB XRAM (User Data Memory)
- 256 byte IRAM
- Hardware watchdog timer

Oscillators:

- Single low-cost 6MHz to 12MHz crystal
- An Internal PLL provides all the necessary clocks to each block of the system

Interrupts:

- Standard 80C515 4-priority level structure
- 9 different sources of interrupt to the core

Power Down Modes:

- 2 standard 80C515 Power Down and IDLE modes
- Sub-μA OFF mode
- ON/OFF Main System Power Switch:
- Input for an SPST momentary switch to ground

Timers:

- (2) Standard 80C52 timers T0 and T1
- (1) 16-bit timer

Built-in ISO-7816 Card Interface:

- Linear regulator produces VCC for the card (1.8V, 3V or 5V)
- Full compliance with EMV 4.1
- Activation/Deactivation sequencers
- Auxiliary I/O lines (C4 and C8 signals)
- 7kV ESD protection on all interface pins

Communication with Smart Cards:

- ISO 7816 UART 9600 to 115kbps for T=0, T=1
- (2) 2-Byte FIFOs for transmit and receive
- Configured to drive multiple external Teridian 73S8010x interfaces (for multi-SAM architectures)

Voltage Detection:

- Analog Input (detection range: 1.0V to 2.5V)

Communication Interfaces:

- Full-duplex serial interface (1200 to 115kbps UART)
- I^2C Master Interface (400kbps)
- Man-Machine Interface and I/Os:
- 6x5 Keyboard (hardware scanning, debouncing and scrambling)
- (8) User I/Os
- Single programmable current output (LED)
- Operating Voltage:
- Single supply 2.7V to 6.5V operation (VPC)
- 5V supply (VBUS 4.4V to 5.5V) with or without battery back up operation (VBAT 4.0V to 6.5V)
- Automated detection of voltage presence - Priority on VBUS over VBAT

DC-DC Converter:

- Requires a single 10μH Inductor
- 3.3V / 20mA supply available for external circuits

Operating Temperature:

- -40°C to 85°C

Package:

- 68-pin QFN, 44 pin QFN

Turnkey Firmware:

- Compliant with PC/SC, ISO7816 and EMV4.1 specifications
- Features a Power Down mode accessible from the host
- Supports Plug & Play over serial interface
- Windows® XP driver available (*)
- Windows CE / Mobile driver available (*)
- Linux and other OS: Upon request
- Or for custom developments:
  - A complete set of ISO-7816, EMV4.1 and low-level libraries are available for T=0 / T=1
  - Two-level Application Programming Interface (ANSI C-language libraries)

(*) Contact Teridian Semiconductor for conditions and availability.

1 Hardware Description

1.1 Pin Description

Table 1: 73S1210 Pinout Description

Pin Name	Pin (68 QFN)	Pin (44 QFN)	Type	Equivalent Circuit*	Description
X12IN	10	9	I	Figure 26	MPU clock crystal oscillator input pin. A 1MΩ resistor is required between pins X12IN and X12OUT.
X12OUT	11	10	O	Figure 26	MPU clock crystal oscillator output pin.
ROW(5:0) 0 1 2 3 4 5	 21 22 24 33 36 37		I	Figure 34	Keypad row input sense.
COL(4:0) 0 1 2 3 4	 12 13 14 16 19		O	Figure 35	Keypad column output scan pins.
USR(7:0) 0 1 2 3 4 5 6 7	 35 34 32 31 30 29 23 20	 22 21 20 19 18 17 14 13	IO	Figure 30	General-purpose user pins, individually configurable as inputs or outputs or as external input interrupt ports.
SCL	5	6	O	Figure 29	I^2C (master mode) compatible Clock signal. Note: the pin is configured as an open drain output. When the I2C interface is being used, an external pull up resistor is required. A value of 3K is recommended.
SDA	6	7	IO	Figure 28	I^2C (master mode) compatible data I/O. Note: this pin is bi-directional. When the pin is configured as output, it is an open drain output. When the I2C interface is being used, an external pull up resistor is required. A value of 3K is recommended.
RXD	17	11	I	Figure 32	Serial UART Receive data pin.
TXD	18	12	O	Figure 29	Serial UART Transmit data pin.
INT3	48	30	I	Figure 32	General purpose interrupt input.
INT2	49	31	I	Figure 32	General purpose interrupt input.
SIO	47	29	IO	Figure 28	IO data signal for use with external Smart Card interface circuit such as 73S8010.
SCLK	45	28	O	Figure 29	Clock signal for use with external Smart Card interface circuit.

Pin Name	Pin (68 QFN)	Pin (44 QFN)	Type	Equivalent Circuit*	Description
PRES	53	34	I	Figure 41	Smart Card presence. Active high. Note: the pin has a very weak pull down resistor. In noisy environments, an external pull down may be desired to insure against a false card event.
CLK	55	36	O	Figure 39	Smart Card clock signal.
RST	57	38	O	Figure 39	Smart Card reset signal.
IO	61	42	IO	Figure 40	Smart Card Data IO signal.
AUX1	60	41	IO	Figure 40	Auxiliary Smart Card IO signal (C4).
AUX2	59	40	IO	Figure 40	Auxiliary Smart Card IO signal (C8).
VCC	58	39	PSO		Smart Card VCC supply voltage output. A 0.47µF capacitor is required and should be located at the smart card connector. The capacitor should be a ceramic type with low ESR.
GND	56	37	GND		Smart Card Ground.
VPC	65	44	PSI		Power supply source for main voltage converter circuit. A 10µF and a 0.1µF capacitor are required at the VPC input. The 10µF capacitor should be a ceramic type with low ESR.
VBUS	62		PSI		Alternate power source input from external power supply.
VBAT	64		PSI		Alternate power source input, typically from two series cells, V > 4V.
VP	54	35	PSO		Intermediate output of main converter circuit. Requires an external 4.7µF low ESR filter capacitor to GND.
LIN	66	1	PSI		Connection to 10µH inductor for internal step up converter. Note: inductor must be rated for 400 mA maximum peak current.
ON_OFF	63	43	I	Figure 43	Power control pin. Connected to normally open SPST switch to ground. Closing switch for duration greater than debounce period will turn 73S1210F on. If 73S1210F is on, closing switch will flag the 73S1210F to go to the off state. Firmware will control when the power is shut down.
OFF_REQ	52	33	O	Figure 33	Digital output. If ON_OFF switch is closed (to ground) for debounce duration and circuit is “on,” OFF_REQ will go high (Request to turn OFF). This output should be connected to an interrupt pin to signal the CPU core that a request to shut down power has been initiated. The firmware can then perform all of its shut down housekeeping duties before shutting down V_{DD}.
TBUS(3:0) 0 1 2 3	 50 46 44 41		IO		Trace bus signals for ICE.

specific SFR registers in the proper sequence. These special pattern/sequence requirements prevent inadvertent erasure of the flash memory.

The mass erase sequence is:

1. Write 1 to the FLSH_MEEN bit in the FLSHCTL register (SFR address 0xB2[1]).
2. Write pattern 0xAA to ERASE (SFR address 0x94).

Note: The mass erase cycle can only be initiated when the ICE port is enabled.

The page erase sequence is:

1. Write the page address to PGADDR (SFR address 0xB7[7:1]).
2. Write pattern 0x55 to ERASE (SFR address 0x94).

The PGADDR register denotes the page address for page erase. The page size is 512 (200h) bytes and there are 128 pages within the flash memory. The PGADDR denotes the upper seven bits of the flash memory address such that bit 7:1 of the PGADDR corresponds to bit 15:9 of the flash memory address. Bit 0 of the PGADDR is not used and is ignored. The MPU may write to the flash memory. This is one of the non-volatile storage options available to the user. The FLSHCTL SFR bit FLSH_PWE (flash program write enable) differentiates 80515 data store instructions (MOVX@DPTR,A) between Flash and XRAM writes. Before setting FLSH_PWE, all interrupts need to be disabled by setting EAL = 1. Table 3 shows the location and description of the 73S1210 flash-specific SFRs.

Any flash modifications must set the CPUCLK to operate at 3.6923 MHz (MPUCLKCtl = 0x0C) before any flash memory operations are executed to insure the proper timing when modifying the flash memory.

1.5 Special Function Registers (SFRs)

The 73S1210F utilizes numerous SFRs to communicate with the 73S1210Fs many peripherals. This results in the need for more SFR locations outside the direct address IRAM space (0x80 to 0xFF). While some peripherals are mapped to unused IRAM SFR locations, additional SFRs for the smart card and other peripheral functions are mapped to the top of the XRAM data space (0xFC00 to 0xFFFF).

1.5.1 Internal Data Special Function Registers (SFRs)

A map of the Special Function Registers is shown in Table 6.

Table 6: IRAM Special Function Registers Locations

Hex\Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/ Hex
F8									FF
F0	B								F7
E8									EF
E0	A								E7
D8	BRCON								DF
D0	PSW	**KCOL**	**KROW**	**KSCAN**	**KSTAT**	**KSIZE**	**KORDERL**	**KORDERH**	D7
C8	T2CON								CF
C0	IRCON								C7
B8	IEN1	IP1	S0RELH	S1RELH					BF
B0			**FLSHCTL**					**PGADDR**	B7
A8	IEN0	IP0	S0RELL						AF
A0									A7
98	S0CON	S0BUF	IEN2	S1CON	S1BUF	S1RELL			9F
90	**USR70**	**UDIR70**	DPS		**ERASE**				97
88	TCON	TMOD	TL0	TL1	TH0	TH1		**MCLKCtl**	8F
80		SP	DPL	DPH	DPL1	DPH1	WDTREL	PCON	87

Only a few addresses are used, the others are not implemented. SFRs specific to the 73S1210F are shown in **bold** print (gray background). Any read access to unimplemented addresses will return undefined data, while most write access will have no effect. However, a few locations are reserved and not user configurable in the 73S1210F. **Writes to the unused SFR locations can affect the operation of the core and therefore must not be written to. This applies to all the SFR areas in both the IRAM and XRAM spaces. In addition, all unused bit locations within valid SFR registers must be left in their default (power on default) states.**

1.5.2 IRAM Special Function Registers (Generic 80515 SFRs)

Table 7 shows the location of the SFRs and the value they assume at reset or power-up.

Table 7: IRAM Special Function Registers Reset Values

Name	Location	Reset Value	Description
SP	0x81	0x07	Stack Pointer
DPL	0x82	0x00	Data Pointer Low 0
DPH	0x83	0x00	Data Pointer High 0
DPL1	0x84	0x00	Data Pointer Low 1
DPH1	0x85	0x00	Data Pointer High 1
WDTREL	0x86	0x00	Watchdog Timer Reload register
PCON	0x87	0x00	Power Control
TCON	0x88	0x00	Timer/Counter Control
TMOD	0x89	0x00	Timer Mode Control
TL0	0x8A	0x00	Timer 0, low byte
TL1	0x8B	0x00	Timer 1, high byte
TH0	0x8C	0x00	Timer 0, low byte
TH1	0x8D	0x00	Timer 1, high byte
MCLKCtl	0x8F	0x0A	Master Clock Control
USR70	0x90	0xFF	User Port Data (7:0)
UDIR70	0x91	0xFF	User Port Direction (7:0)
DPS	0x92	0x00	Data Pointer Select Register
ERASE	0x94	0x00	Flash Erase
S0CON	0x98	0x00	Serial Port 0, Control Register
S0BUF	0x99	0x00	Serial Port 0, Data Buffer
IEN2	0x9A	0x00	Interrupt Enable Register 2
S1CON	0x9B	0x00	Serial Port 1, Control Register
S1BUF	0x9C	0x00	Serial Port 1, Data Buffer
S1RELL	0x9D	0x00	Serial Port 1, Reload Register, low byte
IEN0	0xA8	0x00	Interrupt Enable Register 0
IP0	0xA9	0x00	Interrupt Priority Register 0
S0RELL	0xAA	0xD9	Serial Port 0, Reload Register, low byte
FLSHCTL	0xB2	0x00	Flash Control
PGADDR	0xB7	0x00	Flash Page Address
IEN1	0xB8	0x00	Interrupt Enable Register 1
IP1	0xB9	0x00	Interrupt Priority Register 1
S0RELH	0xBA	0x03	Serial Port 0, Reload Register, high byte
S1RELH	0xBB	0x03	Serial Port 1, Reload Register, high byte
IRCON	0xC0	0x00	Interrupt Request Control Register
T2CON	0xC8	0x00	Timer 2 Control
PSW	0xD0	0x00	Program Status Word
KCOL	0XD1	0x1F	Keypad Column

Name	Location	Reset Value	Description
KROW	0XD2	0x3F	Keypad Row
KSCAN	0XD3	0x00	Keypad Scan Time
KSTAT	0XD4	0x00	Keypad Control/Status
KSIZE	0XD5	0x00	Keypad Size
KORDERL	0XD6	0x00	Keypad Column LS Scan Order
KORDERH	0XD7	0x00	Keypad Column MS Scan Order
BRCON	0xD8	0x00	Baud Rate Control Register (only BRCON.7 bit used)
A	0xE0	0x00	Accumulator
B	0xF0	0x00	B Register

1.5.3 External Data Special Function Registers (SFRs)

A map of the XRAM Special Function Registers is shown in Table 8. The smart card registers are listed separately in Table 107.

Table 8: XRAM Special Function Registers Reset Values

Name	Location	Reset Value	Description
DAR	0x FF80	0x00	Device Address Register (I^2C)
WDR	0x FF81	0x00	Write Data Register (I^2C)
SWDR	0x FF82	0x00	Secondary Write Data Register (I^2C)
RDR	0x FF83	0x00	Read Data Register (I^2C)
SRDR	0x FF84	0x00	Secondary Read Data Register (I^2C)
CSR	0x FF85	0x00	Control and Status Register (I^2C)
USRIntCtl1	0x FF90	0x00	External Interrupt Control 1
USRIntCtl2	0x FF91	0x00	External Interrupt Control 2
USRIntCtl3	0x FF92	0x00	External Interrupt Control 3
USRIntCtl4	0x FF93	0x00	External Interrupt Control 4
INT5Ctl	0x FF94	0x00	External Interrupt Control 5
INT6Ctl	0x FF95	0x00	External Interrupt Control 6
MPUCKCtl	0x FFA1	0x0C	MPU Clock Control
ACOMP	0x FFD0	0x00	Analog Compare Register
TRIMPCtl	0x FFD1	0x00	TRIM Pulse Control
FUSECtl	0x FFD2	0x00	FUSE Control
VDDFCtl	0x FFD4	0x00	VDDFault Control
SECReg	0x FFD7	0x00	Security Register
MISCtl0	0x FFF1	0x00	Miscellaneous Control Register 0
MISCtl1	0x FFF2	0x10	Miscellaneous Control Register 1
LEDCtl	0x FFF3	0xFF	LED Control Register

Accumulator (ACC, A): ACC is the accumulator register. Most instructions use the accumulator to hold the operand. The mnemonics for accumulator-specific instructions refer to accumulator as “A”, not ACC.

B Register: The B register is used during multiply and divide instructions. It can also be used as a scratch-pad register to hold temporary data.

Power Control Register 0 (PCON): 0x87 ← 0x00

The SMOD bit used for the baud rate generator is set up via this register.

Table 35: The PCON Register

MSB							LSB
SMOD	–	–	–	GF1	GF0	STOP	IDLE

Bit	Symbol	Function
PCON.7	SMOD	If SM0D = 1, the baud rate is doubled.
PCON.6	–	
PCON.5	–	
PCON.4	–	
PCON.3	GF1	General purpose flag 1.
PCON.2	GF0	General purpose flag 1.
PCON.1	STOP	Sets CPU to Stop mode.
PCON.0	IDLE	Sets CPU to Idle mode.

Baud Rate Control Register 0 (BRCON): 0xD8 ← 0x00

The BSEL bit used to enable the baud rate generator is set up via this register.

Table 36: The BRCON Register

MSB							LSB
BSEL	–	–	–	–	–	–	–

Bit	Symbol	Function
BRCON.7	BSEL	If BSEL = 0, the baud rate is derived using timer 1. If BSEL = 1 the baud rate generator circuit is used.
BRCON.6	–	
BRCON.5	–	.
BRCON.4	–	
BRCON.3	–	
BRCON.2	–	
BRCON.1	–	
BRCON.0	–	

External Interrupt Control Register (USRIntCtl1) : 0xFF90 ← 0x00

Table 50: The USRIntCtl1 Register

MSB							LSB
–	U1IS.6	U1IS.5	U1IS.4	–	U0IS.2	U0IS.1	U0IS.0

External Interrupt Control Register (USRIntCtl2) : 0xFF91 ← 0x00

Table 51: The USRIntCtl2 Register

MSB							LSB
–	U3IS.6	U3IS.5	U3IS.4	–	U2IS.2	U2IS.1	U2IS.0

External Interrupt Control Register (USRIntCtl3) : 0xFF92 ← 0x00

Table 52: The USRIntCtl3 Register

MSB							LSB
–	U5IS.6	U5IS.5	U5IS.4	–	U4IS.2	U4IS.1	U4IS.0

External Interrupt Control Register (USRIntCtl4) : 0xFF93 ← 0x00

Table 53: The USRIntCtl4 Register

MSB							LSB
–	U7IS.6	U7IS.5	U7IS.4	–	U6IS.2	U6IS.1	U6IS.0

1.7.11 LED Driver

The 73S1210F provides a single dedicated output pin for driving an LED. The LED driver pin can be configured as a current source that will pull to ground to drive an LED that is connected to VDD without the need for an external current limiting resistor. This pin may be used as general purpose output with the programmed pull-down current and a strong (CMOS) pull-up, if enabled. The analog block must be enabled when this output is being used to drive the selected output current.

This pin may be used as an input with consideration of the programmed output current and level. The register bit when read, indicates the state of the pin.

LED Control Register (LEDCtl): 0xFFF3 ← 0xFF

Table 56: The LEDCtl Register

MSB LSB

–	LPUEN	ISET.1	ISET.0	–	–	–	LEDD0

Bit	Symbol	Function
LEDCtl.7	–	
LEDCtl.6	LPUEN	0 = Pull-ups are enabled for all of the LED pins.
LEDCtl.5	ISET.1	These two bits control the drive current (to ground) for the LED driver pin. Current levels are: 00 = 0ma(off) 01 = 2ma 10 = 4ma 11 = 10ma
LEDCtl.4	ISET.0	
LEDCtl.3	–	
LEDCtl.2	–	
LEDCtl.1	–	
LEDCtl.0	LEDD0	Write data controls output level of pin LED0. Read will report level of pin LED0.

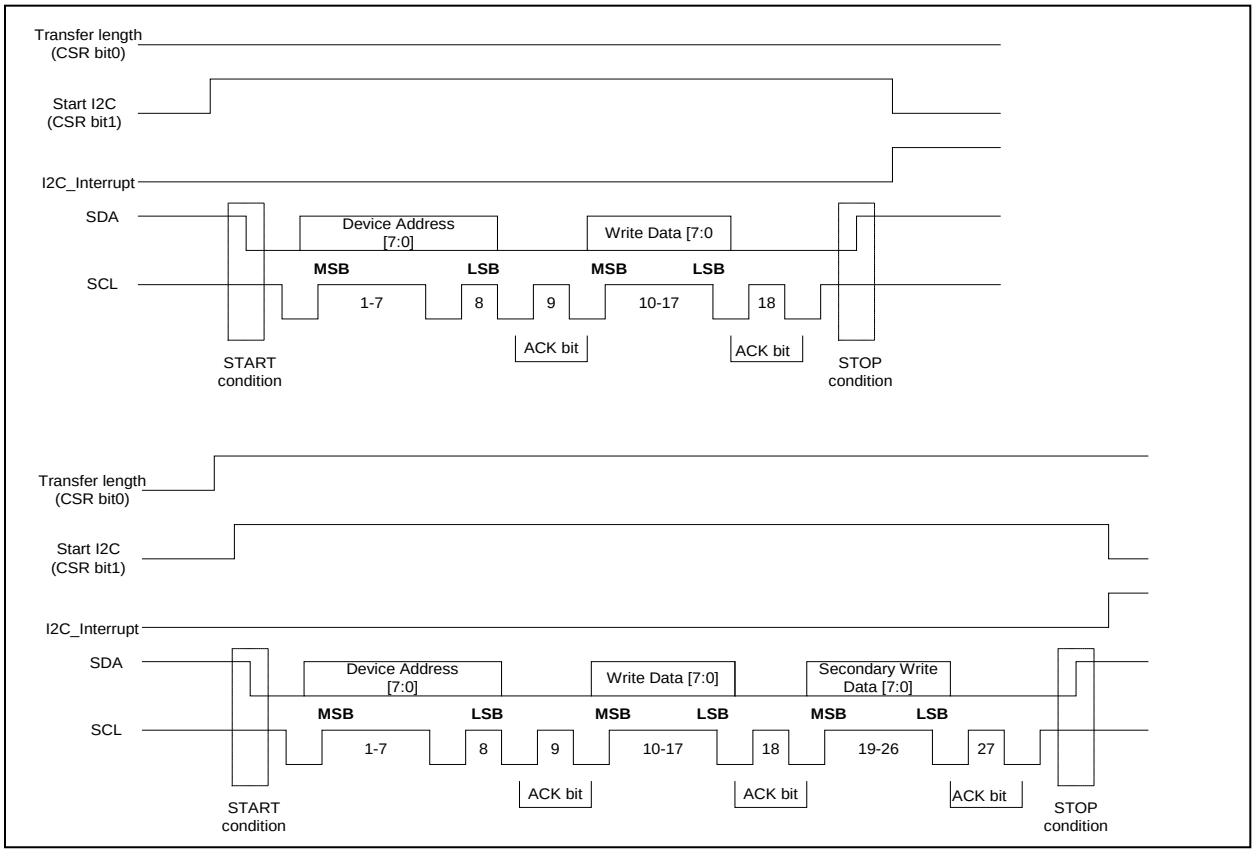
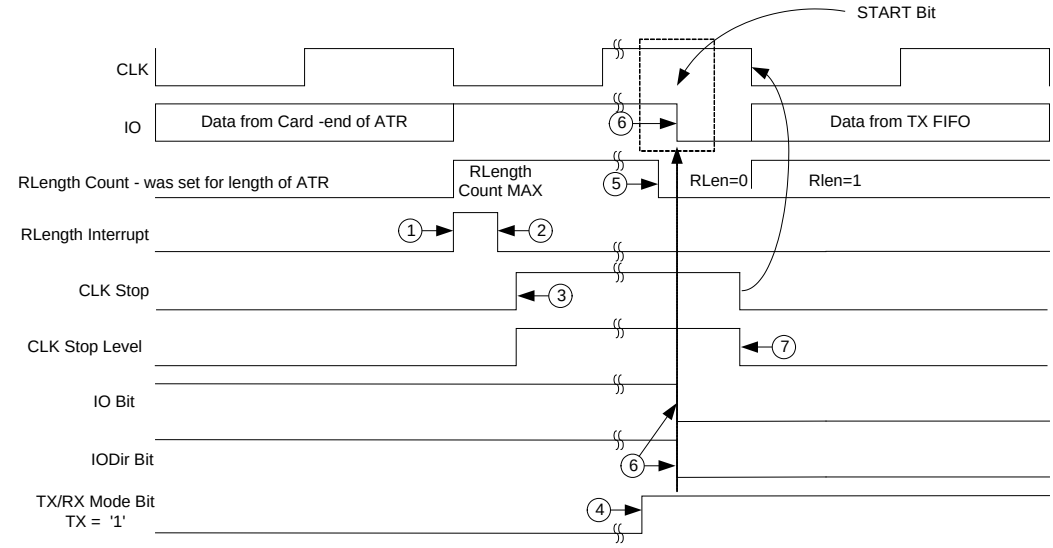


Figure 10: I²C Write Mode Operation

1.7.12.2 I²C Read Sequence

To read data on the I²C Master Bus from a slave device, the 80515 has to program the following registers in this sequence:

1. Write slave device address to Device Address register (DAR). The data contains 7 bits device address and 1 bit of op-code. The op-code bit should be written with a 1.
2. Write control data to Control and Status register. Write a 1 to bit 1 to start I²C Master Bus. Also write a 1 to bit 0 if the Secondary Read Data register (SRDR) is to be captured from the I²C Slave device.
3. Wait for I²C interrupt to be asserted. It indicates that the read operation on the I²C bus is done. Refer to information about the INT6Ctl, IEN1 and IRCON registers for masking and flag operation.
4. Read data from the Read Data register (RDR).
5. Read data from Secondary Read Data register (SRDR) if bit 0 of Control and Status register (CSR) is written with a 1.

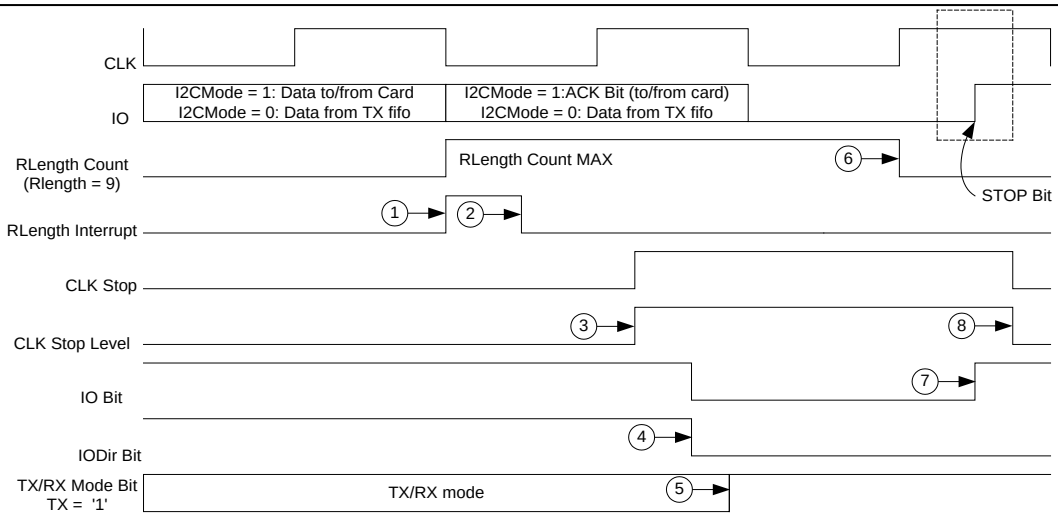


1. Interrupt generated when Rlength counter is MAX.
2. Read and clear Interrupt.
3. Set CLK Stop and CLK Stop level high in Interrupt routine.
4. Set TX/RX Bit to TX mode.
5. Reload Rlength Counter.
6. Set IO Bit low and IODir = Output. Since Rlen=(MAX or 0) and TX/RX =1, IO pin is controlled by IO bit.
7. Clear CLK Stop and CLK Stop level.

Note: Data in TX fifo should not be Empty here.

Synchronous Clock Start/Stop Mode style Start bit procedure. This procedure should be used to generate the start bit insertion in Synchronous mode for Synchronous Clock Start/Stop Mode protocol.

Figure 22: Creation of Synchronous Clock Start/Stop Mode Start Bit in Sync Mode



1. Interrupt generated when Rlength counter is MAX.
2. Read and clear Interrupt.
3. Set CLK Stop and CLK Stop level high.
4. Set IO Bit low and IODir = Output.
5. Set TX/RX Bit to TX mode.
6. Reload Rlength Counter.
7. Set IO Bit High and IODir = Output.
8. Clear CLK Stop and CLK Stop level.

Note: Data in TX fifo should not be Empty here.

Synchronous Clock Start/Stop Mode Stop bit procedure. This procedure should be used to generate the Stop bit in Synchronous Mode. SYCKST is bit 7 of STXCTL register.

Figure 23: Creation of Synchronous Clock Start/Stop Mode Stop Bit in Sync Mode

Smart Card Control Register (SCCtl): 0xFE0A ← 0x21

This register is used to monitor reception of data from the smart card.

Table 82: The SCCtl Register

MSB LSB

RSTCRD	–	IO	IOD	C8	C4	CLKLVL	CLKOFF

Bit	Symbol	Function
SCCtl.7	RSTCRD	1 = Asserts the RST (set RST = 0) to the smart card interface, 0 = De-assert the RST (set RST = 1) to the smart card interface. Can be used to extend RST to the smart card. Refer to RLength register description. This bit is operational in all modes and can be used to extend RST during activation or perform a "Warm Reset" as required. In auto-sequence mode, this bit should be set = 0 to allow the sequencer to de-assert RST per the RLength parameters. In sync mode (see the SPrtcol register) the sense of this bit is non-inverted, if set = 1, RST = 1, if set = 0, RST = 0. Rlen has no effect on Reset in sync mode.
SCCtl.6	–	
SCCtl.5	IO	Smart Card I/O. Read is state of I/O signal (Caution, this signal is not synchronized to the MPU clock). In Bypass mode, write value is state of signal on I/O. In sync mode, this bit will contain the value of I/O pin on the latest rising edge of CLK.
SCCtl.4	IOD	Smart Card I/O Direction control Bypass mode or sync mode. 1 = input (default), 0 = output.
SCCtl.3	C8	Smart Card C8. When C8 is an output, the value written to this bit will appear on the C8 line. The value read when C8 is an output is the value stored in the register. When C8 is an input, the value read is the value on the C8 pin (Caution, this signal is not synchronized to the MPU clock). When C8 is an input, the value written will be stored in the register but not presented to the C8 pin.
SCCtl.2	C4	Smart Card C4. When C4 is an output, the value written to this bit will appear on the C4 line. The value read when C4 is an output is the value stored in the register. When C4 is an input, the value read is the value on the C4 pin (Caution, this signal is not synchronized to the MPU clock). When C4 is an input, the value written will be stored in the register but not presented to the C4 pin.
SCCtl.1	CLKLVL	1 = High, 0 = Low. If CLKOFF is set = 1, the CLK to smart card will be at the logic level indicated by this bit. If in bypass mode, this bit directly controls the state of CLK.
SCCtl.0	CLKOFF	0 = CLK is enabled. 1 = CLK is not enabled. When asserted, the CLK will stop at the level selected by CLKLVL. This bit has no effect if in bypass mode.

Byte Control Register (SByteCtl): 0xFE12 ← 0x2C

This register controls the processing of characters and the detection of the TS byte. When receiving, a Break is asserted at 10.5 ETU after the beginning of the start bit. Break from the card is sampled at 11 ETU.

Table 89: The SByteCtl Register

MSB LSB

–	DETTS	DIRTS	BRKDUR.1	BRKDUR.0	–	–	–

Bit	Symbol	Function
SByteCtl.7	–	
SByteCtl.6	DETTS	Detect TS Byte – 1 = Next Byte is TS, 0 = Next byte is not TS. When set, the hardware will treat the next character received as the TS and determine if direct or indirect convention is being used. Direct convention is the default used if firmware does not set this bit prior to transmission of TS by the smart card to the firmware. The hardware will check parity and generate a break as defined by the DISPAR and BRKGEN bits in the parity control register. This bit is cleared by hardware after TS is received. TS is decoded prior to the FIFO and is stored in the receive FIFO.
SByteCtl.5	DIRTS	Direct Mode TS Select – 1 = direct mode, 0 = indirect mode. Set/cleared by hardware when TS is processed indicating either direct/indirect mode of operation. When switching between smart cards, the firmware should write the bit appropriately since this register is not unique to an individual smart card (firmware should keep track of this bit).
SByteCtl.4	BRKDUR.1	Break Duration Select – 00 = 1 ETU, 01 = 1.5 ETU, 10 = 2 ETU, 11 = reserved. Determines the length of a Break signal which is generated when detecting a parity error on a character reception in T=0 mode.
SByteCtl.3	BRKDUR.0	
SByteCtl.2	–	
SByteCtl.1	–	
SByteCtl.0	–	

Table 93: Divider Values for the ETU Clock

	Fi code	0000	0001	0010	0011	0100	0101
Di code	F→ D↓	372	372	558	744	1116	1488
0001	1	744	744	1116	1488	2232	2976
0010	2	372	372	558	744	1116	1488
0011	4	186	186	279	372	558	744
0100	8	93	93	138	186	279	372
1000	12	62	62	93	124	186	248
0101	16	47	47	70	93	140	186
1001	20	37	37	56	74	112	149
0110	32	23	23	35	47	70	93

	Fi code	0110	1001	1010	1011	1100	1101
Di code	F→ D↓	1860	512	768	1024	1536	2048
0001	1	3720	1024	1536	2048	3072	4096
0010	2	1860	512	768	1024	1536	2048
0011	4	930	256	384	512	768	1024
0100	8	465	128	192	256	384	512
1000	12	310	85	128	171	256	341
0101	16	233	64	96	128	192	256
1001	20	186	51	77	102	154	205
0110	32	116	32	48	64	96	128

1.7.16 VDD Fault Detect Function

The 73S1210F contains a circuit to detect a low-voltage condition on the supply voltage V_{DD}. If enabled, it will deactivate the active internal smart card interface when V_{DD} falls below the V_{DD} Fault threshold. The register configures the V_{DD} Fault threshold for the nominal default of 2.3V* or a user selectable threshold. The user's code may load a different value using the FOVRVDDF bit = 1 after the power-up cycle has completed.

VDDFault Control Register (VDDFCtl): 0xFFD4 ← 0x00

Table 108: The VDDFCtl Register

MSB LSB

–	FOVRVDDF	VDDFLTEN	–	STXDAT.3	VDDFTH.2	VDDFTH.1	VDDFTH.0

Bit	Symbol	Function
VDDFCtl.7	–	
VDDFCtl.6	FOVRVDDF	Setting this bit high will allow the VDDFLT(2:0) bits set in this register to control the VDDFault threshold. When this bit is set low, the VDDFault threshold will be set to the factory default setting of 2.3V*.
VDDFCtl.5	VDDFLTEN	Set = 1 will disable VDD Fault operation.
VDDFCtl.4	–	
VDDFCtl.3	–	
VDDFCtl.2	VDDFTH.2	VDD Fault Threshold. Bit Value(2:0) VDDFault Voltage 000 2.3 (nominal default) 001 2.4 010 2.5 011 2.6 100 2.7 101 2.8 110 2.9 111 3.0
VDDFCtl.1	VDDFTH.1	
VDDFCtl.0	VDDFTH.0	

* Note: The V_{DD} Fault factory default can be set to any threshold as defined by bits VDDFTH(2:0). The 73S1210F has the capability to burn fuses at the factory to set the factory default to any of these voltages. Contact Teridian for further details.

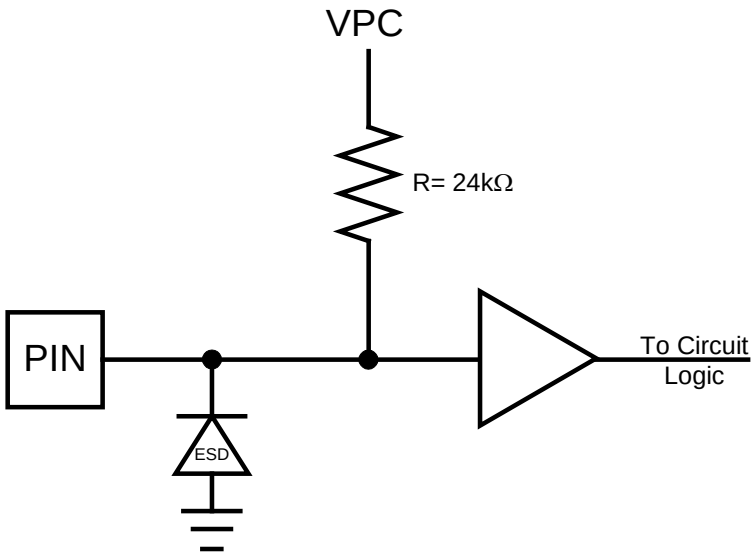


Figure 43: ON_OFF Input Circuit

5.2 44-pin QFN Pinout

CAUTION: Use handling procedures necessary for a static sensitive component.

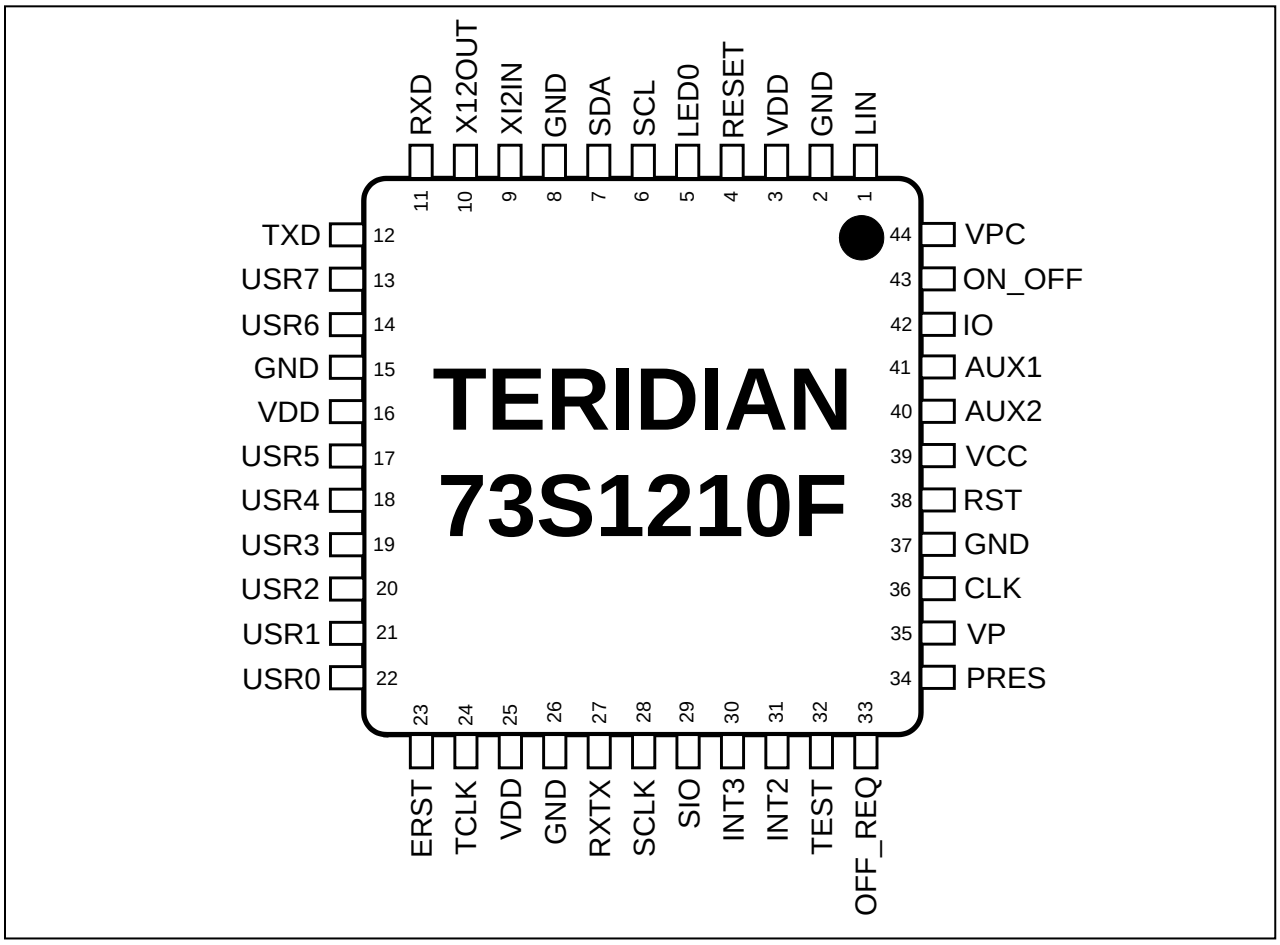


Figure 45: 73S1210F 44 QFN Pinout

6.2 44-Pin QFN Package Outline

Notes: 5.1mm x 5.1mm exposed pad area must remain UNCONNECTED (clear of PCB traces or vias). Controlling dimensions are in mm.

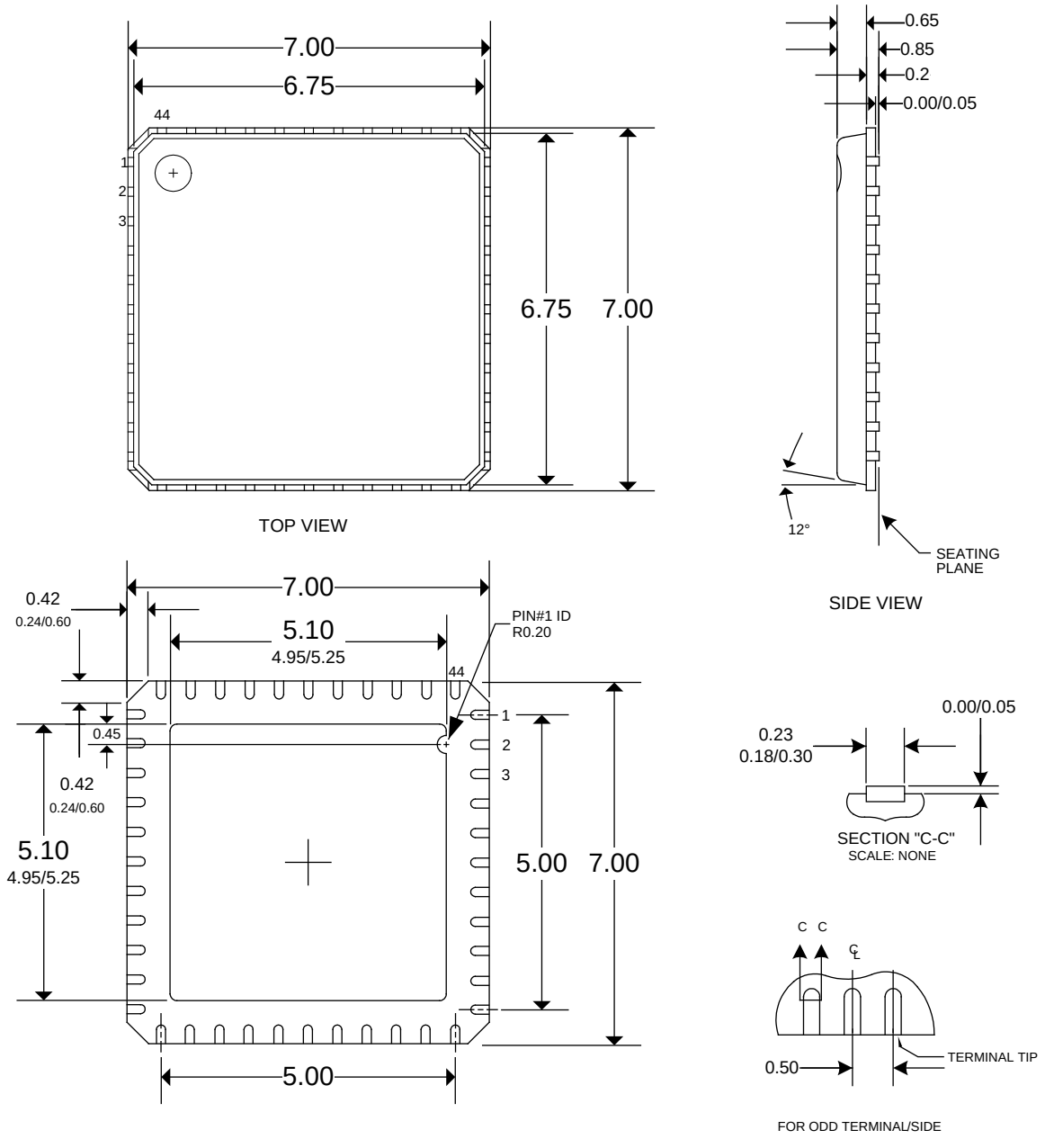


Figure 47: 73S1210F 44 QFN Package Drawing