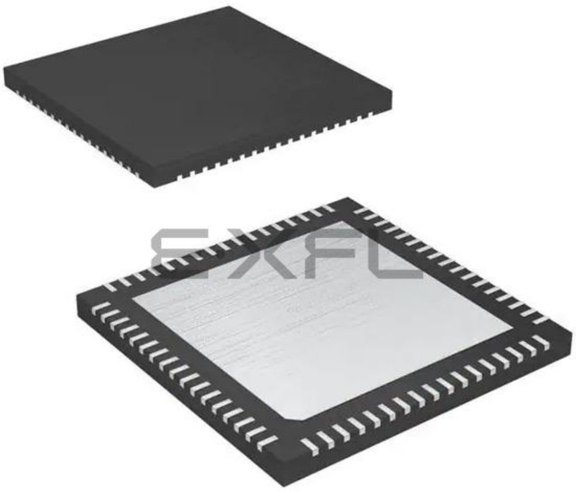

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80515
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SmartCard, UART/USART
Peripherals	LED, POR, WDT
Number of I/O	8
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/73s1210f-68mr-f-ph

Figures

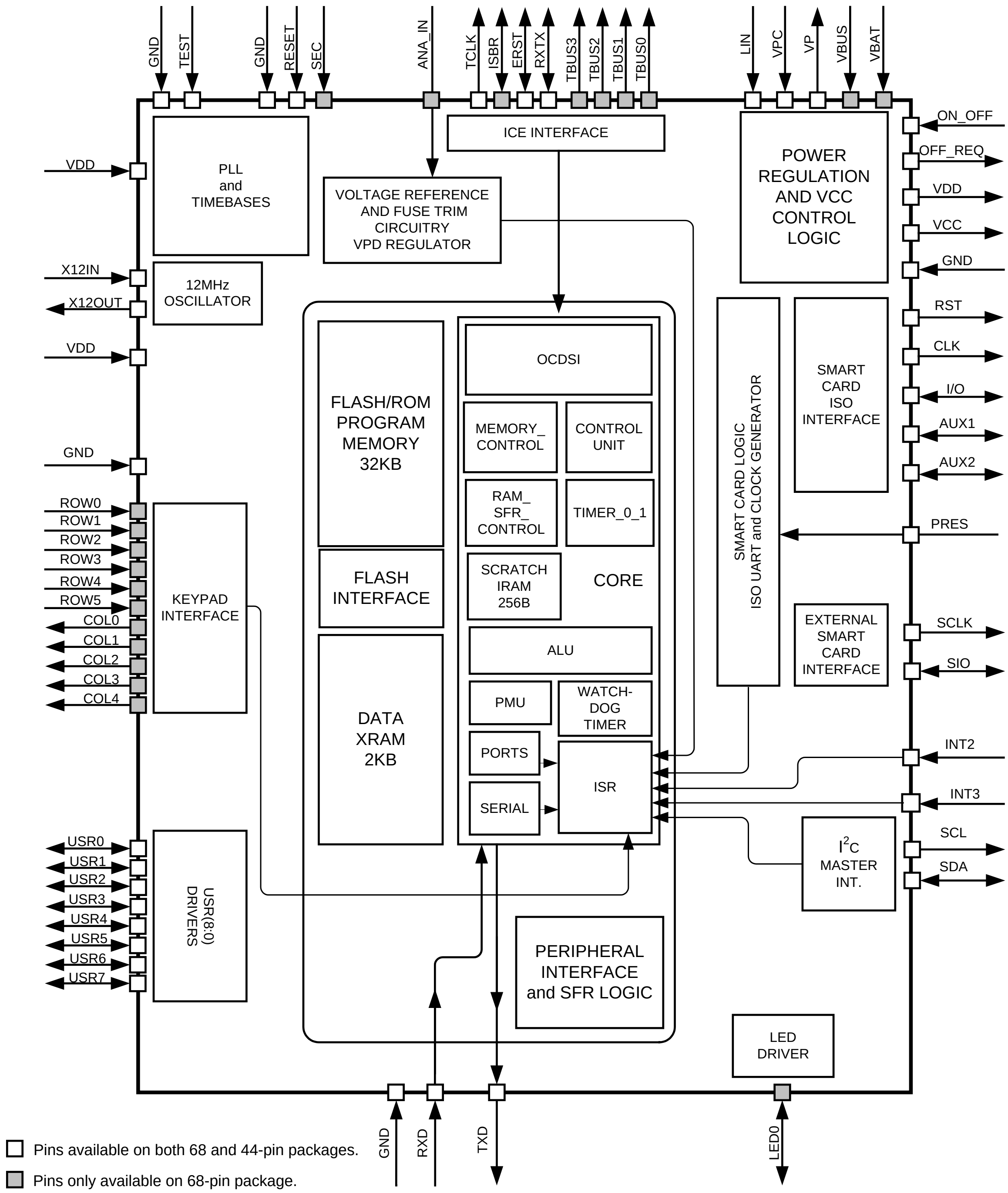

Figure 1: IC Functional Block Diagram

Pin Name	Pin (68 QFN)	Pin (44 QFN)	Type	Equivalent Circuit*	Description
PRES	53	34	I	Figure 41	Smart Card presence. Active high. Note: the pin has a very weak pull down resistor. In noisy environments, an external pull down may be desired to insure against a false card event.
CLK	55	36	O	Figure 39	Smart Card clock signal.
RST	57	38	O	Figure 39	Smart Card reset signal.
IO	61	42	IO	Figure 40	Smart Card Data IO signal.
AUX1	60	41	IO	Figure 40	Auxiliary Smart Card IO signal (C4).
AUX2	59	40	IO	Figure 40	Auxiliary Smart Card IO signal (C8).
VCC	58	39	PSO		Smart Card VCC supply voltage output. A 0.47μF capacitor is required and should be located at the smart card connector. The capacitor should be a ceramic type with low ESR.
GND	56	37	GND		Smart Card Ground.
VPC	65	44	PSI		Power supply source for main voltage converter circuit. A 10μF and a 0.1μF capacitor are required at the VPC input. The 10μF capacitor should be a ceramic type with low ESR.
VBUS	62		PSI		Alternate power source input from external power supply.
VBAT	64		PSI		Alternate power source input, typically from two series cells, V > 4V.
VP	54	35	PSO		Intermediate output of main converter circuit. Requires an external 4.7μF low ESR filter capacitor to GND.
LIN	66	1	PSI		Connection to 10μH inductor for internal step up converter. Note: inductor must be rated for 400 mA maximum peak current.
ON_OFF	63	43	I	Figure 43	Power control pin. Connected to normally open SPST switch to ground. Closing switch for duration greater than debounce period will turn 73S1210F on. If 73S1210F is on, closing switch will flag the 73S1210F to go to the off state. Firmware will control when the power is shut down.
OFF_REQ	52	33	O	Figure 33	Digital output. If ON_OFF switch is closed (to ground) for debounce duration and circuit is "on," OFF_REQ will go high (Request to turn OFF). This output should be connected to an interrupt pin to signal the CPU core that a request to shut down power has been initiated. The firmware can then perform all of its shut down housekeeping duties before shutting down V_{DD}.
TBUS(3:0) 0 1 2 3	 50 46 44 41		IO		Trace bus signals for ICE.

1.2 Hardware Overview

The 73S1210F single smart card controller integrates all primary functional blocks required to implement a smart card reader. Included on chip are an 8051-compatible microprocessor (MPU) which executes up to one instruction per clock cycle (80515), a fully integrated IS0 7816 compliant smart card interface, expansion smart card interface, serial interface, I2C interface, 6 x 5 keypad interface, RAM, FLASH memory, and a variety of I/O pins.

The power management circuitry provides a 3.3V voltage output (VDD, pin #68) that must be connected to the power supply inputs of the digital core of the circuit, pins # 28 and 40 (these are not internally connected). Should external circuitry require a 3.3V digital power supply, the VDD output is capable of supplying additional current.

Figure 1 shows a functional block diagram of the 73S1210F.

1.3 80515 MPU Core

1.3.1 80515 Overview

The 73S1210F includes an 80515 MPU (8-bit, 8051-compatible) that performs most instructions in one clock cycle. The 80515 architecture eliminates redundant bus states and implements parallel execution of fetch and execution phases. Normally a machine cycle is aligned with a memory fetch, therefore, most of the 1-byte instructions are performed in a single cycle. This leads to an 8x performance (average) improvement (in terms of MIPS) over the Intel 8051 device running at the same clock frequency.

Actual processor clocking speed can be adjusted to the total processing demand of the application (cryptographic calculations, key management, memory management, and I/O management) using the XRAM special function register MPUCKCtl.

Typical smart card, serial, keyboard and I2C management functions are available for the MPU as part of the Teridian standard library. A standard ANSI “C” 80515-application programming interface library is available to help reduce design cycle. Refer to the *73S12xxF Software User’s Guide*.

1.3.2 Memory Organization

The 80515 MPU core incorporates the Harvard architecture with separate code and data spaces. Memory organization in the 80515 is similar to that of the industry standard 8051. There are three memory areas: Program memory (Flash), external data memory (XRAM), and internal data memory (IRAM). Data bus address space is allocated to on-chip memory as shown Table 2

Table 2: MPU Data Memory Map

Address (hex)	Memory Technology	Memory Type	Typical Usage	Memory Size (bytes)
0000-7FFF	Flash Memory	Non-volatile	Program and non-volatile data	32KB
0000-07FF	Static RAM	Volatile	MPU data XRAM	2KB
FC00-FFFF	External SFR	Volatile	Peripheral control	1KB

Note: The IRAM is part of the core and is addressed differently.

Program Memory: The 80515 can address up to 32KB of program memory space from 0x0000 to 0xFFFF. Program memory is read when the MPU fetches instructions or performs a MOVC operation. After reset, the MPU starts program execution from location 0x0000. The lower part of the program memory includes reset and interrupt vectors. The interrupt vectors are spaced at 8-byte intervals, starting from 0x0003. Reset is located at 0x0000.

Flash Memory: The program memory consists of flash memory. The flash memory is intended to primarily contain MPU program code. Flash erasure is initiated by writing a specific data pattern to specific SFR registers in the proper sequence. These special pattern/sequence requirements prevent inadvertent erasure of the flash memory.

The mass erase sequence is:

1. Write 1 to the FLSH_MEEN bit in the FLSHCTL register (SFR address 0xB2[1]).
2. Write pattern 0xAA to ERASE (SFR address 0x94).

Note: The mass erase cycle can only be initiated when the ICE port is enabled.

The page erase sequence is:

1. Write the page address to PGADDR (SFR address 0xB7[7:1]).
2. Write pattern 0x55 to ERASE (SFR address 0x94).

The PGADDR register denotes the page address for page erase. The page size is 512 (200h) bytes and there are 128 pages within the flash memory. The PGADDR denotes the upper seven bits of the flash memory address such that bit 7:1 of the PGADDR corresponds to bit 15:9 of the flash memory address. Bit 0 of the PGADDR is not used and is ignored. The MPU may write to the flash memory. This is one of the non-volatile storage options available to the user. The FLSHCTL SFR bit FLSH_PWE (flash program write enable) differentiates 80515 data store instructions (MOVX@DPTR,A) between Flash and XRAM writes. Before setting FLSH_PWE, all interrupts need to be disabled by setting EAL = 1. Table 3 shows the location and description of the 73S1210 flash-specific SFRs.

Any flash modifications must set the CPUCLK to operate at 3.6923 MHz (MPUCLKCtl = 0x0C) before any flash memory operations are executed to insure the proper timing when modifying the flash memory.

1.4 Program Security

Two levels of program and data security are available. Each level requires a specific fuse to be blown in order to enable or set the specific security mode. Mode 0 security is enabled by setting the SECURE bit (bit 6 of SFR register FLSHCTL 0xB2). Mode 0 limits the ICE interface to only allow bulk erase of the flash program memory. All other ICE operations are blocked. This guarantees the security of the user's MPU program code. Security (Mode 0) is enabled by MPU code that sets the SECURE bit. The MPU code must execute the setting of the SECURE bit immediately after a reset to properly enable Mode 0. This should be the first instruction after the reset vector jump has been executed. If the "startup.a51" assembly file is used in an application, then it must be modified to set the SECURE bit after the reset vector jump. If not using "startup.a51", then this should be the first instruction in main(). Once security Mode 0 is enabled, the only way to disable it is to perform a global erase of the flash followed by a full circuit reset. Once the flash has been erased and the reset has been executed, security Mode 0 is disabled and the ICE has full control of the core. The flash can be reprogrammed after the bulk erase operation is completed. Global erase of the flash will also clear the data XRAM memory.

The security enable bit (SECURE) is reset whenever the MPU is reset. Hardware associated with the bit only allows it to be set. As a result, the code may set the SECURE bit to enable the security Mode 0 feature but may not reset it. Once the SECURE bit is set, the code is protected and no external read of program code in flash or data (in XRAM) is possible. In order to invoke the security Mode 0, the SECSET0 (bit 1 of the XRAM SFR register SECReg 0xFFD7) fuse must be blown beforehand or the security mode 0 will not be enabled. The SECSET0 and SECSET1 fuses once blown, cannot be overridden.

Specifically, when SECURE is set:

- The ICE is limited to bulk flash erase only.
- Page zero of flash memory, the preferred location for the user's preboot code, may not be page-erased by either MPU or ICE. Page zero may only be erased with global flash erase. Note that global flash erase erases XRAM whether the SECURE bit is set or not.
- Writes to page zero, whether by MPU or ICE, are inhibited.

Security mode 1 is in effect when the SECSET1 fuse has been programmed (blown open). In security mode 1, the ICE is completely and permanently disabled. The Flash program memory and the MPU are not available for alteration, observation, nor control. As soon as the fuse has been blown, the ICE is disabled. The testing of the SECSET1 fuse will occur during the reset and before the start of pre-boot and boot cycles. This mode is not reversible, nor recoverable. In order to blow the SECSET1 fuse, the SEC pin must be held high for the fuse burning sequence to be executed properly. The firmware can check to see if this pin is held high by reading the SECPIN bit (bit 5 of XRAM SFR register SECReg 0xFFD7). If this bit is set and the firmware desires, it can blow the SECSET1 fuse. The burning of the SECSET0 does not require the SEC pin to be held high.

In order to blow the fuse for SECSET1 and SECSET0, a particular set of register writes in a specific order need to be followed. There are two additional registers that need to have a specific value written to them in order for the desired fuse to be blown. These registers are FUSECtl (0xFFD2) and TRIMPCtl (0xFFD1). The sequence for blowing the fuse is as follows:

1. Write 0x54H to FUSECtl.
2. Write 0x81H for security mode 0. Note: only program one security mode at a time.
   Write 0x82H for security mode 1. Note: SEC pin must be high for security mode 1.
3. Write 0xA6 to TRIMPCtl.
4. Delay about 500 µs.
5. Write 0x00 to TRIMPCtl and FUSECtl.

1.5 Special Function Registers (SFRs)

The 73S1210F utilizes numerous SFRs to communicate with the 73S1210Fs many peripherals. This results in the need for more SFR locations outside the direct address IRAM space (0x80 to 0xFF). While some peripherals are mapped to unused IRAM SFR locations, additional SFRs for the smart card and other peripheral functions are mapped to the top of the XRAM data space (0xFC00 to 0xFFFF).

1.5.1 Internal Data Special Function Registers (SFRs)

A map of the Special Function Registers is shown in Table 6.

Table 6: IRAM Special Function Registers Locations

Hex\Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/ Hex
F8									FF
F0	B								F7
E8									EF
E0	A								E7
D8	BRCON								DF
D0	PSW	**KCOL**	**KROW**	**KSCAN**	**KSTAT**	**KSIZE**	**KORDERL**	**KORDERH**	D7
C8	T2CON								CF
C0	IRCON								C7
B8	IEN1	IP1	S0RELH	S1RELH					BF
B0			**FLSHCTL**					**PGADDR**	B7
A8	IEN0	IP0	S0RELL						AF
A0									A7
98	S0CON	S0BUF	IEN2	S1CON	S1BUF	S1RELL			9F
90	**USR70**	**UDIR70**	DPS		**ERASE**				97
88	TCON	TMOD	TL0	TL1	TH0	TH1		**MCLKCtl**	8F
80		SP	DPL	DPH	DPL1	DPH1	WDTREL	PCON	87

Only a few addresses are used, the others are not implemented. SFRs specific to the 73S1210F are shown in **bold** print (gray background). Any read access to unimplemented addresses will return undefined data, while most write access will have no effect. However, a few locations are reserved and not user configurable in the 73S1210F. **Writes to the unused SFR locations can affect the operation of the core and therefore must not be written to. This applies to all the SFR areas in both the IRAM and XRAM spaces. In addition, all unused bit locations within valid SFR registers must be left in their default (power on default) states.**

1.5.2 IRAM Special Function Registers (Generic 80515 SFRs)

Table 7 shows the location of the SFRs and the value they assume at reset or power-up.

Table 7: IRAM Special Function Registers Reset Values

Name	Location	Reset Value	Description
SP	0x81	0x07	Stack Pointer
DPL	0x82	0x00	Data Pointer Low 0
DPH	0x83	0x00	Data Pointer High 0
DPL1	0x84	0x00	Data Pointer Low 1
DPH1	0x85	0x00	Data Pointer High 1
WDTREL	0x86	0x00	Watchdog Timer Reload register
PCON	0x87	0x00	Power Control
TCON	0x88	0x00	Timer/Counter Control
TMOD	0x89	0x00	Timer Mode Control
TL0	0x8A	0x00	Timer 0, low byte
TL1	0x8B	0x00	Timer 1, high byte
TH0	0x8C	0x00	Timer 0, low byte
TH1	0x8D	0x00	Timer 1, high byte
MCLKCtl	0x8F	0x0A	Master Clock Control
USR70	0x90	0xFF	User Port Data (7:0)
UDIR70	0x91	0xFF	User Port Direction (7:0)
DPS	0x92	0x00	Data Pointer Select Register
ERASE	0x94	0x00	Flash Erase
S0CON	0x98	0x00	Serial Port 0, Control Register
S0BUF	0x99	0x00	Serial Port 0, Data Buffer
IEN2	0x9A	0x00	Interrupt Enable Register 2
S1CON	0x9B	0x00	Serial Port 1, Control Register
S1BUF	0x9C	0x00	Serial Port 1, Data Buffer
S1RELL	0x9D	0x00	Serial Port 1, Reload Register, low byte
IEN0	0xA8	0x00	Interrupt Enable Register 0
IP0	0xA9	0x00	Interrupt Priority Register 0
S0RELL	0xAA	0xD9	Serial Port 0, Reload Register, low byte
FLSHCTL	0xB2	0x00	Flash Control
PGADDR	0xB7	0x00	Flash Page Address
IEN1	0xB8	0x00	Interrupt Enable Register 1
IP1	0xB9	0x00	Interrupt Priority Register 1
S0RELH	0xBA	0x03	Serial Port 0, Reload Register, high byte
S1RELH	0xBB	0x03	Serial Port 1, Reload Register, high byte
IRCON	0xC0	0x00	Interrupt Request Control Register
T2CON	0xC8	0x00	Timer 2 Control
PSW	0xD0	0x00	Program Status Word
KCOL	0XD1	0x1F	Keypad Column

All ports on the chip are bi-directional. Each consists of a Latch (SFR 'USR70'), an output driver, and an input buffer, therefore the MPU can output or read data through any of these ports if they are not used for alternate purposes.

1.6 Instruction Set

All instructions of the generic 8051 microcontroller are supported. A complete list of the instruction set and of the associated op-codes is contained in the *73S12xxF Software User's Guide*.

1.7 Peripheral Descriptions

1.7.1 Oscillator and Clock Generation

The 73S1210F has one oscillator circuit for the main CPU clock. The main oscillator circuit is designed to operate with various crystal or external clock frequencies. An internal divider working in conjunction with a PLL and VCO provides a 96MHz internal clock within the 73S1210F. 96 MHz is the recommended frequency for proper operation of specific peripheral blocks such as the specific timers, ISO 7816 UART and interfaces, Step-up converter, and keypad. The clock generation and control circuits are shown in Figure 3.

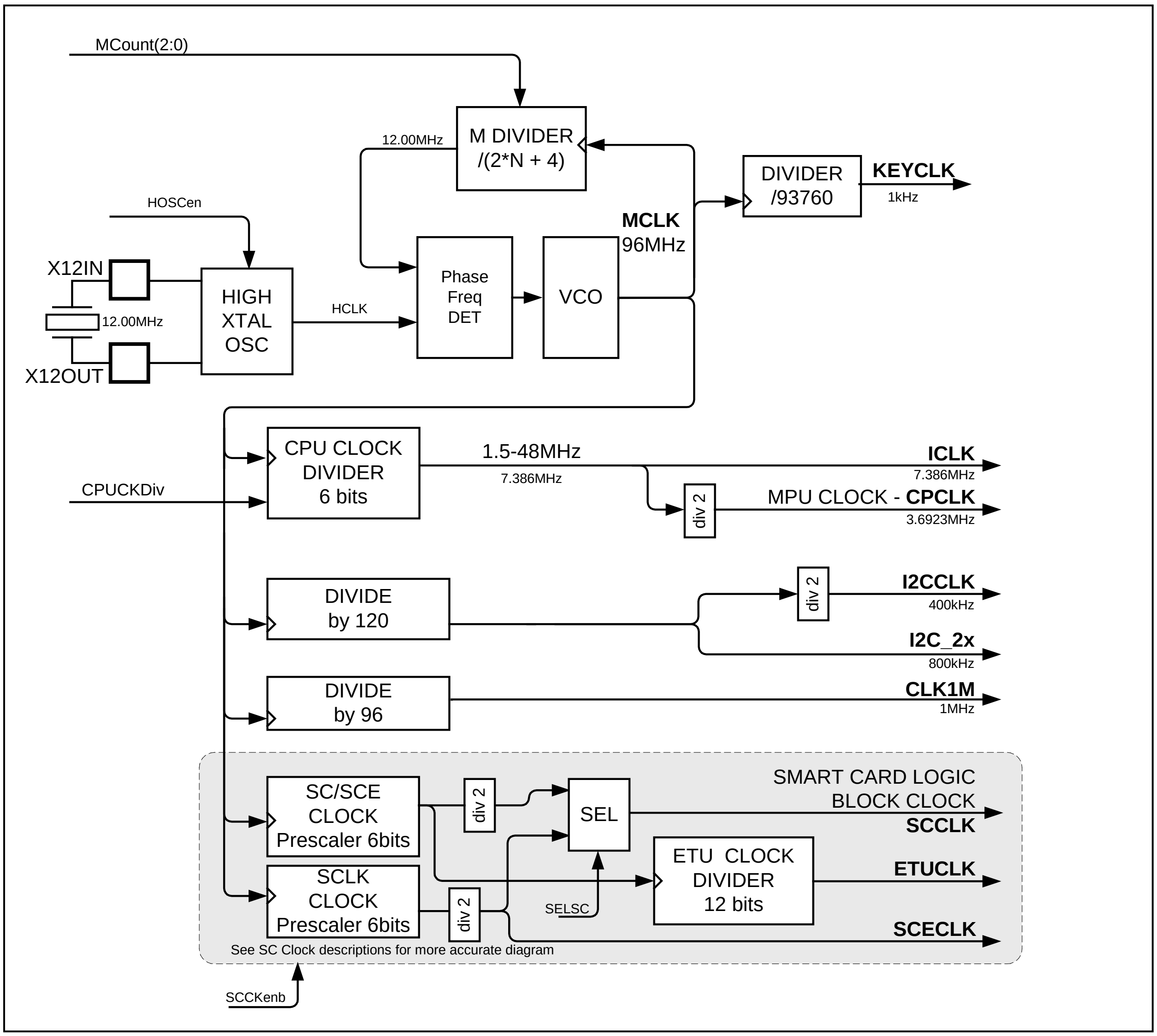

Figure 3: Clock Generation and Control Circuits

Interrupt Request Register (IRCON): 0xC0 ← 0x00

Table 24: The IRCON Register

MSB							LSB
–	–	EX6	IEX5	IEX4	IEX3	IEX2	–

Bit	Symbol	Function
IRCON.7	–	
IRCON.6	–	
IRCON.5	IEX6	External interrupt 6 flag.
IRCON.4	IEX5	External interrupt 5 flag.
IRCON.3	IEX4	External interrupt 4 flag.
IRCON.2	IEX3	External interrupt 3 flag.
IRCON.1	IEX2	External interrupt 2 flag.
IRCON.0	–	

1.7.5.3 External Interrupts

The external interrupts (external to the CPU core) are connected as shown in Table 25. Interrupts with multiple sources are OR'ed together and individual interrupt source control is provided in XRAM SFRs to mask the individual interrupt sources and provide the corresponding interrupt flags. Multifunction USR [7:0] pins control Interrupts 0 and 1. Dedicated external interrupt pins INT2 and INT3 control interrupts 2 and 3. The polarity of interrupts 2 and 3 is programmable in the MPU. Interrupts 4, 5 and 6 have multiple peripheral sources and are multiplexed to one of these three interrupts. The peripheral functions will be described in subsequent sections. Generic 80515 MPU literature states that interrupts 4 through 6 are defined as rising edge sensitive. Thus, the hardware signals attached to interrupts 4, 5 and 6 are converted to rising edge level by the hardware.

SFR (special function register) enable bits must be set to permit any of these interrupts to occur. Likewise, each interrupt has its own flag bit that is set by the interrupt hardware and is reset automatically by the MPU interrupt handler.

Table 25: External MPU Interrupts

External Interrupt	Connection	Polarity	Flag Reset
0	USR I/O High Priority	see USRIntCtlx	Automatic
1	USR I/O Low Priority	see USRIntCtlx	Automatic
2	External Interrupt Pin INT2	Edge selectable	Automatic
3	External Interrupt Pin INT3	Edge selectable	Automatic
4	Smart Card Interrupts	N/A	Automatic
5	Keypad	N/A	Automatic
6	I^2C, V_{DD}_Fault, Analog Comp	N/A	Automatic

Note: Interrupts 4, 5 and 6 have multiple interrupt sources and the flag bits are cleared upon reading of the corresponding register. To prevent any interrupts from being ignored, the register containing multiple interrupt flags should be stored temporary to allow each interrupt flag to be tested separately to see which interrupt(s) is/are pending.

Mode 0

Putting either timer/counter into mode 0 configures it as an 8-bit timer/counter with a divide-by-32 prescaler. In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1's to all 0's, it sets the timer overflow flag TF0. The overflow flag TF0 then can be used to request an interrupt. The counted input is enabled to the timer when TRx = 1 and either GATE = 0 or TX = 1 (setting GATE = 1 allows the timer to be controlled by external input TX, to facilitate pulse width measurements). TRx are control bits in the special function register TCON; GATE is in TMOD. The 13-bit register consists of all 8 bits of TH1 and the lower 5 bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Setting the run flag (TRx) does not clear the registers. Mode 0 operation is the same for timer 0 as for timer 1.

Mode 1

Mode 1 is the same as mode 0, except that the timer register is run with all 16 bits.

Mode 2

Mode 2 configures the timer register as an 8-bit counter (TLx) with automatic reload. The overflow from TLx not only sets TFx, but also reloads TLx with the contents of THx, which is preset by software. The reload leaves THx unchanged.

Mode 3

Mode 3 has different effects on timer 0 and timer 1. Timer 1 in mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in mode 3 establishes TL0 and TH0 as two separate counters. TL0 uses the timer 0 control bits: C/T, GATE, TR0, INT0, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from timer 1. Thus, TH0 now controls the "timer 1" interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer or counter. When timer 0 is in mode 3, timer 1 can be turned on and off by switching it out of and into its own mode 3, or can still be used by the serial channel as a baud rate generator, or in fact, in any application not requiring an interrupt from timer 1 itself.

Timer/Counter Control Register (TCON): 0x88 ← 0x00

Table 42: The TCON Register

MSB LSB

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Bit	Symbol	Function
TCON.7	TF1	Timer 1 overflow flag.
TCON.6	TR1	Not used for interrupt control.
TCON.5	TF0	Timer 0 overflow flag.
TCON.4	TR0	Not used for interrupt control.
TCON.3	IE1	Interrupt 1 edge flag is set by hardware when the falling edge on external interrupt int1 is observed. Cleared when an interrupt is processed.
TCON.2	IT1	Interrupt 1 type control bit. 1 selects falling edge and 0 selects low level for input pin to cause an interrupt.
TCON.1	IE0	Interrupt 0 edge flag is set by hardware when the falling edge on external interrupt int0 is observed. Cleared when an interrupt is processed.
TCON.0	IT0	Interrupt 0 type control bit. 1 selects falling edge and 0 sets low level for input pin to cause interrupt.

Interrupt Enable 1 Register (IEN1): 0xB8 ← 0x00

Table 44: The IEN1 Register

MSB							LSB
–	SWDT	EX6	EX5	EX4	EX3	EX2	–

Bit	Symbol	Function
IEN1.7	–	
IEN1.6	SWDT	Watchdog timer start/refresh flag. Set to activate/refresh the watchdog timer. When directly set after setting WDT, a watchdog timer refresh is performed. Bit SWDT is reset by the hardware 12 clock cycles after it has been set.
IEN1.5	EX6	EX6 = 0 – disable external interrupt 6.
IEN1.4	EX5	EX5 = 0 – disable external interrupt 5.
IEN1.3	EX4	EX4 = 0 – disable external interrupt 4.
IEN1.2	EX3	EX3 = 0 – disable external interrupt 3.
IEN1.1	EX2	EX2 = 0 – disable external interrupt 2.
IEN1.0	–	

Interrupt Priority 0 Register (IP0): 0xA9 ← 0x00

Table 45: The IP0 Register

MSB							LSB
–	WDTS	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0

Bit	Symbol	Function
IP0.6	WDTS	Watchdog timer status flag. Set when the watchdog timer has expired. The internal reset will be generated, but this bit will not be cleared by the reset. This allows the user program to determine if the watchdog timer caused the reset to occur and respond accordingly. Can be read and cleared by software.

Note: The remaining bits in the IP0 register are not used for watchdog control.

Watchdog Timer Reload Register (WDTREL): 0x86 ← 0x00

Table 46: The WDTREL Register

MSB							LSB
WDPSEL	WDREL6	WDREL5	WDREL4	WDREL3	WDREL2	WDREL1	WDREL0

Bit	Symbol	Function
WDTREL.7	WDPSEL	Prescaler select bit. When set, the watchdog is clocked through an additional divide-by-16 prescaler.
WDTREL.6 to WDTREL.0	WDREL6-0	Seven bit reload value for the high-byte of the watchdog timer. This value is loaded to the WDT when a refresh is triggered by a consecutive setting of bits WDT and SWDT.

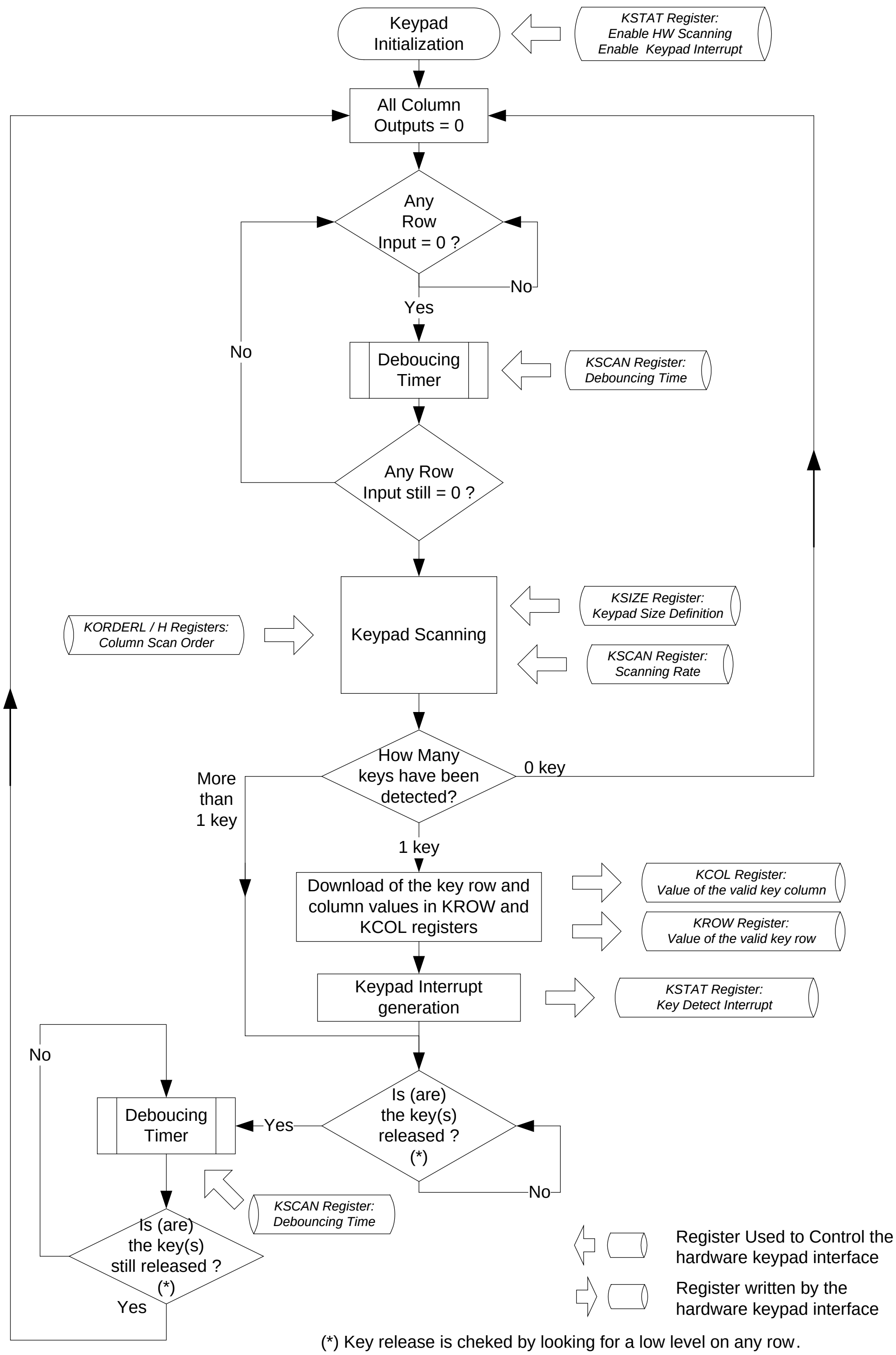

Figure 13: Keypad Interface Flow Chart

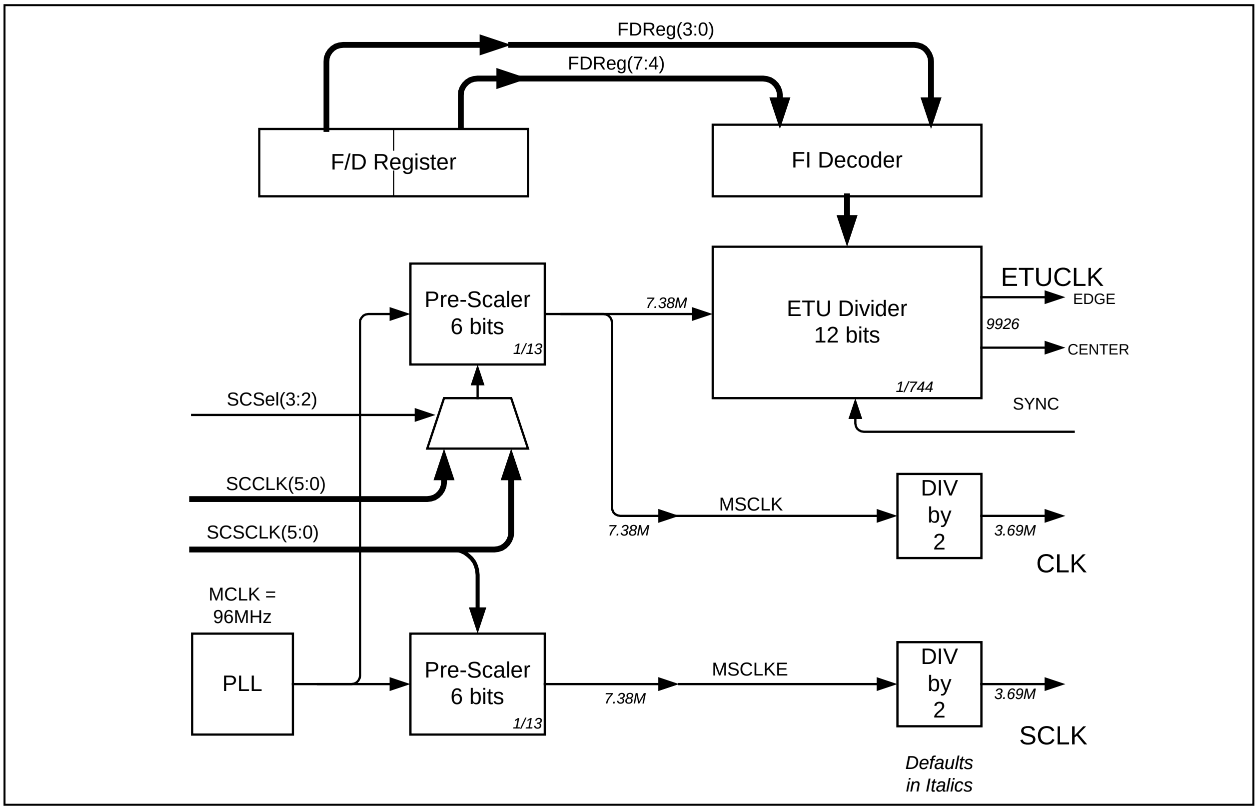

Figure 18: Smart Card CLK and ETU Generation

There are two, two-byte FIFOs that are used to buffer transmit and receive data. During a T=0 processing, if a parity error is detected by the 73S1210F during message reception, an error signal (BREAK) will be generated to the smart card. The byte received will be discarded and the firmware notified of the error. Break generation and receive byte dropping can be disabled under firmware control. During the transmission of a byte, if an error signal (BREAK) is detected, the last byte is retransmitted again and the firmware notified. Retransmission can be disabled by firmware. When a correct byte is received, an interrupt is generated to the firmware, which then reads the byte from the receive FIFO. Receive overruns are detected by the hardware and reported via an interrupt. During transmission of a message, the firmware will write bytes into the transmit FIFO. The hardware will send them to the smart card. When the last byte of a message has been written, the firmware will need to set the LASTTX bit in the STXCtl SFR. This will cause the hardware to insert the CRC/LRC if in a T=1 protocol mode. CRC/LRC generation/checking is only provided during T=1 processing. Firmware will need to instruct the smart function to go into receive mode after this last transmit data byte if it expects a response from the smart card. At the end of the smart card response, the firmware will put the interface back into transmit mode if appropriate.

The hardware can check for the following card-related timeouts:

- Character Waiting Time (CWT)
- Block Waiting Time (BWT)
- Initial Waiting Time (IWT)

The firmware will load the Wait Time with the appropriate value for the operating mode at the appropriate time. Figure 19 shows the guard, block, wait and ATR time definitions. If a timeout occurs, an interrupt will be generated and the firmware can take appropriate recovery steps. Support is provided for adding additional guard times between characters using the Extra Guard Time register (EGT), and between the last byte received by the 73S1210F and the first byte transmitted by the 73S1210F using the Block Guard Time register (BGT). Other than the protocol checks described above, the firmware is responsible for all protocol checking and error recovery.

Smart Card Interrupt Register (SCInt): 0xFE01 ← 0x00

When the smart card interrupt is asserted, the firmware can read this register to determine the actual cause of the interrupt. The bits are cleared when this register is read. Each interrupt can be disabled by the Smart Card Interrupt Enable register. Error processing must be handled by the firmware. This register relates to the interface that is active – see the SCSel register (above).

Table 73: The SCInt Register

MSB LSB

WAITTO	CRDEVT	VCCTMRI	RXDAV	TXEVT	TXSENT	TXERR	RXERR

Bit	Symbol	Function
SCInt.7	WAITTO	Wait Timeout - An ATR or card wait timeout has occurred. In sync mode, this interrupt is asserted when the RLen counter (it advances on falling edges of CLK/ETU) reaches the loaded (max) value. This bit is cleared when the SCInt register is read. When running in Synchronous Clock Stop Mode, this bit becomes RLenINT interrupt (set when the Rlen counter reaches the terminal count).
SCInt.6	CRDEVT	Card Event - A card event is signaled via pin DETCARD either when the Card was inserted or removed (read the CRDCtl register to determine card presence) or there was a fault condition in the interface circuitry. This bit is functional even if the smart card logic clock is disabled and when the PWRDN bit is set. This bit is cleared when the SCInt register is read.
SCInt.5	VCCTMRI	VCC Timer - This bit is set when the VCCTMR times out. This bit is cleared when the SCInt register is read.
SCInt.4	RXDAV	Rx Data Available - Data was received from the smart card because the Rx FIFO is not empty. In bypass mode, this interrupt is generated on a falling edge of the smart card I/O line. After receiving this interrupt in bypass mode, firmware should disable it until the firmware has received the entire byte and is waiting for the next start delimiter. This bit is cleared when there is no RX data available in the RX FIFO.
SCInt.3	TXEVNT	TX Event - Set whenever the TXEMTY or TXFULL bits are set in the SRXCtl SFR. This bit is cleared when the STXCtl register is read.
SCInt.2	TXSENT	TX Sent - Set whenever the ISO UART has successfully transmitted a byte to the smart card. Also set when a CRC/LRC byte is sent in T=1 mode. Will not be set in T=0 when a break is detected at the end of a byte (when break detection is enabled). This bit is cleared when the SCInt register is read.
SCInt.1	TXERR	TX Error - An error was detected during the transmission of data to the smart card as indicated by either BREAKD or TXUNDR bit being set in the STXCtl SFR. Additional information can be found in that register description. This bit is cleared when the STXCtl register is read.
SCInt.0	RXERR	RX Error - An error was detected during the reception of data from the smart card. Additional information can be found in the SRXCtl register. This interrupt will be asserted for RXOVRR, or RX Parity error events. This bit is cleared when the SRXCtl register is read.

Card Status/Control Register (CRDCtl): 0xFE05 ← 0x00

This register is used to configure the card detect pin (DETCARD) and monitor card detect status. This register must be written to properly configure Debounce, Detect_Polarity (= 0 or = 1), and the pull-up/down enable before setting CDETEN. The card detect logic is functional even without smart card logic clock. When the PWRDN bit is set = 1, no debounce is provided but card presence is operable.

Table 77: The CRDCtl Register

MSB							LSB
DEBOUN	CDETEN	–	–	DETPOL	PUENB	PDEN	CARDIN

Bit	Symbol	Function
CRDCtl.7	DEBOUN	Debounce - When set = 1, this will enable hardware debounce of the card detect pin. The debounce function shall wait for 64ms of stable card detect assertion before setting the CARDIN bit. This counter/timer uses the keypad clock as a source of 1kHz signal. De-assertion of the CARDIN bit is immediate upon de-assertion of the card detect pin(s).
CRDCtl.6	CDETEN	Card Detect Enable - When set = 1, activates card detection input. Default upon power-on reset is 0.
CRDCtl.5	–	
CRDCtl.4	–	
CRDCtl.3	DETPOL	Detect Polarity - When set = 1, the DETCARD pin shall interpret a logic 1 as card present.
CRDCtl.2	PUENB	Enable pull-up current on DETCARD pin (active low).
CRDCtl.1	PDEN	Enable pull-down current on DETCARD pin.
CRDCtl.0	CARDIN	Card Inserted - (Read only). 1 = card inserted, 0 = card not inserted. A change in the value of this bit is a “card event.” A read of this bit indicates whether smart card is inserted or not inserted in conjunction with the DETPOL setting.

TX Control/Status Register (STXCtl): 0xFE06 ← 0x00

This register is used to control transmission of data to the smart card. Some control and some status bits are in this register.

Table 78: The STXCtl Register

MSB							LSB
I2CMODE	–	TXFULL	TXEMTY	TXUNDR	LASTTX	TX/RXB	BREAKD

Bit	Symbol	Function
STXCtl.7	I2CMODE	I2C Mode - When in sync mode and this bit is set, and when the RLen count value = max or 0, the source of the smart card data for IO pin (or SIO pin) will be connected to the IO bit in SCCtl (or SCECtl) register rather than the TX FIFO. See the description for the Protocol Mode Register for more detail.
STXCtl.6	–	
STXCtl.5	TXFULL	TX FIFO is full. Additional writes may corrupt the contents of the FIFO. This bit it will remain set as long as the TX FIFO is full. Generates a TX_Event interrupt upon going full.
STXCtl.4	TXEMTY	1 = TX FIFO is empty, 0 = TX FIFO is not empty. If there is data in the TX FIFO, the circuit will transmit it to the smart card if in transmit mode. In T=1 mode, if the LASTTX bit is set and the hardware is configured to transmit the CRC/LRC, the TXEMTY will not be set until the CRC/LRC is transmitted. In T=0, if the LASTTX bit is set, TXEMTY will be set after the last word has been successfully transmitted to the smart card. Generates a TXEVNT interrupt upon going empty.
STXCtl.3	TXUNDR	TX Underrrun - (Read only) Asserted when a transmit under-run condition has occurred. An under-run condition is defined as an empty TX FIFO when the last data word has been successfully transmitted to the smart card and the LASTTX bit was not set. No special processing is performed by the hardware if this condition occurs. Cleared when read by firmware. This bit generates a TXERR interrupt.
STXCtl.2	LASTTX	Last TX Byte - Set by firmware (in both T=0 and T=1) when the last byte in the current message has been written into the transmit FIFO. In T=1 mode, the CRC/LRC will be appended to the message. Should be set after the last byte has been written into the transmit FIFO. Should be cleared by firmware before writing first byte of next message into the transmit FIFO. Used in T=0 to determine when to set TXEMTY.
STXCtl.1	TX/RXB	1 = Transmit mode, 0 = Receive mode. Configures the hardware to be receiving from or transmitting to the smart card. Determines which counters should be enabled. This bit should be set to receive mode prior to switching to another interface. Setting and resetting this bit shall initialize the CRC logic. If LASTTX is set, this bit can be reset to RX mode and UART logic will automatically change mode to RX when TX operation is completed (TX_Empty = 1).
STXCtl.0	BREAKD	Break Detected - (Read only) 1 = A break has been detected on the I/O line indicating that the smart card detected a parity error. Cleared when read. This bit generates a TXERR interrupt.

SC Clock Configuration Register (SCCLK): 0xFE0F ← 0x0C

This register controls the internal smart card (CLK) clock generation.

Table 86: The SCCLK Register

MSB							LSB
–	–	ICLKFS.5	ICLKFS.4	ICLKFS.3	ICLKFS.2	ICLKFS.1	ICLKFS.0

Bit	Symbol	Function
SCCLK.7	–	
SCCLK.6	–	
SCCLK.5	ICLKFS.5	Internal Smart Card CLK Frequency Select - Division factor to determine internal smart card CLK frequency. MCLK clock is divided by (register value + 1) to clock the ETU divider, and then by 2 to generate CLK. Default ratio is 13. The programmed value in this register is applied to the divider after this value is written, in such a manner as to produce a glitch-free output, regardless of the selection of active interface. A register value = 0 will default to the same effect as register value = 1.
SCCLK.4	ICLKFS.4	
SCCLK.3	ICLKFS.3	
SCCLK.2	ICLKFS.2	
SCCLK.1	ICLKFS.1	
SCCLK.0	ICLKFS.0	

External SC Clock Configuration Register (SCECLK): 0xFE10 ← 0x0C

This register controls the external smart card (SCLK) clock generation.

Table 87: The SCECLK Register

MSB							LSB
–	–	ECLKFS.5	ECLKFS.4	ECLKFS.3	ECLKFS.2	ECLKFS.1	ECLKFS.0

Bit	Symbol	Function
SCECLK.7	–	
SCECLK.6	–	
SCECLK.5	ECLKFS.5	External Smart Card CLK Frequency Select - Division factor to determine external smart card CLK frequency. MCLK clock is divided by (register value + 1) to clock the ETU divider, and then by 2 to generate SCLK. Default ratio is 13. The programmed value in this register is applied to the divider after this value is written, in such a manner as to produce a glitch-free output, regardless of the selection of active interface. A register value = 0 will default to the same effect as register value = 1.
SCECLK.4	ECLKFS.4	
SCECLK.3	ECLKFS.3	
SCECLK.2	ECLKFS.2	
SCECLK.1	ECLKFS.1	
SCECLK.0	ECLKFS.0	

1.7.16 VDD Fault Detect Function

The 73S1210F contains a circuit to detect a low-voltage condition on the supply voltage V_{DD}. If enabled, it will deactivate the active internal smart card interface when V_{DD} falls below the V_{DD} Fault threshold. The register configures the V_{DD} Fault threshold for the nominal default of 2.3V* or a user selectable threshold. The user's code may load a different value using the FOVRVDDF bit = 1 after the power-up cycle has completed.

VDDFault Control Register (VDDFCtl): 0xFFD4 ← 0x00

Table 108: The VDDFCtl Register

MSB							LSB
–	FOVRVDDF	VDDFLTEN	–	STXDAT.3	VDDFTH.2	VDDFTH.1	VDDFTH.0

Bit	Symbol	Function
VDDFCtl.7	–	
VDDFCtl.6	FOVRVDDF	Setting this bit high will allow the VDDFLT(2:0) bits set in this register to control the VDDFault threshold. When this bit is set low, the VDDFault threshold will be set to the factory default setting of 2.3V*.
VDDFCtl.5	VDDFLTEN	Set = 1 will disable VDD Fault operation.
VDDFCtl.4	–	
VDDFCtl.3	–	
VDDFCtl.2	VDDFTH.2	VDD Fault Threshold. Bit Value(2:0) VDDFault Voltage 000 2.3 (nominal default) 001 2.4 010 2.5 011 2.6 100 2.7 101 2.8 110 2.9 111 3.0
VDDFCtl.1	VDDFTH.1	
VDDFCtl.0	VDDFTH.0	

* Note: The V_{DD} Fault factory default can be set to any threshold as defined by bits VDDFTH(2:0). The 73S1210F has the capability to burn fuses at the factory to set the factory default to any of these voltages. Contact Teridian for further details.