AMD Xilinx - XC2S100E-6FT256C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	600
Number of Logic Elements/Cells	2700
Total RAM Bits	40960
Number of I/O	182
Number of Gates	100000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s100e-6ft256c

Spartan-IIE FPGA Family: Introduction and Ordering Information

DS077-1 (v3.0) August 9, 2013

Product Specification

Introduction

The Spartan®-IIE Field-Programmable Gate Array family gives users high performance, abundant logic resources, and a rich feature set, all at an exceptionally low price. The seven-member family offers densities ranging from 50,000 to 600,000 system gates, as shown in Table 1. System performance is supported beyond 200 MHz.

Features include block RAM (to 288K bits), distributed RAM (to 221,184 bits), 19 selectable I/O standards, and four DLLs (Delay-Locked Loops). Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

The Spartan-IIE family is a superior alternative to mask-programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary (impossible with ASICs).

Features

- Second generation ASIC replacement technology
  - Densities as high as 15,552 logic cells with up to 600,000 system gates
  - Streamlined features based on Virtex®-E FPGA architecture
  - Unlimited in-system reprogrammability
  - Very low cost
  - Cost-effective 0.15 micron technology
- System level features
  - SelectRAM™ hierarchical memory:
    - 16 bits/LUT distributed RAM
    - Configurable 4K-bit true dual-port block RAM
    - Fast interfaces to external RAM
  - Fully 3.3V PCI compliant to 64 bits at 66 MHz and CardBus compliant
  - Low-power segmented routing architecture
  - Dedicated carry logic for high-speed arithmetic
  - Efficient multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with enable, set, reset
  - Four dedicated DLLs for advanced clock control
    - Eliminate clock distribution delay
    - Multiply, divide, or phase shift
  - Four primary low-skew global clock distribution nets
  - IEEE 1149.1 compatible boundary scan logic
- Versatile I/O and packaging
  - Pb-free package options
  - Low-cost packages available in all densities
  - Family footprint compatibility in common packages
  - 19 high-performance interface standards
    - LVTTL, LVCMOS, HSTL, SSTL, AGP, CTT, GTL
    - LVDS and LVPECL differential I/O
  - Up to 205 differential I/O pairs that can be input, output, or bidirectional
  - Hot swap I/O (CompactPCI friendly)
- Core logic powered at 1.8V and I/Os powered at 1.5V, 2.5V, or 3.3V
- Fully supported by powerful Xilinx® ISE® development system
  - Fully automatic mapping, placement, and routing
  - Integrated with design entry and verification tools
  - Extensive IP library including DSP functions and soft processors

Table 1: **Spartan-IIE FPGA Family Members**

Device	Logic Cells	Typical System Gate Range (Logic and RAM)	CLB Array (R x C)	Total CLBs	Maximum Available User I/O(1)	Maximum Differential I/O Pairs	Distributed RAM Bits	Block RAM Bits
XC2S50E	1,728	23,000 - 50,000	16 x 24	384	182	83	24,576	32K
XC2S100E	2,700	37,000 - 100,000	20 x 30	600	202	86	38,400	40K
XC2S150E	3,888	52,000 - 150,000	24 x 36	864	265	114	55,296	48K
XC2S200E	5,292	71,000 - 200,000	28 x 42	1,176	289	120	75,264	56K
XC2S300E	6,912	93,000 - 300,000	32 x 48	1,536	329	120	98,304	64K
XC2S400E	10,800	145,000 - 400,000	40 x 60	2,400	410	172	153,600	160K
XC2S600E	15,552	210,000 - 600,000	48 x 72	3,456	514	205	221,184	288K

Notes:

1. User I/O counts include the four global clock/user input pins. See details in Table 2, page 5

General Overview

The Spartan-IIE family of FPGAs have a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), surrounded by a perimeter of programmable Input/Output Blocks (IOBs). There are four Delay-Locked Loops (DLLs), one at each corner of the die. Two columns of block RAM lie on opposite sides of the die, between the CLBs and the IOB columns. The XC2S400E has four columns and the XC2S600E has six columns of block RAM. These functional elements are interconnected by a powerful hierarchy of versatile routing channels (see Figure 1).

Spartan-IIE FPGAs are customized by loading configuration data into internal static memory cells. Unlimited reprogramming cycles are possible with this approach. Stored values in these cells determine logic functions and interconnections implemented in the FPGA. Configuration data can be read from an external serial PROM (master serial mode), or written into the FPGA in slave serial, slave parallel, or Boundary Scan modes. Xilinx offers multiple types of low-cost configuration solutions including the Platform Flash in-system programmable configuration PROMs.

Spartan-IIE FPGAs are typically used in high-volume applications where the versatility of a fast programmable solution adds benefits. Spartan-IIE FPGAs are ideal for shortening product development cycles while offering a cost-effective solution for high volume production.

Spartan-IIE FPGAs achieve high-performance, low-cost operation through advanced architecture and semiconductor technology. Spartan-IIE devices provide system clock rates beyond 200 MHz. In addition to the conventional benefits of high-volume programmable logic solutions, Spartan-IIE FPGAs also offer on-chip synchronous single-port and dual-port RAM (block and distributed form), DLL clock drivers, programmable set and reset on all flip-flops, fast carry logic, and many other features.

Spartan-IIE Family Compared to Spartan-II Family

- Higher density and more I/O
- Higher performance
- Unique pinouts in cost-effective packages
- Differential signaling
  - LVDS, Bus LVDS, LVPECL
- V_{CCINT} = 1.8V
  - Lower power
  - 5V tolerance with external resistor
  - 3V tolerance directly
- PCI, LVTTL, and LVCMOS2 input buffers powered by V_{CCO} instead of V_{CCINT}
- Unique larger bitstream

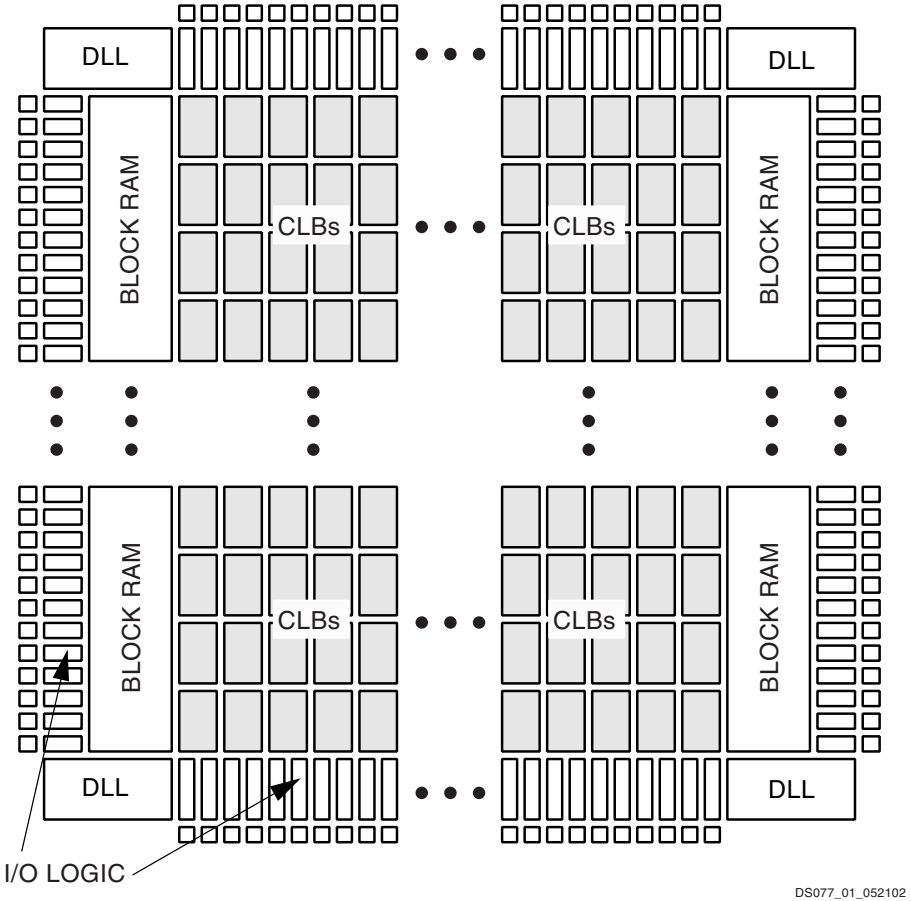


Figure 1: **Basic Spartan-IIE Family FPGA Block Diagram**

Architectural Description

Spartan-IIE FPGA Array

The Spartan®-IIE user-programmable gate array, shown in Figure 3, is composed of five major configurable elements:

- IOBs provide the interface between the package pins and the internal logic
- CLBs provide the functional elements for constructing most logic
- Dedicated block RAM memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- Versatile multi-level interconnect structure

As can be seen in Figure 3, the CLBs form the central logic structure with easy access to all support and routing structures. The IOBs are located around all the logic and memory elements for easy and quick routing of signals on and off the chip.

Values stored in static memory cells control all the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

Each of these elements will be discussed in detail in the following sections.

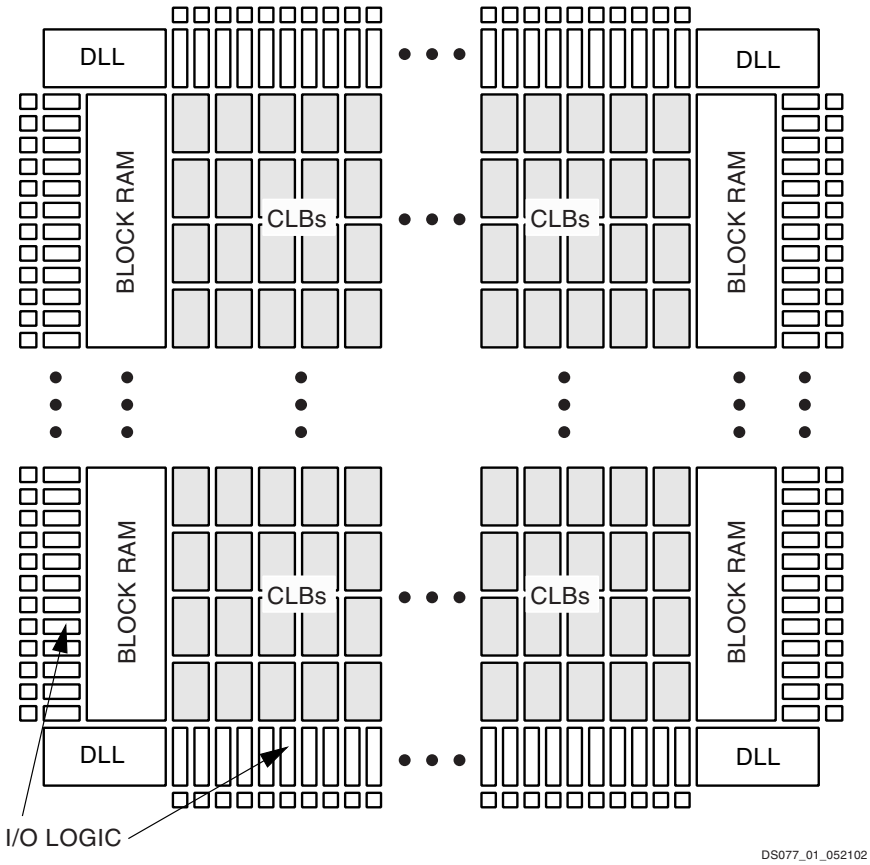


Figure 3: **Basic Spartan-IIE Family FPGA Block Diagram**

Table 8: **Boundary-Scan Instructions *(Continued)***

Boundary-Scan Command	Binary Code[4:0]	Description
INTEST	00111	Enables boundary-scan INTEST operation
USERCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIGHZ	01010	Disables output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions

The public boundary-scan instructions are available prior to configuration, except for USER1 and USER2. After configuration, the public instructions remain available together with any USERCODE instructions installed during the configuration. While the SAMPLE/PRELOAD and BYPASS instructions are available during configuration, it is recommended that boundary-scan operations not be performed during this transitional period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

To facilitate internal scan chains, the User Register provides three outputs (Reset, Update, and Shift) that represent the corresponding states in the boundary-scan internal state machine.

Figure 14 is a diagram of the Spartan-IIE family boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

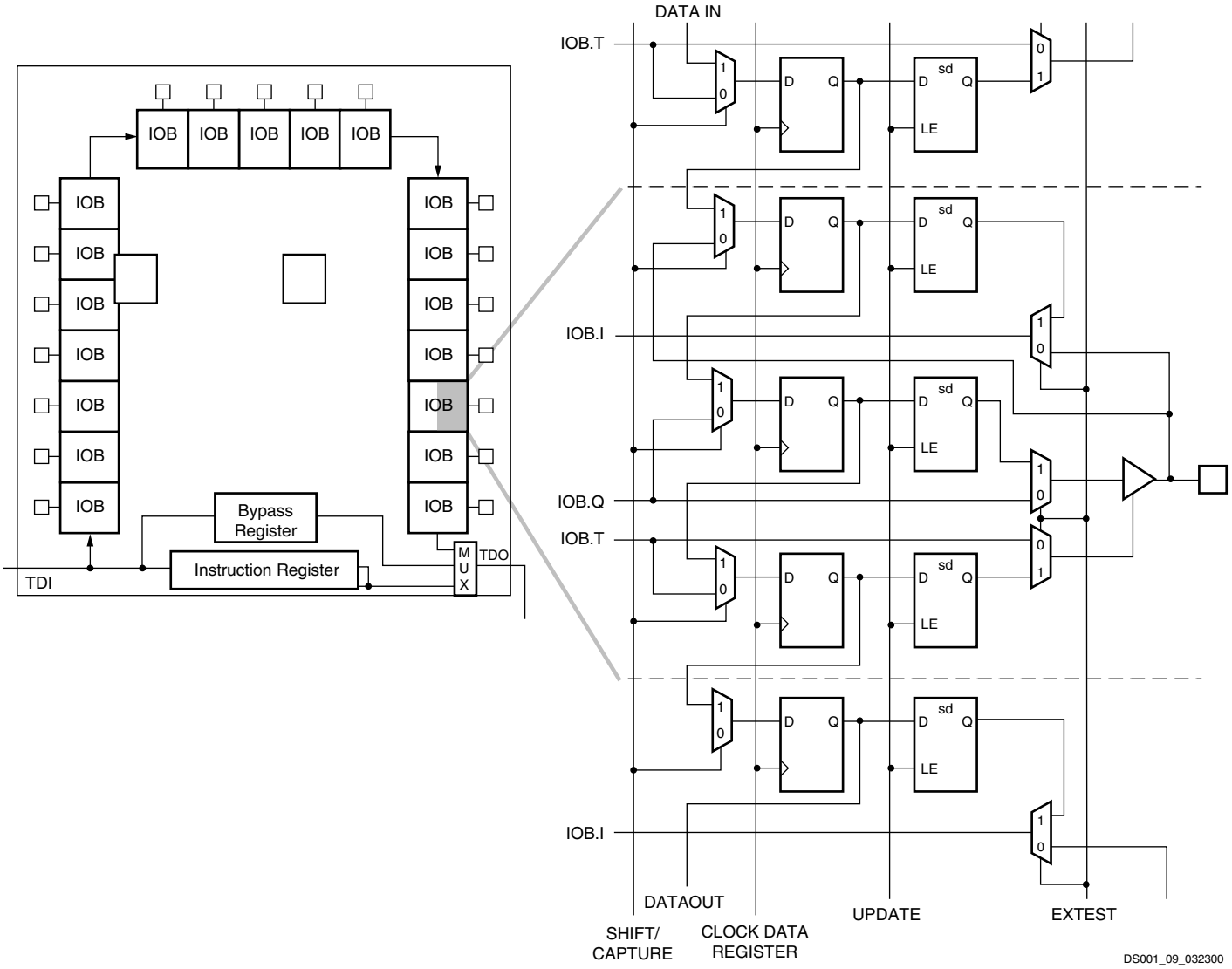


Figure 14: **Spartan-IIE Family Boundary Scan Logic**

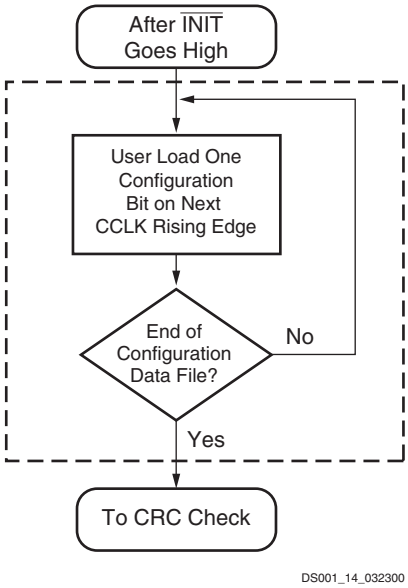


Figure 18: **Loading Serial Mode Configuration Data**

Slave Serial Mode

In Slave Serial mode, the FPGA's CCLK pin is driven by an external source, allowing the FPGA to be configured from other logic devices such as microprocessors or in a daisy-chain configuration. Figure 19 shows connections for a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-IIE device in slave serial mode should be connected as shown for the third device from the left. Slave Serial mode is selected by a <11x> on the mode pins (M0, M1, M2). The weak pull-ups on the mode pins make slave serial the default mode if the pins are left unconnected.

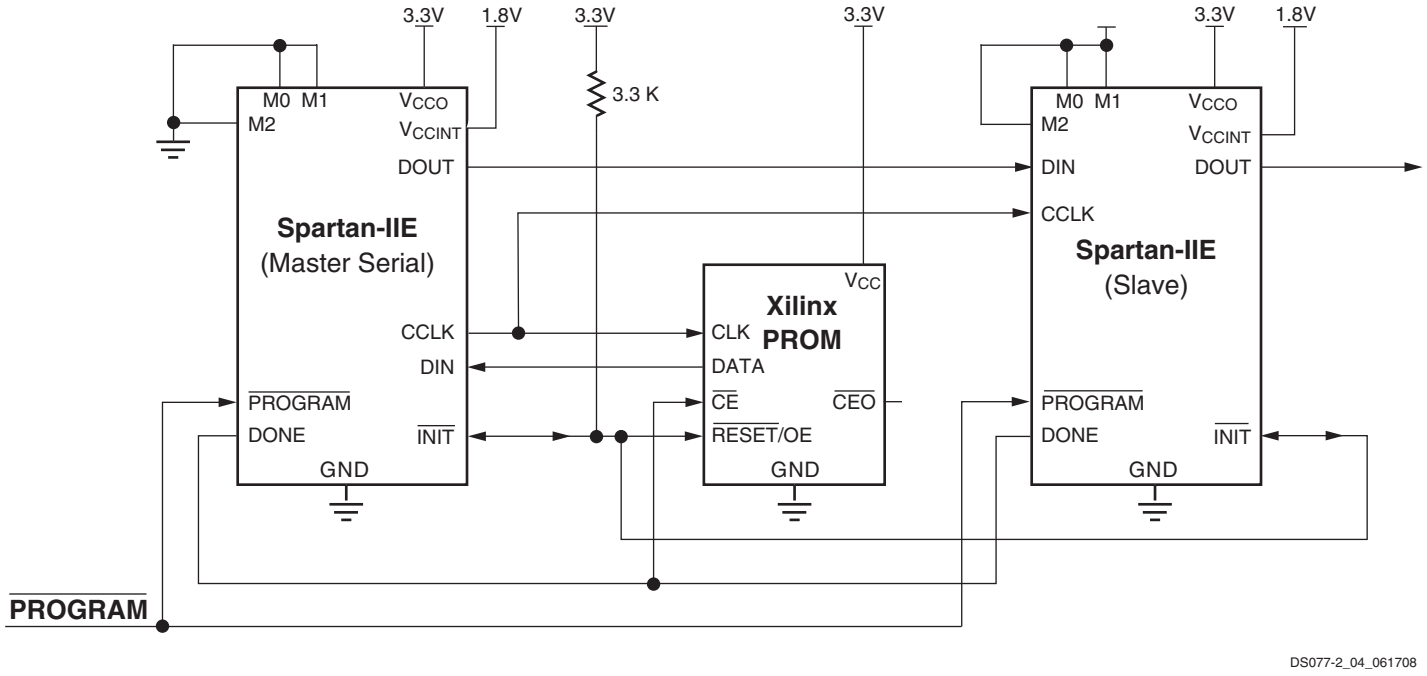
The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

Timing for Slave Serial mode is shown in Figure 24, page 49.

Daisy Chain

Multiple FPGAs in Slave Serial mode can be daisy-chained for configuration from a single source. After an FPGA is configured, data for the next device is sent to the DOUT pin. Data on the DOUT pin changes on the rising edge of CCLK. Note that DOUT changes on the falling edge of CCLK for some Xilinx families but mixed daisy chains are allowed. Configuration must be delayed until $\overline{\text{INIT}}$ pins of all daisy-chained FPGAs are High. For more information, see Start-up, page 23.

The maximum amount of data that can be sent to the DOUT pin for a serial daisy chain is 2^{20}-1 (1,048,575) 32-bit words, or 33,554,400 bits, which is approximately 8 XC2S600E bitstreams. The configuration bitstream of downstream devices is limited to this size.



Notes:
1. If the DriveDone configuration option is not active for any of the FPGAs, pull up DONE with a 330Ω resistor.

Figure 19: **Master/Slave Serial Configuration Circuit Diagram**

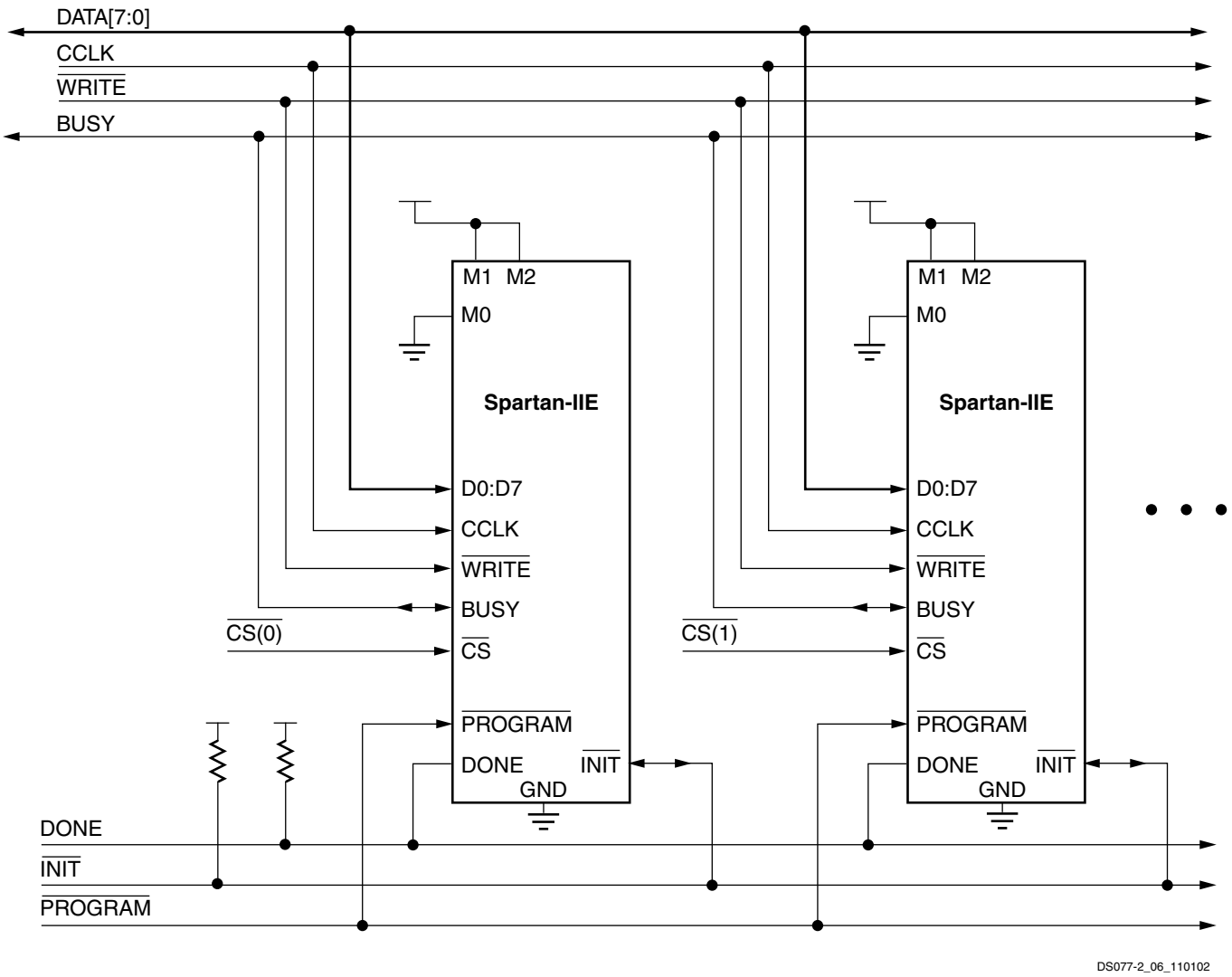


Figure 20: **Slave Parallel Configuration Circuit Diagram**

Multiple Spartan-IIE FPGAs can be configured using the Slave Parallel mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, $\overline{\text{WRITE}}$, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the $\overline{\text{CS}}$ pin of each device in turn and writing the appropriate data. Sync-to-DONE start-up timing is used to ensure that the start-up sequence does not begin until all the FPGAs have been loaded. See Start-up, page 23.

Write

When using the Slave Parallel Mode, write operations send packets of byte-wide configuration data into the FPGA. Figure 21, page 28 shows a flowchart of the write sequence used to load data into the Spartan-IIE FPGA. This is an expansion of the "Load Configuration Data Frames" block in Figure 16, page 23.

The timing for Slave Parallel mode is shown in Figure 26, page 50.

For the present example, the user holds $\overline{\text{WRITE}}$ and $\overline{\text{CS}}$ Low throughout the sequence of write operations. Note that when $\overline{\text{CS}}$ is asserted on successive CCLKs, $\overline{\text{WRITE}}$ must remain either asserted or deasserted. Otherwise an abort will be initiated, as in the next section.

1. Drive data onto D0-D7. Note that to avoid contention, the data source should not be enabled while $\overline{\text{CS}}$ is Low and $\overline{\text{WRITE}}$ is High. Similarly, while $\overline{\text{WRITE}}$ is High, no more than one device's $\overline{\text{CS}}$ should be asserted.
2. On the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this happens.
3. Repeat steps 1 and 2 until all the data has been sent.
4. Deassert $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL I	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	8	–8
HSTL III	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	24	–8
HSTL IV	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	48	–8
SSTL3 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	–8
SSTL3 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	–16
SSTL2 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.61	V_{REF} + 0.61	7.6	–7.6
SSTL2 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	15.2	–15.2
CTT	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.4	V_{REF} + 0.4	8	–8
AGP	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	Note (2)	Note (2)

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested.
2. Tested according to the relevant specifications.

LVDS DC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		2.375	2.5	2.625	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	1.25	1.425	1.6	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	0.9	1.075	1.25	V
V_{ODIFF}	Differential output voltage (Q – $\overline{Q}$), Q = High or ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	250	350	450	mV
V_{OCM}	Output common-mode voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.125	1.25	1.375	V
V_{IDIFF}	Differential input voltage (Q – $\overline{Q}$), Q = High or ($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25 V	100	350	-	mV
V_{ICM}	Input common-mode voltage	Differential input voltage = ±350 mV	0.2	1.25	2.2	V

LVPECL DC Specifications

These values are valid at the output of the source termination pack shown under LVPECL, with a 100Ω differential load only. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. The following table summarizes the DC output specifications of LVPECL.

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential input voltage	0.3	-	0.3	-	0.3	-	V

IOB Input Switching Characteristics(1)

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in IOB Input Delay Adjustments for Different Standards, page 38.

Symbol	Description	Device	Speed Grade				Units
			-7		-6		
			Min	Max	Min	Max	
Propagation Delays							
T_{IOPI}	Pad to I output, no delay	All	0.4	0.8	0.4	0.8	ns
T_{IOPID}	Pad to I output, with delay	All	0.5	1.0	0.5	1.0	ns
T_{IOPLI}	Pad to output IQ via transparent latch, no delay	All	0.7	1.5	0.7	1.6	ns
T_{IOPLID}	Pad to output IQ via transparent latch, with delay	XC2S50E	1.3	3.0	1.3	3.1	ns
		XC2S100E	1.3	3.0	1.3	3.1	ns
		XC2S150E	1.3	3.2	1.3	3.3	ns
		XC2S200E	1.3	3.2	1.3	3.3	ns
		XC2S300E	1.3	3.2	1.3	3.3	ns
		XC2S400E	1.4	3.2	1.4	3.4	ns
		XC2S600E	1.5	3.5	1.5	3.7	ns
Sequential Delays							
T_{IOCKIQ}	Clock CLK to output IQ	All	0.1	0.7	0.1	0.7	ns
Setup/Hold Times with Respect to Clock CLK							
T_{IOPICK} / T_{IOICKP}	Pad, no delay	All	1.4 / 0	-	1.5 / 0	-	ns
$T_{IOPICKD}$ / $T_{IOICKPD}$	Pad, with delay	XC2S50E	2.9 / 0	-	2.9 / 0	-	ns
		XC2S100E	2.9 / 0	-	2.9 / 0	-	ns
		XC2S150E	3.1 / 0	-	3.1 / 0	-	ns
		XC2S200E	3.1 / 0	-	3.1 / 0	-	ns
		XC2S300E	3.1 / 0	-	3.1 / 0	-	ns
		XC2S400E	3.2 / 0	-	3.2 / 0	-	ns
		XC2S600E	3.5 / 0	-	3.5 / 0	-	ns
$T_{IOICECK}$ / $T_{IOCKICE}$	ICE input	All	0.7 / 0.01	-	0.7 / 0.01	-	ns
Set/Reset Delays							
$T_{IOSRCKI}$	SR input (IFF, synchronous)	All	0.9	-	1.0	-	ns
T_{IOSRIQ}	SR input to IQ (asynchronous)	All	0.5	1.2	0.5	1.4	ns
T_{GSRQ}	GSR to output IQ	All	3.8	8.5	3.8	9.7	ns

Notes:
1. Input timing for LVTTL is measured at 1.4V. For other I/O standards, see the table Delay Measurement Methodology, page 41.

IOB Output Delay Adjustments for Different Standards(1)

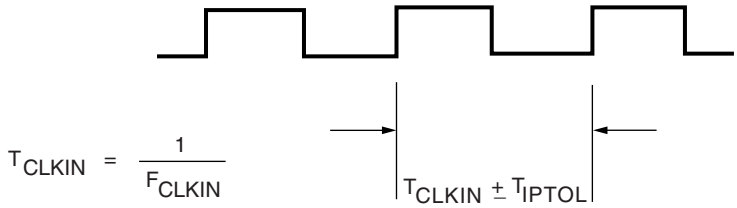
Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade		Units
			-7	-6	
Output Delay Adjustments (Adj)					
T_{OLVTTL_S2}	Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, C_{SL})	LVTTL, Slow, 2 mA	14.7	14.7	ns
T_{OLVTTL_S4}		4 mA	7.5	7.5	ns
T_{OLVTTL_S6}		6 mA	4.8	4.8	ns
T_{OLVTTL_S8}		8 mA	3.0	3.0	ns
T_{OLVTTL_S12}		12 mA	1.9	1.9	ns
T_{OLVTTL_S16}		16 mA	1.7	1.7	ns
T_{OLVTTL_S24}		24 mA	1.3	1.3	ns
T_{OLVTTL_F2}		LVTTL, Fast, 2 mA	13.1	13.1	ns
T_{OLVTTL_F4}		4 mA	5.3	5.3	ns
T_{OLVTTL_F6}		6 mA	3.1	3.1	ns
T_{OLVTTL_F8}		8 mA	1.0	1.0	ns
T_{OLVTTL_F12}		12 mA	0	0	ns
T_{OLVTTL_F16}		16 mA	–0.05	–0.05	ns
T_{OLVTTL_F24}		24 mA	–0.20	–0.20	ns
$T_{OLVCMOS2}$		LVCMOS2	0.09	0.09	ns
$T_{OLVCMOS18}$		LVCMOS18	0.7	0.7	ns
T_{OLVDS}		LVDS	–1.2	–1.2	ns
$T_{OLVPECL}$		LVPECL	–0.41	–0.41	ns
T_{OPCI33_3}		PCI, 33 MHz, 3.3V	2.3	2.3	ns
T_{OPCI66_3}		PCI, 66 MHz, 3.3V	–0.41	–0.41	ns
T_{OGTL}		GTL	0.49	0.49	ns
T_{OGTLP}		GTL+	0.8	0.8	ns
T_{OHSTL_I}		HSTL I	–0.51	–0.51	ns
T_{OHSTL_III}		HSTL III	–0.91	–0.91	ns
T_{OHSTL_IV}		HSTL IV	–1.01	–1.01	ns
T_{OSSTL2_I}		SSTL2 I	–0.51	–0.51	ns
T_{OSSLT2_II}		SSTL2 II	–0.91	–0.91	ns
T_{OSSTL3_I}		SSTL3 I	–0.51	–0.51	ns
T_{OSSTL3_II}		SSTL3 II	–1.01	–1.01	ns
T_{OCTT}		CTT	–0.61	–0.61	ns
T_{OAGP}		AGP	–0.91	–0.91	ns

Notes:

1. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see the tables Constants for Calculating T_{IOOP} and Delay Measurement Methodology, page 41.

Period Tolerance: the allowed input clock period change in nanoseconds.



Output Jitter: the difference between an ideal reference clock edge and the actual design.

Phase Offset and Maximum Phase Difference

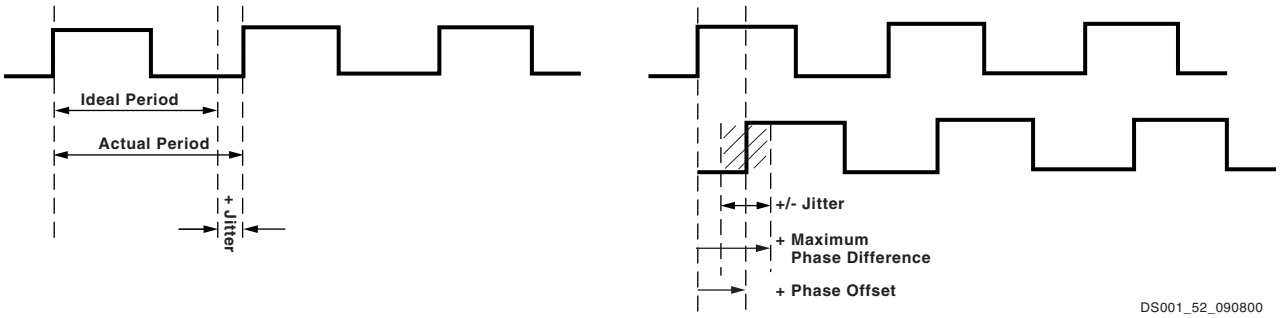


Figure 22: **Period Tolerance and Clock Jitter**

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Combinatorial Delays						
T_{ILO}	4-input function: F/G inputs to X/Y outputs	0.18	0.42	0.18	0.47	ns
T_{IF5}	5-input function: F/G inputs to F5 output	0.3	0.8	0.3	0.9	ns
T_{IF5X}	5-input function: F/G inputs to X output	0.3	0.8	0.3	0.9	ns
T_{IF6Y}	6-input function: F/G inputs to Y output via F6 MUX	0.3	0.9	0.3	1.0	ns
T_{F5INY}	6-input function: F5IN input to Y output	0.04	0.2	0.04	0.22	ns
T_{IFNCTL}	Incremental delay routing through transparent latch to XQ/YQ outputs	-	0.7	-	0.8	ns
T_{BYYB}	BY input to YB output	0.18	0.46	0.18	0.51	ns
Sequential Delays						
T_{CKO}	FF clock CLK to XQ/YQ outputs	0.3	0.9	0.3	1.0	ns
T_{CKLO}	Latch clock CLK to XQ/YQ outputs	0.3	0.9	0.3	1.0	ns
Setup/Hold Times with Respect to Clock CLK						
T_{ICK} / T_{CKI}	4-input function: F/G inputs	1.0 / 0	-	1.1 / 0	-	ns
T_{IF5CK} / T_{CKIF5}	5-input function: F/G inputs	1.4 / 0	-	1.5 / 0	-	ns
T_{F5INCK} / T_{CKF5IN}	6-input function: F5IN input	0.8 / 0	-	0.8 / 0	-	ns
T_{IF6CK} / T_{CKIF6}	6-input function: F/G inputs via F6 MUX	1.5 / 0	-	1.6 / 0	-	ns
T_{DICK} / T_{CKDI}	BX/BY inputs	0.7 / 0	-	0.8 / 0	-	ns
T_{CECK} / T_{CKCE}	CE input	0.7 / 0	-	0.7 / 0	-	ns
T_{RCK} / T_{CKR}	SR/BY inputs (synchronous)	0.52 / 0	-	0.6 / 0	-	ns
Clock CLK						
T_{CH}	Pulse width, High	1.3	-	1.4	-	ns
T_{CL}	Pulse width, Low	1.3	-	1.4	-	ns
Set/Reset						
T_{RPW}	Pulse width, SR/BY inputs	2.1	-	2.4	-	ns
T_{RQ}	Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	0.3	0.9	0.3	1.0	ns
F_{TOG}	Toggle frequency (for export control)	-	400	-	357	MHz

CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Combinatorial Delays						
T_{OPX}	F operand inputs to X via XOR	-	0.8	-	0.8	ns
T_{OPXB}	F operand input to XB output	-	0.8	-	0.9	ns
T_{OPY}	F operand input to Y via XOR	-	1.4	-	1.5	ns
T_{OPYB}	F operand input to YB output	-	1.1	-	1.3	ns
T_{OPCYF}	F operand input to COUT output	-	0.9	-	1.0	ns
T_{OPGY}	G operand inputs to Y via XOR	-	0.8	-	0.9	ns
T_{OPGYB}	G operand input to YB output	-	1.2	-	1.3	ns
T_{OPCYG}	G operand input to COUT output	-	0.9	-	1.0	ns
T_{BXCY}	BX initialization input to COUT	-	0.51	-	0.6	ns
T_{CINX}	CIN input to X output via XOR	-	0.6	-	0.7	ns
T_{CINXB}	CIN input to XB	-	0.07	-	0.1	ns
T_{CINY}	CIN input to Y via XOR	-	0.7	-	0.7	ns
T_{CINYB}	CIN input to YB	-	0.4	-	0.5	ns
T_{BYP}	CIN input to COUT output	-	0.14	-	0.15	ns
Multiplier Operation						
T_{FANDXB}	F1/2 operand inputs to XB output via AND	-	0.35	-	0.4	ns
T_{FANDYB}	F1/2 operand inputs to YB output via AND	-	0.7	-	0.8	ns
T_{FANDCY}	F1/2 operand inputs to COUT output via AND	-	0.5	-	0.6	ns
T_{GANDYB}	G1/2 operand inputs to YB output via AND	-	0.6	-	0.7	ns
T_{GANDCY}	G1/2 operand inputs to COUT output via AND	-	0.3	-	0.4	ns
Setup/Hold Times with Respect to Clock CLK						
T_{CCKX} / T_{CKCX}	CIN input to FFX	1.2 / 0	-	1.3 / 0	-	ns
T_{CCKY} / T_{CKCY}	CIN input to FFY	1.2 / 0	-	1.3 / 0	-	ns

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 1, L6P	1	P178	XC2S50E, 200E, 300E	All
I/O, L6N	1	P179	XC2S50E, 200E, 300E	-
I/O	1	P180	-	-
I/O (DLL), L5P	1	P181	-	-
GCK2, I	1	P182	-	-
GND	-	P183	-	-
VCCO	-	P184	-	-
GCK3, I	0	P185	-	-
VCCINT	-	P186	-	-
I/O (DLL), L5N	0	P187	-	-
I/O, L4P	0	P188	XC2S50E, 200E, 300E	-
I/O, VREF Bank 0, L4N	0	P189	XC2S50E, 200E, 300E	All
GND	-	P190	-	-
I/O, L3P	0	P191	XC2S50E, 200E, 300E	-
I/O, L3N	0	P192	XC2S50E, 200E, 300E	-
I/O, L2P	0	P193	XC2S50E, 100E, 200E, 300E	-
I/O, L2N	0	P194	XC2S50E, 100E, 200E, 300E	-
VCCINT	-	P195	-	-
VCCO	-	P196	-	-
GND	-	P197	-	-
I/O, L1P	0	P198	XC2S50E, 100E, 200E, 300E	-
I/O, L1N	0	P199	XC2S50E, 100E, 200E, 300E	XC2S100E, 150E, 200E, 300E
I/O	0	P200	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O	0	P201	-	-
I/O, L0P_YY	0	P202	All	-
I/O, VREF Bank 0, L0N_YY	0	P203	All	All
I/O	0	P204	-	-
I/O	0	P205	-	XC2S200E, 300E
I/O	0	P206	-	-
TCK	-	P207	-	-
VCCO	-	P208	-	-

PQ208 Differential Clock Pins

Clock	Bank	P		N	
		Pin	Name	Pin	Name
GCK0	4	P80	GCK0, I	P81	I/O (DLL), L31P
GCK1	5	P77	GCK1, I	P75	I/O (DLL), L31N
GCK2	1	P182	GCK2, I	P181	I/O (DLL), L5P
GCK3	0	P185	GCK3, I	P187	I/O (DLL), L5N

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O (D5), L35N_YY	3	L13	All	-
I/O, L35P_YY	3	K14	All	-
I/O, L34N	3	K15	XC2S100E, 150E, 400E	-
I/O, L34P	3	K16	XC2S100E, 150E, 400E	-
I/O, L33N	3	L12	XC2S50E, 100E, 150E, 200E, 300E(1)	-
I/O, L33P	3	K12	XC2S50E, 100E, 150E, 200E, 300E(1)	-
I/O, VREF Bank 3, L32N	3	K13	XC2S50E, 300E, 400E	All
I/O (D4), L32P	3	J14	XC2S50E, 300E, 400E	-
I/O, L31N	3	J15	XC2S100E, 150E, 200E, 400E	-
I/O, L31P	3	J16	XC2S100E, 150E, 200E, 400E	XC2S400E
I/O (TRDY)	3	J13	-	-
I/O (IRDY), L30N_YY	2	H16	All	-
I/O, L30P_YY	2	G16	All	-
I/O, L29N	2	H14	XC2S100E, 150E, 200E, 400E	XC2S400E
I/O, L29P	2	H15	XC2S100E, 150E, 200E, 400E	-
I/O (D3), L28N	2	G15	XC2S50E, 300E, 400E	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 2, L28P	2	F16	XC2S50E, 300E, 400E	All
I/O, L27N	2	H13	XC2S50E, 100E, 150E, 200E, 300E(1)	-
I/O, L27P	2	G14	XC2S50E, 100E, 150E, 200E, 300E(2)	-
I/O, L26N	2	F15	XC2S100E, 150E, 400E	-
I/O, L26P	2	E16	XC2S100E, 150E, 400E	-
I/O, L25N_YY	2	G13	All	-
I/O (D2), L25P_YY	2	F14	All	-
I/O (D1), L24N	2	E15	XC2S50E, 300E, 400E	-
I/O, L24P	2	D16	XC2S50E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L23N	2	F13	XC2S150E, 200E, 400E	-
I/O, L23P	2	E14	XC2S150E, 200E, 400E	-
I/O, L22N	2	D15	XC2S50E, 150E, 200E, 300E, 400E	-
I/O, VREF Bank 2, L22P	2	C16	XC2S50E, 150E, 200E, 300E, 400E	All
I/O, L21N	2	G12	XC2S50E, 100E, 200E, 300E	-
I/O, L21P	2	F12	XC2S50E, 100E, 200E, 300E	-
I/O, L20N	2	E13	XC2S100E, 200E, 300E	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L20P	2	D14	XC2S100E, 200E, 300E	XC2S200E, 300E, 400E
I/O (DIN, D0), L19N_YY	2	B16	All	-
I/O (DOUT, BUSY), L19P_YY	2	C15	All	-
CCLK	2	A15	-	-
TDO	2	B14	-	-
TDI	-	C13	-	-
I/O ($\overline{CS}$), L18P_YY	1	A14	All	-
I/O ($\overline{WRITE}$), L18N_YY	1	A13	All	-
I/O, L17P	1	B13	XC2S50E, 100E, 200E, 300E, 400E	XC2S200E, 300E, 400E
I/O, L17N	1	C12	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L16P_YY	1	B12	All	-
I/O, L16N_YY	1	A12	All	-
I/O, VREF Bank 1, L15P_YY	1	D12	All	All
I/O, L15N_YY	1	E11	All	-
I/O, L14P	1	D11	XC2S50E, 100E, 150E, 300E	-
I/O, L14N	1	C11	XC2S50E, 100E, 150E, 300E	-
I/O, L13P	1	B11	XC2S50E, 100E, 200E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L13N	1	A11	XC2S50E, 100E, 200E, 300E, 400E	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L12P	1	E10	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L12N	1	D10	XC2S50E, 100E, 200E, 300E, 400E	-
I/O	1	C10	-	-
I/O, L11P	1	B10	XC2S50E, 200E, 300E, 400E	-
I/O, L11N	1	A10	XC2S50E, 200E, 300E, 400E	-
I/O, VREF Bank 1, L10P	1	D9	XC2S50E, 200E, 300E, 400E	All
I/O, L10N	1	C9	XC2S50E, 200E, 300E, 400E	-
I/O, L9P	1	B9	XC2S50E, 150E, 200E, 400E	-
I/O, L9N	1	A9	XC2S50E, 150E, 200E, 400E	XC2S400E
I/O (DLL), L8P	1	A8	-	-
GCK2, I	1	B8	-	-
GCK3, I	0	C8	-	-
I/O (DLL), L8N	0	D8	-	-
I/O	0	A7	-	XC2S400E
I/O, L7P	0	E7	XC2S50E, 200E, 300E, 400E	-
I/O, VREF Bank 0, L7N	0	D7	XC2S50E, 200E, 300E, 400E	All

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O, L#P_YY	7	L5	All	-	I/O, L75P_YY	I/O, L99P_YY	I/O, L105P_YY	I/O, L105P_YY	I/O, L105P_YY	I/O, L105P_YY
I/O (IRDY), L#N_YY	7	L6	All	-	I/O (IRDY), L75N_YY	I/O (IRDY), L99N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY
I/O (TRDY)	6	M1	-	-	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)
I/O	6	M2	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P_Y	6	M3	XC2S200E, 300E, 600E	-	-	I/O	I/O, L104P_Y	I/O, L104P_Y	I/O, L104P	I/O, L104P_Y
I/O, L#N_Y	6	M4	XC2S100E, 150E, 200E, 300E, 600E	XC2S400E, 600E	I/O, L74P_Y	I/O, L98P_Y	I/O, L104N_Y	I/O, L104N_Y	I/O, VREF Bank 6, L104N	I/O, VREF Bank 6, L104N_Y
I/O, L#P_Y	6	M5	XC2S100E, 150E, 300E, 400E	-	I/O, L74N_Y	I/O, L98N_Y	I/O, L103P	I/O, L103P_Y	I/O, L103P_Y	I/O, L103P
I/O, L#N_Y	6	M6	XC2S300E, 400E	-	-	-	I/O, L103N	I/O, L103N_Y	I/O, L103N_Y	I/O, L103N
I/O	6	N1	-	-	-	-	-	I/O	I/O	I/O
I/O	6	N2	-	-	I/O, L73P	I/O, L97P	I/O	I/O	I/O	I/O
I/O, VREF Bank 6, L#P	6	N3	XC2S200E, 400E	All	I/O, VREF Bank 6, L73N	I/O, VREF Bank 6, L97N	I/O, VREF Bank 6, L102P_Y	I/O, VREF Bank 6, L102P	I/O, VREF Bank 6, L102P_Y	I/O, VREF Bank 6, L102P
I/O, L#N	6	N4	XC2S100E, 150E, 200E, 400E	-	I/O, L72P_Y	I/O, L96P_Y	I/O, L102N_Y	I/O, L102N	I/O, L102N_Y	I/O, L102N
I/O, L#P_Y	6	N5	XC2S100E, 150E, 300E, 600E	-	I/O, L72N_Y	I/O, L96N_Y	I/O, L101P	I/O, L101P_Y	I/O, L101P	I/O, L101P_Y
I/O, L#N_Y	6	N6	XC2S300E, 600E	-	-	-	I/O, L101N	I/O, L101N_Y	I/O, L101N	I/O, L101N_Y
I/O, L#P_Y	6	P1	XC2S150E, 200E, 300E, 600E	-	-	I/O, L95P_Y	I/O, L100P_Y	I/O, L100P_Y	I/O, L100P	I/O, L100P_Y
I/O, L#N_Y	6	P2	XC2S100E, 150E, 200E, 300E, 600E	-	I/O, L71P_Y	I/O, L95N_Y	I/O, L100N_Y	I/O, L100N_Y	I/O, L100N	I/O, L100N_Y
I/O	6	R1	XC2S100E, 150E	-	I/O, L71N_Y	I/O, L94P_Y	I/O	I/O	I/O	I/O
I/O, L#P_Y	6	P3	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L94N_Y	I/O, L99P_Y	I/O, L99P_Y	I/O, L99P_Y	I/O, L99P_Y
I/O, L#N_Y	6	P4	XC2S200E, 300E, 400E, 600E	-	-	-	I/O, L99N_Y	I/O, L99N_Y	I/O, L99N_Y	I/O, L99N_Y
I/O, L#P_YY	6	P5	All	-	I/O, L70P_YY	I/O, L93P_YY	I/O, L98P_YY	I/O, L98P_YY	I/O, L98P_YY	I/O, L98P_YY
I/O, L#N_YY	6	P6	All	-	I/O, L70N_YY	I/O, L93N_YY	I/O, L98N_YY	I/O, L98N_YY	I/O, L98N_YY	I/O, L98N_YY

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O, L#P_Y	6	R2	XC2S300E, 400E, 600E	-	I/O, L69P	I/O, L92P	I/O, L97P	I/O, L97P_Y	I/O, L97P_Y	I/O, L97P_Y
I/O, VREF Bank 6, L#N_Y	6	R3	XC2S300E, 400E, 600E	All	I/O, VREF Bank 6, L69N	I/O, VREF Bank 6, L92N	I/O, VREF Bank 6, L97N	I/O, VREF Bank 6, L97N_Y	I/O, VREF Bank 6, L97N_Y	I/O, VREF Bank 6, L97N_Y
I/O	6	R4	-	-	-	-	-	I/O	I/O	I/O
I/O	6	R5	-	-	I/O	I/O	I/O	I/O	I/O	I/O
I/O, L#P	6	T2	XC2S200E, 400E, 600E	XC2S600E	I/O, L68P	I/O, L91P	I/O, L96P_Y	I/O, L96P	I/O, L96P_Y	I/O, VREF Bank 6, L96P_Y
I/O, L#N	6	T3	XC2S200E, 400E, 600E	-	I/O, L68N	I/O, L91N	I/O, L96N_Y	I/O, L96N	I/O, L96N_Y	I/O, L96N_Y
I/O, L#P_Y	6	T4	XC2S150E, 300E, 400E	-	-	I/O, L90P_Y	I/O, L95P	I/O, L95P_Y	I/O, L95P_Y	I/O, L95P
I/O, L#N_Y	6	T5	XC2S150E, 300E, 400E	-	-	I/O, L90N_Y	I/O, L95N	I/O, L95N_Y	I/O, L95N_Y	I/O, L95N
I/O, L#P_Y	6	T1	XC2S150E, 200E, 300E, 400E, 600E	-	I/O, L67P	I/O, L89P_Y	I/O, L94P_Y	I/O, L94P_Y	I/O, L94P_Y	I/O, L94P_Y
I/O, VREF Bank 6, L#N_Y	6	U1	XC2S150E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 6, L67N	I/O, VREF Bank 6, L89N_Y	I/O, VREF Bank 6, L94N_Y	I/O, VREF Bank 6, L94N_Y	I/O, VREF Bank 6, L94N_Y	I/O, VREF Bank 6, L94N_Y
I/O	6	U2	XC2S100E	-	I/O, L66P_Y	I/O	I/O	I/O	I/O	I/O
I/O, L#P_Y	6	U3	XC2S100E, 150E, 200E, 300E, 400E, 600E	-	I/O, L66N_Y	I/O, L88P_Y	I/O, L93P_Y	I/O, L93P_Y	I/O, L93P_Y	I/O, L93P_Y
I/O, L#N_Y	6	U4	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L88N_Y	I/O, L93N_Y	I/O, L93N_Y	I/O, L93N_Y	I/O, L93N_Y
I/O	6	V1	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P_Y	6	W1	XC2S100E, 200E, 300E, 600E	-	I/O, L65P_Y	I/O, L87P	I/O, L92P_Y	I/O, L92P_Y	I/O, L92P	I/O, L92P_Y
I/O, L#N_Y	6	V2	XC2S100E, 200E, 300E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L65N_Y	I/O, L87N	I/O, VREF Bank 6, L92N_Y	I/O, VREF Bank 6, L92N_Y	I/O, VREF Bank 6, L92N	I/O, VREF Bank 6, L92N_Y
I/O	6	W2	-	-	I/O	I/O	I/O	I/O	I/O	I/O
I/O, L#P_Y	6	V3	XC2S200E, 300E, 400E	-	-	I/O, L86P	I/O, L91P_Y	I/O, L91P_Y	I/O, L91P_Y	I/O, L91P
I/O, L#N_Y	6	V4	XC2S200E, 300E, 400E	-	-	I/O, L86N	I/O, L91N_Y	I/O, L91N_Y	I/O, L91N_Y	I/O, L91N
I/O	6	Y1	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P_YY	6	Y2	All	-	I/O, L64P_YY	I/O, L85P_YY	I/O, L90P_YY	I/O, L90P_YY	I/O, L90P_YY	I/O, L90P_YY
I/O, L#N_YY	6	W3	All	-	I/O, L64N_YY	I/O, L85N_YY	I/O, L90N_YY	I/O, L90N_YY	I/O, L90N_YY	I/O, L90N_YY
M1	-	U5	-	-	M1	M1	M1	M1	M1	M1

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L88P_YY	3	V25	All	-	I/O, L88P_YY	I/O, L88P_YY
I/O	3	V26	-	-	I/O	I/O
I/O, VREF Bank 3, L87N_YY	3	U19	All	All	I/O, VREF Bank 3, L87N_YY	I/O, VREF Bank 3, L87N_YY
I/O (D6), L87P_YY	3	U20	All	-	I/O (D6), L87P_YY	I/O (D6), L87P_YY
I/O (D5), L86N_YY	3	U22	All	-	I/O (D5), L86N_YY	I/O (D5), L86N_YY
I/O, L86P_YY	3	U23	All	-	I/O, L86P_YY	I/O, L86P_YY
I/O	3	U24	-	-	-	I/O
I/O, L85N	3	U25	XC2S600E	-	-	I/O, L85N_Y
I/O, L85P	3	U26	XC2S600E	-	I/O	I/O, L85P_Y
I/O	3	R18	-	-	I/O	I/O
I/O, L84N	3	T19	XC2S400E	-	I/O, L84N_Y	I/O, L84N
I/O, L84P	3	T20	XC2S400E	-	I/O, L84P_Y	I/O, L84P
I/O, L83N	3	T21	XC2S600E	-	I/O, L83N	I/O, L83N_Y
I/O, L83P	3	T22	XC2S600E	-	I/O, L83P	I/O, L83P_Y
I/O	3	T24	-	-	-	I/O
I/O, L82N	3	T25	XC2S600E	-	I/O, L82N	I/O, L82N_Y
I/O, L82P	3	T26	XC2S600E	-	I/O, L82P	I/O, L82P_Y
I/O	3	R19	-	-	-	I/O
I/O, L81N	3	R20	XC2S600E	-	I/O, L81N	I/O, L81N_Y
I/O, L81P	3	R21	XC2S600E	-	I/O, L81P	I/O, L81P_Y
I/O, VREF Bank 3, L80N_YY	3	R22	All	All	I/O, VREF Bank 3, L80N_YY	I/O, VREF Bank 3, L80N_YY
I/O (D4), L80P_YY	3	R23	All	-	I/O (D4), L80P_YY	I/O (D4), L80P_YY
I/O	3	P18	-	-	-	I/O
I/O, L79N_YY	3	R25	All	-	I/O, L79N_YY	I/O, L79N_YY
I/O, L79P_YY	3	R26	All	-	I/O, L79P_YY	I/O, L79P_YY
I/O	3	P19	-	-	-	I/O
I/O, L78N	3	P20	XC2S400E	-	I/O, L78N_Y	I/O, L78N
I/O, L78P	3	P21	XC2S400E	-	I/O, L78P_Y	I/O, L78P
I/O, VREF Bank 3, L77N	3	P22	XC2S600E	All	I/O, VREF Bank 3, L77N	I/O, VREF Bank 3, L77N_Y
I/O, L77P	3	P23	XC2S600E	-	I/O, L77P	I/O, L77P_Y
I/O	3	P24	-	-	-	I/O
I/O, L76N_YY	3	P25	All	-	I/O, L76N_YY	I/O, L76N_YY
I/O, L76P_YY	3	P26	All	-	I/O, L76P_YY	I/O, L76P_YY

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L51N	2	D24	-	-	-	I/O, L51N
I/O, L51P	2	C25	-	-	-	I/O, L51P
I/O (DIN, D0), L50N_YY	2	C26	All	-	I/O (DIN, D0), L50N_YY	I/O (DIN, D0), L50N_YY
I/O (DOUT, BUSY), L50P_YY	2	B26	All	-	I/O (DOUT, BUSY), L50P_YY	I/O (DOUT, BUSY), L50P_YY
CCLK	2	A25	-	-	CCLK	CCLK
TDO	2	C23	-	-	TDO	TDO
TDI	-	D22	-	-	TDI	TDI
I/O ($\overline{CS}$), L49P_YY	1	B24	All	-	I/O ($\overline{CS}$), L49P_YY	I/O ($\overline{CS}$), L49P_YY
I/O ($\overline{WRITE}$), L49N_YY	1	A24	All	-	I/O ($\overline{WRITE}$), L49N_YY	I/O ($\overline{WRITE}$), L49N_YY
I/O, L48P	1	B23	-	-	I/O	I/O, L48P
I/O, L48N	1	A23	-	-	-	I/O, L48N
I/O, L47P	1	B22	XC2S400E	-	I/O, L47P_Y	I/O, L47P
I/O, L47N	1	A22	XC2S400E	-	I/O, L47N_Y	I/O, L47N
I/O, L46P_YY	1	D21	All	-	I/O, L46P_YY	I/O, L46P_YY
I/O, L46N_YY	1	C21	All	-	I/O, L46N_YY	I/O, L46N_YY
I/O, VREF Bank 1, L45P_YY	1	B21	All	All	I/O, VREF Bank 1, L45P_YY	I/O, VREF Bank 1, L45P_YY
I/O, L45N_YY	1	A21	All	-	I/O, L45N_YY	I/O, L45N_YY
I/O, L44P	1	F20	XC2S600E	-	-	I/O, L44P_Y
I/O, L44N	1	E20	XC2S600E	-	I/O	I/O, L44N_Y
I/O, L43P_YY	1	D20	All	-	I/O, L43P_YY	I/O, L43P_YY
I/O, L43N_YY	1	C20	All	-	I/O, L43N_YY	I/O, L43N_YY
I/O, L42P_YY	1	B20	All	-	I/O, L42P_YY	I/O, L42P_YY
I/O, L42N_YY	1	A20	All	-	I/O, L42N_YY	I/O, L42N_YY
I/O, VREF Bank 1, L41P_YY	1	G19	All	All	I/O, VREF Bank 1, L41P_YY	I/O, VREF Bank 1, L41P_YY
I/O, L41N_YY	1	F19	All	-	I/O, L41N_YY	I/O, L41N_YY
I/O	1	E19	-	-	-	I/O
I/O, L40P_YY	1	B19	All	-	I/O, L40P_YY	I/O, L40P_YY
I/O, L40N_YY	1	A19	All	-	I/O, L40N_YY	I/O, L40N_YY
I/O	1	H18	-	-	I/O	I/O
I/O, L39P	1	G18	XC2S600E	-	I/O, L39P	I/O, L39P_Y

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L14N_YY	0	E10	All	-	I/O, L14N_YY	I/O, L14N_YY
I/O	0	G10	-	-	-	I/O
I/O, L13P	0	A9	XC2S600E	-	I/O, L13P	I/O, L13P_Y
I/O, L13N	0	B9	XC2S600E	-	I/O, L13N	I/O, L13N_Y
I/O	0	H10	-	-	-	I/O
I/O, L12P_YY	0	C9	All	-	I/O, L12P_YY	I/O, L12P_YY
I/O, L12N_YY	0	D9	All	-	I/O, L12N_YY	I/O, L12N_YY
I/O	0	E9	-	-	I/O	I/O
I/O, VREF Bank 0, L11P	0	F9	-	All	I/O, VREF Bank 0, L11P	I/O, VREF Bank 0, L11P
I/O, L11N	0	G9	-	-	I/O, L11N	I/O, L11N
I/O, L10P	0	A8	-	-	I/O, L10P	I/O, L10P
I/O, L10N	0	B8	-	-	I/O, L10N	I/O, L10N
I/O	0	H9	-	-	I/O	I/O
I/O, L9P	0	E8	XC2S600E	-	I/O	I/O, L9P_Y
I/O, L9N	0	F8	XC2S600E	XC2S600E	-	I/O, VREF Bank 0, L9N_Y
I/O, L8P	0	A7	XC2S600E	-	I/O, L8P	I/O, L8P_Y
I/O, L8N	0	B7	XC2S600E	-	I/O, L8N	I/O, L8N_Y
I/O	0	G8	-	-	I/O	I/O
I/O, L7P_YY	0	C7	All	-	I/O, L7P_YY	I/O, L7P_YY
I/O, L7N_YY	0	D7	All	-	I/O, L7N_YY	I/O, L7N_YY
I/O	0	E7	-	-	-	I/O
I/O, L6P_YY	0	F7	All	-	I/O, L6P_YY	I/O, L6P_YY
I/O, VREF Bank 0, L6N_YY	0	G7	All	All	I/O, VREF Bank 0, L6N_YY	I/O, VREF Bank 0, L6N_YY
I/O	0	A6	-	-	I/O	I/O
I/O, L5P	0	B6	-	-	I/O, L5P	I/O, L5P
I/O, L5N	0	C6	-	-	I/O, L5N	I/O, L5N
I/O, L4P	0	D6	-	-	I/O, L4P	I/O, L4P
I/O, L4N	0	E6	-	-	I/O, L4N	I/O, L4N
I/O	0	F6	-	-	-	I/O
I/O, L3P_YY	0	A5	All	-	I/O, L3P_YY	I/O, L3P_YY
I/O, VREF Bank 0, L3N_YY	0	B5	All	All	I/O, VREF Bank 0, L3N_YY	I/O, VREF Bank 0, L3N_YY
I/O, L2P_YY	0	D5	All	-	I/O, L2P_YY	I/O, L2P_YY