AMD Xilinx - XC2S100E-6FTG256C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	600
Number of Logic Elements/Cells	2700
Total RAM Bits	40960
Number of I/O	182
Number of Gates	100000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s100e-6ftg256c

General Overview

The Spartan-IIE family of FPGAs have a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), surrounded by a perimeter of programmable Input/Output Blocks (IOBs). There are four Delay-Locked Loops (DLLs), one at each corner of the die. Two columns of block RAM lie on opposite sides of the die, between the CLBs and the IOB columns. The XC2S400E has four columns and the XC2S600E has six columns of block RAM. These functional elements are interconnected by a powerful hierarchy of versatile routing channels (see Figure 1).

Spartan-IIE FPGAs are customized by loading configuration data into internal static memory cells. Unlimited reprogramming cycles are possible with this approach. Stored values in these cells determine logic functions and interconnections implemented in the FPGA. Configuration data can be read from an external serial PROM (master serial mode), or written into the FPGA in slave serial, slave parallel, or Boundary Scan modes. Xilinx offers multiple types of low-cost configuration solutions including the Platform Flash in-system programmable configuration PROMs.

Spartan-IIE FPGAs are typically used in high-volume applications where the versatility of a fast programmable solution adds benefits. Spartan-IIE FPGAs are ideal for shortening product development cycles while offering a cost-effective solution for high volume production.

Spartan-IIE FPGAs achieve high-performance, low-cost operation through advanced architecture and semiconductor technology. Spartan-IIE devices provide system clock rates beyond 200 MHz. In addition to the conventional benefits of high-volume programmable logic solutions, Spartan-IIE FPGAs also offer on-chip synchronous single-port and dual-port RAM (block and distributed form), DLL clock drivers, programmable set and reset on all flip-flops, fast carry logic, and many other features.

Spartan-IIE Family Compared to Spartan-II Family

- Higher density and more I/O
- Higher performance
- Unique pinouts in cost-effective packages
- Differential signaling
  - LVDS, Bus LVDS, LVPECL
- V_{CCINT} = 1.8V
  - Lower power
  - 5V tolerance with external resistor
  - 3V tolerance directly
- PCI, LVTTL, and LVCMOS2 input buffers powered by V_{CCO} instead of V_{CCINT}
- Unique larger bitstream

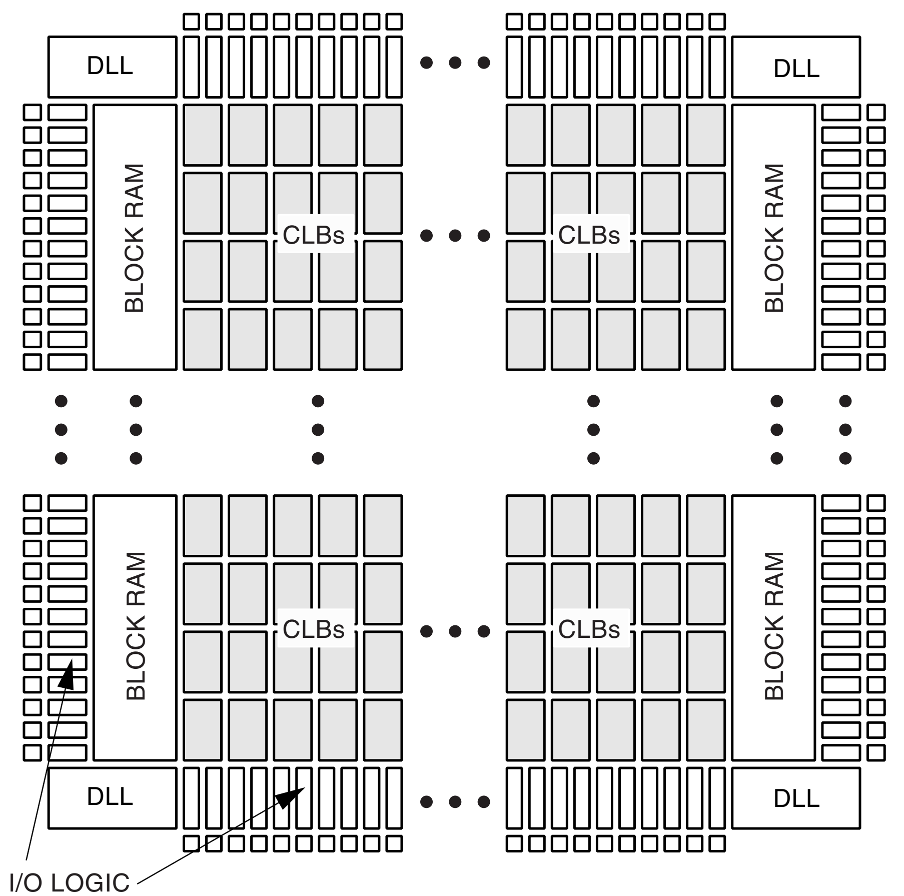

Figure 1: **Basic Spartan-IIE Family FPGA Block Diagram**

Spartan-IIE Product Availability

Table 2 shows the maximum user I/Os available on the device and the number of user I/Os available for each device/package combination.

Table 2: **Spartan-IIE FPGA User I/O Chart**

Device	Maximum User I/O	Available User I/O According to Package Type				
		TQ144 TQG144	PQ208 PQG208	FT256 FTG256	FG456 FGG456	FG676 FGG676
XC2S50E	182	102	146	182	-	-
XC2S100E	202	102	146	182	202	-
XC2S150E	265	-	146	182	265	-
XC2S200E	289	-	146	182	289	-
XC2S300E	329	-	146	182	329	-
XC2S400E	410	-	-	182	329	410
XC2S600E	514	-	-	-	329	514

Notes:
1. User I/O counts include the four global clock/user input pins.

is required for most output standards and for LVTTL, LVCMOS, and PCI inputs.

Table 4: **Compatible Standards**

V_{CCO}	Compatible Standards
3.3V	PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, LVPECL, GTL, GTL+
2.5V	SSTL2 I, SSTL2 II, LVCMOS2, LVDS, Bus LVDS, GTL, GTL+
1.8V	LVCMOS18, GTL, GTL+
1.5V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage, V_{REF}. In this case, certain user-I/O pins are automatically configured as inputs for the V_{REF} voltage. About one in six of the I/O pins in the bank assume this role.

V_{REF} pins within a bank are interconnected internally and consequently only one V_{REF} voltage can be used within each bank. All V_{REF} pins in the bank, however, must be connected to the external voltage source for correct operation.

In a bank, inputs requiring V_{REF} can be mixed with those that do not but only one V_{REF} voltage may be used within a bank. The V_{CCO} and V_{REF} pins for each bank appear in the device pinout tables.

Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device. All V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage, and not used for I/O.

Table 5: **I/O Banking**

Package	TQ144, PQ208	FT256, FG456, FG676
V_{CCO} Banks	Interconnected as 1	8 independent
V_{REF} Banks	8 independent	8 independent

See Xilinx® Application Note XAPP179 for more information on I/O resources.

Hot Swap, Hot Insertion, Hot Socketing Support

The I/O pins support hot swap — also called hot insertion and hot socketing — and are considered CompactPCI Friendly according to the PCI Bus v2.2 Specification. Consequently, an unpowered Spartan-IIE FPGA can be plugged directly into a powered system or backplane without affecting or damaging the system or the FPGA. The hot swap functionality is built into every XC2S150E, XC2S400E, and XC2S600E device. All other Spartan-IIE devices built after Product Change Notice PCN2002-05 also include hot swap functionality.

To support hot swap, Spartan-IIE devices include the following I/O features.

- Signals can be applied to Spartan-IIE FPGA I/O pins before powering the FPGA's V_{CCINT} or V_{CCO} supply inputs.
- Spartan-IIE FPGA I/O pins are high-impedance (i.e., three-stated) before and throughout the power-up and configuration processes when employing a configuration mode that does not enable the preconfiguration weak pull-up resistors (see Table 11, page 22).
- There is no current path from the I/O pin back to the V_{CCINT} or V_{CCO} voltage supplies.
- Spartan-IIE FPGAs are immune to latch-up during hot swap.

Once connected to the system, each pin adds a small amount of capacitance (C_{IN}). Likewise, each I/O consumes a small amount of DC current, equivalent to the input leakage specification (I_L). There also may be a small amount of temporary AC current (I_{HSPO}) when the pin input voltage exceeds V_{CCO} plus 0.4V, which lasts less than 10 ns.

A weak-keeper circuit within each user-I/O pin is enabled during the last frame of configuration data and has no noticeable effect on robust system signals driven by an active driver or a strong pull-up or pull-down resistor. Undriven or floating system signals may be affected. The specific effect depends on how the I/O pin is configured. User-I/O pins configured as outputs or enabled outputs have a weak pull-up resistor to V_{CCO} during the last configuration frame. User-I/O pins configured as inputs or bidirectional I/Os have weak pull-down resistors. The weak-keeper circuit turns off when the DONE pin goes High, provided that it is not used in the configured application.

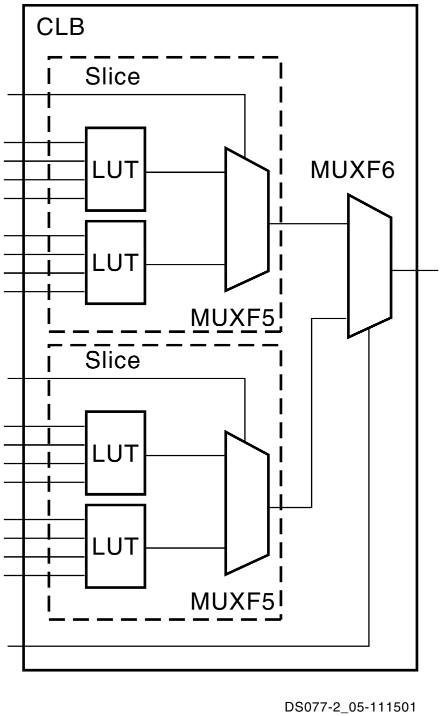

Figure 7: **F5 and F6 Multiplexers**

Each CLB has four direct feedthrough paths, one per LC. These paths provide extra data input lines or additional local routing that does not consume logic resources.

Arithmetic Logic

Dedicated carry logic provides capability for high-speed arithmetic functions. The Spartan-IIE FPGA CLB supports two separate carry chains, one per slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 1-bit full adder to be implemented within an LC. In addition, a dedicated AND gate improves the efficiency of multiplier implementations.

The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

BUFTs

Each Spartan-IIE FPGA CLB contains two 3-state drivers (BUFTs) that can drive on-chip busses. The IOBs on the left and right sides can also drive the on-chip busses. See Dedicated Routing, page 17. Each Spartan-IIE FPGA BUFT has an independent 3-state control pin and an independent input pin. The 3-state control pin is an active-Low enable (T). When all BUFTs on a net are disabled, the net is High. There is no need to instantiate a pull-up unless desired for simulation purposes. Simultaneously driving BUFTs onto the same net will not cause contention. If driven both High and Low, the net will be Low.

Block RAM

Spartan-IIE FPGAs incorporate several large block RAM memories. These complement the distributed RAM Look-Up Tables (LUTs) that provide shallow memory structures implemented in CLBs.

Block RAM memory blocks are organized in columns. Most Spartan-IIE devices contain two such columns, one along each vertical edge. The XC2S400E has four block RAM columns and the XC2S600E has six block RAM columns. These columns extend the full height of the chip. Each memory block is four CLBs high, and consequently, a Spartan-IIE device 16 CLBs high will contain four memory blocks per column, and a total of eight blocks.

Table 6: **Spartan-IIE Block RAM Amounts**

Spartan-IIE Device	# of Blocks	Total Block RAM Bits
XC2S50E	8	32K
XC2S100E	10	40K
XC2S150E	12	48K
XC2S200E	14	56K
XC2S300E	16	64K
XC2S400E	40	160K
XC2S600E	72	288K

Each block RAM cell, as illustrated in Figure 8, is a fully synchronous dual-ported 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

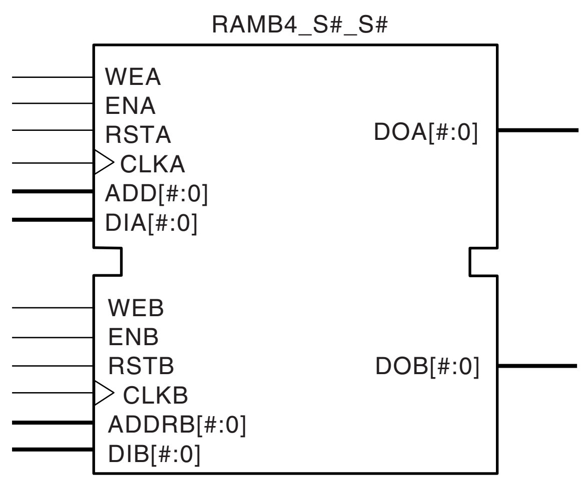

Figure 8: **Dual-Port Block RAM**

Table 7 shows the depth and width aspect ratios for the block RAM.

Table 7: **Block RAM Port Aspect Ratios**

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

The Spartan-IIE FPGA block RAM also includes dedicated routing to provide an efficient interface with both CLBs and other block RAMs. See Xilinx Application Note XAPP173 for more information on block RAM.

Programmable Routing

It is the longest delay path that limits the speed of any design. Consequently, the Spartan-IIE FPGA routing architecture and its place-and-route software were defined jointly to minimize long-path delays and yield the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

The software automatically uses the best available routing based on user timing requirements. The details are provided here for reference.

Local Routing

The local routing resources, as shown in Figure 9, provide the following three types of connections:

- Interconnections among the LUTs, flip-flops, and General Routing Matrix (GRM), described below.
- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM

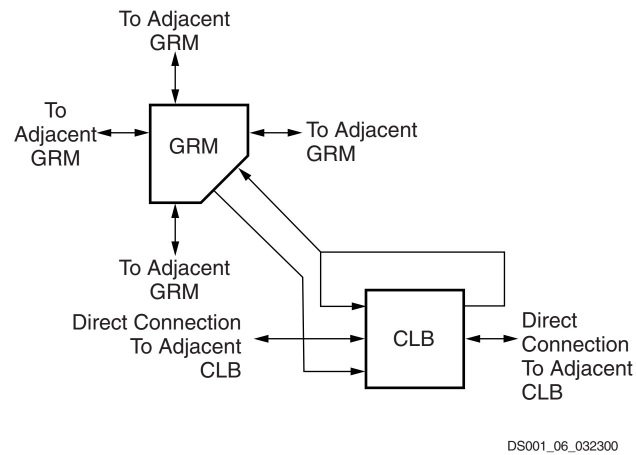

Figure 9: **Spartan-IIE Local Routing**

General Purpose Routing

Most Spartan-IIE FPGA signals are routed on the general purpose routing, and consequently, the majority of interconnect resources are associated with this level of the routing hierarchy. The general routing resources are located in horizontal and vertical routing channels associated with the rows and columns of CLBs. The general-purpose routing resources are listed below.

- Adjacent to each CLB is a General Routing Matrix (GRM). The GRM is the switch matrix through which horizontal and vertical routing resources connect, and is also the means by which the CLB gains access to the general purpose routing.
- 24 single-length lines route GRM signals to adjacent GRMs in each of the four directions.
- 96 buffered Hex lines route GRM signals to other GRMs six blocks away in each one of the four directions. Organized in a staggered pattern, Hex lines may be driven only at their endpoints. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source). One third of the Hex lines are bidirectional, while the remaining ones are unidirectional.
- 12 Longlines are buffered, bidirectional wires that distribute signals across the device quickly and efficiently. Vertical Longlines span the full height of the device, and horizontal ones span the full width of the device.

I/O Routing

Spartan-IIE devices have additional routing resources around their periphery that form an interface between the CLB array and the IOBs. This additional routing, called the VersaRing™ routing, facilitates pin-swapping and pin-locking, such that logic redesigns can adapt to existing PCB layouts. Time-to-market is reduced, since PCBs and other system components can be manufactured while the logic design is still in progress.

Table 8: **Boundary-Scan Instructions *(Continued)***

Boundary-Scan Command	Binary Code[4:0]	Description
INTEST	00111	Enables boundary-scan INTEST operation
USERCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIGHZ	01010	Disables output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions

The public boundary-scan instructions are available prior to configuration, except for USER1 and USER2. After configuration, the public instructions remain available together with any USERCODE instructions installed during the configuration. While the SAMPLE/PRELOAD and BYPASS instructions are available during configuration, it is recommended that boundary-scan operations not be performed during this transitional period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

To facilitate internal scan chains, the User Register provides three outputs (Reset, Update, and Shift) that represent the corresponding states in the boundary-scan internal state machine.

Figure 14 is a diagram of the Spartan-IIE family boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

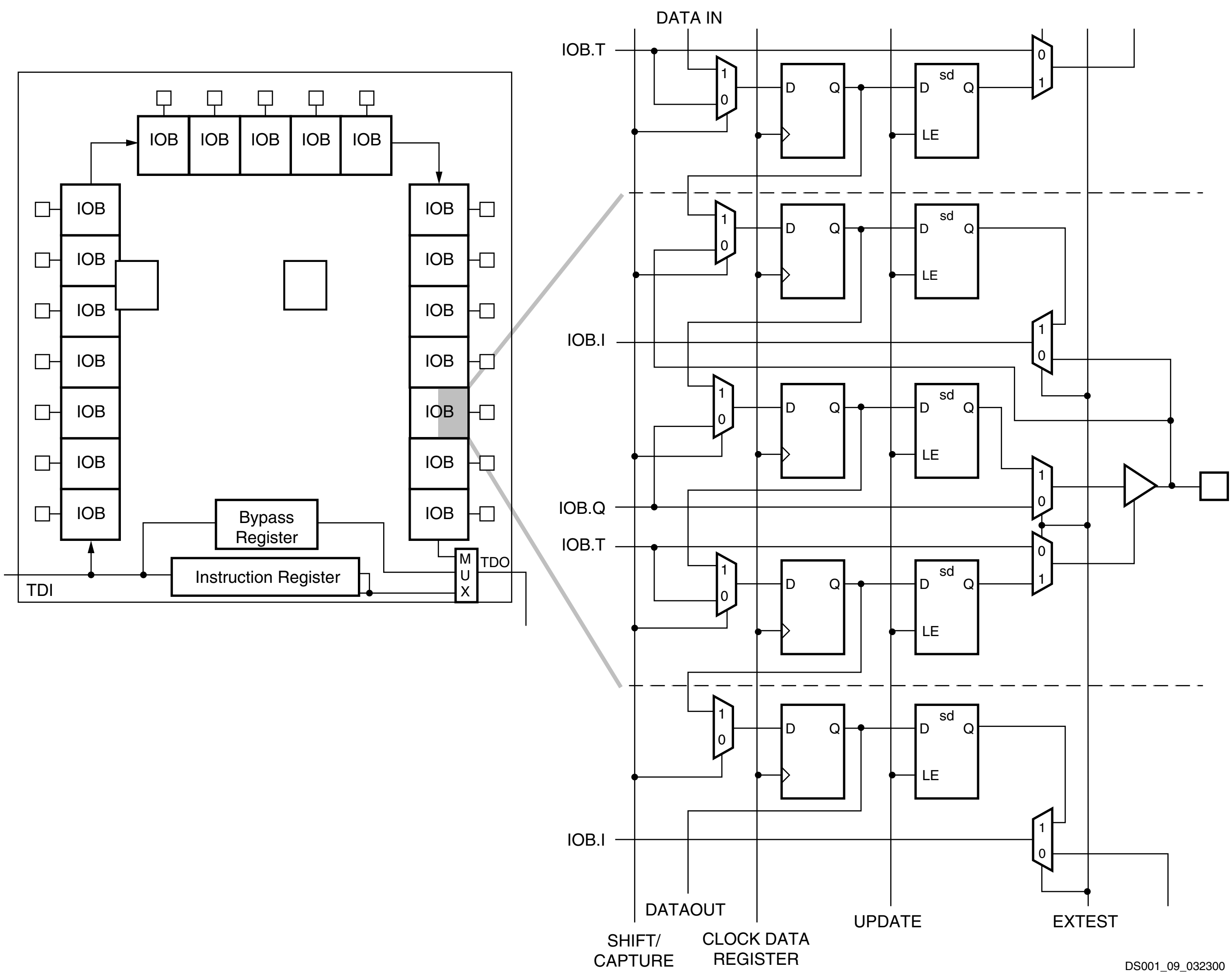

Figure 14: **Spartan-IIE Family Boundary Scan Logic**

design, thus allowing the most convenient entry method to be used for each portion of the design.

Design Implementation

The place-and-route tools automatically provide the implementation flow described in this section. The partitioner takes the EDIF netlist for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floorplanning.

The implementation software incorporates timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines then recognize these user-specified requirements and accommodate them.

Timing requirements are entered in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the netlist for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the static timing analyzer.

For in-circuit debugging, Xilinx offers a download cable, which connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can read back the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

Configuration

Configuration is the process by which the bitstream of a design, as generated by the Xilinx development software, is loaded into the internal configuration memory of the FPGA. Spartan-IIE devices support both serial configuration, using the master/slave serial and JTAG modes, as well as byte-wide configuration employing the Slave Parallel mode.

Configuration File

Spartan-IIE devices are configured by sequentially loading frames of data that have been concatenated into a configuration file. Table 10 shows how much nonvolatile storage space is needed for Spartan-IIE devices.

It is important to note that, while a PROM is commonly used to store configuration data before loading them into the FPGA, it is by no means required. Any of a number of different kinds of under populated nonvolatile storage already available either on or off the board (for example, hard drives, FLASH cards, and so on) can be used.

Table 10: **Spartan-IIE Configuration File Size**

Device	Configuration File Size (Bits)
XC2S50E	630,048
XC2S100E	863,840
XC2S150E	1,134,496
XC2S200E	1,442,016
XC2S300E	1,875,648
XC2S400E	2,693,440
XC2S600E	3,961,632

Modes

Spartan-IIE devices support the following four configuration modes:

- Slave Serial mode
- Master Serial mode
- Slave Parallel mode
- Boundary-scan mode

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to the end of configuration. The selection codes are listed in Table 11.

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected.

During start-up, the device performs four operations:

1. The assertion of DONE. The failure of DONE to go High may indicate the unsuccessful loading of configuration data.
2. The release of the Global Three State (GTS). This activates all the I/Os to which signals are assigned. The remaining I/Os stay in a high-impedance state with internal weak pull-up resistors present.
3. The release of the Global Set Reset (GSR). This allows all flip-flops to change state.
4. The assertion of Global Write Enable (GWE). This allows all RAMs and flip-flops to change state.

By default, these operations are synchronized to CCLK. The entire start-up sequence lasts eight cycles, called C0-C7, after which the loaded design is fully functional. The four operations can be selected to switch on any CCLK cycle C1-C6 through settings in the Xilinx Development Software. The default timing for start-up is shown in the top half of Figure 17; heavy lines show default settings.

The default Start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The bottom half of Figure 17 shows another commonly used version of the start-up timing known as Sync-to-DONE. This version makes the GTS, GSR, and GWE events conditional upon the DONE pin going High. This timing is important for a daisy chain of multiple FPGAs in serial mode, since it ensures that all FPGAs go through start-up together, after all their DONE pins have gone High.

Sync-to-DONE timing is selected by setting the GTS, GSR, and GWE cycles to a value of DONE in the configuration options. This causes these signals to transition one clock cycle after DONE externally transitions High.

The sequence can also be paused at any stage until lock has been achieved on any or all DLLs.

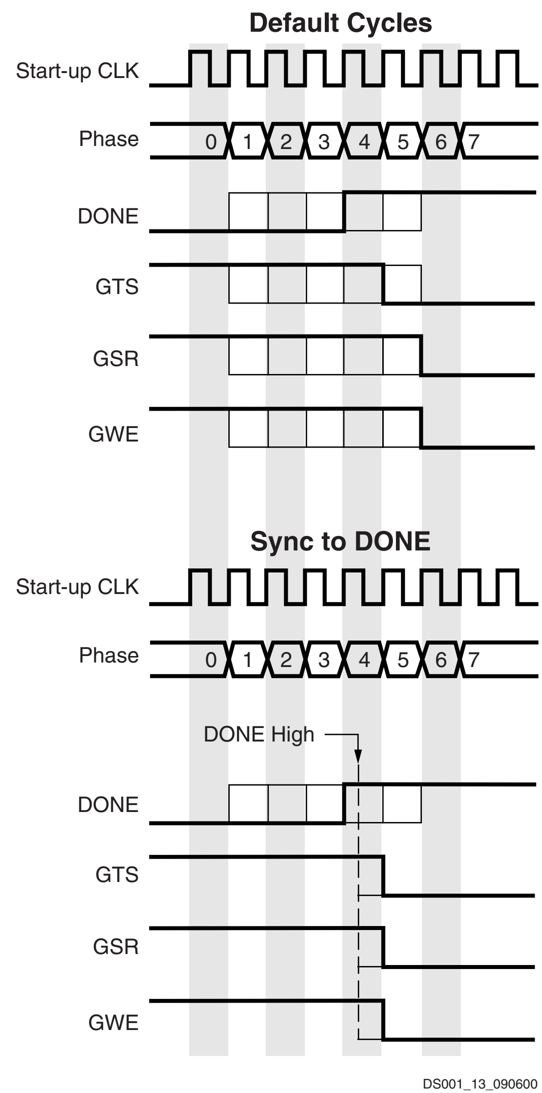

Figure 17: **Start-Up Waveforms**

Serial Modes

There are two serial configuration modes. In Master Serial mode, the FPGA controls the configuration process by driving CCLK as an output. In Slave Serial mode, the FPGA passively receives CCLK as an input from an external agent (e.g., a microprocessor, CPLD, or second FPGA in master mode) that is controlling the configuration process. In both modes, the FPGA is configured by loading one bit per CCLK cycle. The MSB of each configuration data byte is always written to the DIN pin first.

See Figure 18 for the sequence for loading data into the Spartan-IIE FPGA serially. This is an expansion of the "Load Configuration Data Frames" block in Figure 16, page 23. Note that $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$ are not normally used during serial configuration. To ensure successful loading of the FPGA, do not toggle $\overline{\text{WRITE}}$ with $\overline{\text{CS}}$ Low during serial configuration.

Revision History

Date	Version	Description
11/15/2001	1.0	Initial Xilinx release.
11/18/2002	2.0	Added XC2S400E and XC2S600E. Removed Preliminary designation. Clarified details of I/O standards, boundary scan, and configuration.
07/09/2003	2.1	Added hot swap description (see Hot Swap, Hot Insertion, Hot Socketing Support). Added Table 9 containing JTAG IDCODE values. Clarified configuration PROM support.
06/18/2008	2.3	Added note that TDI, TMS, and TCK have a default pull-up resistor. Add note on maximum daisy-chain limit. Updated Figure 19 since Mode pins can be pulled up to either 2.5V or 3.3V. Updated all modules for continuous page, figure, and table numbering. Updated links. Synchronized all modules to v2.3.
08/09/2013	3.0	This product is obsolete/discontinued per XCN12026.

Global Clock Setup and Hold for LVTTL Standard, *with* DLL (Pin-to-Pin)

Symbol	Description	Speed Grade		Units
		-7	-6	
		Min	Min	
T_{PSDLL} / T_{PHDLL}	Input setup and hold time relative to global clock input signal for LVTTL standard, no delay, IFF,(1) *with* DLL	1.6 / 0	1.7 / 0	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DLL output jitter is already included in the timing calculation.
4. For data input with different standards, adjust the setup time delay by the values shown in IOB Input Delay Adjustments for Different Standards, page 38. For a global clock input with standards other than LVTTL, adjust delays with values from the I/O Standard Global Clock Input Adjustments, page 42.
5. A zero hold time listing indicates no hold time or a negative hold time.

Global Clock Setup and Hold for LVTTL Standard, *without* DLL (Pin-to-Pin)

Symbol	Description	Device	Speed Grade		Units
			-7	-6	
			Min	Min	
T_{PSFD} / T_{PHFD}	Input setup and hold time relative to global clock input signal for LVTTL standard, with delay, IFF,(1) *without* DLL	XC2S50E	1.8 / 0	1.8 / 0	ns
		XC2S100E	1.8 / 0	1.8 / 0	ns
		XC2S150E	1.9 / 0	1.9 / 0	ns
		XC2S200E	1.9 / 0	1.9 / 0	ns
		XC2S300E	2.0 / 0	2.0 / 0	ns
		XC2S400E	2.0 / 0	2.0 / 0	ns
		XC2S600E	2.1 / 0	2.1 / 0	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. For data input with different standards, adjust the setup time delay by the values shown in IOB Input Delay Adjustments for Different Standards, page 38. For a global clock input with standards other than LVTTL, adjust delays with values from the I/O Standard Global Clock Input Adjustments, page 42.

Spartan-IIE Package Pinouts

The Spartan®-IIE family of FPGAs is available in five popular, low-cost packages, including plastic quad flat packs and fine-pitch ball grid arrays. Family members have footprint compatibility across devices provided in the same package, with minor exceptions due to the smaller number of I/O in smaller devices or due to LVDS/LVPECL pin pairing. The Spartan-IIE family is not footprint compatible with any other FPGA family. The following package-specific pinout tables indicate function, pin, and bank information for all devices available in that package. The pinouts follow the pad locations around the die, starting from pin 1 on the QFP packages.

Table 12: **Spartan-IIE Family Package Options**

Package	Leads	Type	Maximum I/O	Lead Pitch (mm)	Footprint Area (mm)	Height (mm)	Mass[1] (g)
TQ144 / TQG144	144	Thin Quad Flat Pack (TQFP)	102	0.5	22 x 22	1.60	1.4
PQ208 / PQG208	208	Plastic Quad Flat Pack (PQFP)	146	0.5	30.6 x 30.6	3.70	5.3
FT256 / FTG256	256	Fine-pitch Thin Ball Grid Array (FBGA)	182	1.0	17 x 17	1.55	1.0
FG456 / FGG456	456	Fine-pitch Ball Grid Array (FBGA)	329	1.0	23 x 23	2.60	2.2
FG676 / FGG676	676	Fine-pitch Ball Grid Array (FBGA)	514	1.0	27 x 27	2.60	3.1

Notes:

1. Package mass is ±10%.

Package Overview

Table 12 shows the five low-cost, space-saving production package styles for the Spartan-IIE family.

Each package style is available in an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra ‘G’ in the package style name. For example, the standard “TQ144” package becomes “TQG144” when ordered as the Pb-free option. Leaded (non-Pb-free) packages may be available for selected devices, with the same pin-out and without the "G" in the ordering code; contact Xilinx® sales for more information. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 13.

For additional package information, see UG112: *Device Package User Guide*.

Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx web site at the specified location in Table 13.

Material Declaration Data Sheets (MDDS) are also available on the Xilinx web site for each package.

Table 13: **Xilinx Package Documentation**

Package	Drawing	MDDS
TQ144	Package Drawing	PK169_TQ144
TQG144		PK126_TQG144
PQ208	Package Drawing	PK166_PQ208
PQG208		PK123_PQG208
FT256	Package Drawing	PK158_FT256
FTG256		PK115_FTG256
FG456	Package Drawing	PK154_FG456
FGG456		PK109_FGG456
FG676	Package Drawing	PK155_FG676
FGG676		PK111_FGG676

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name			LVDS	
Function	**Bank**	**Pin**	**Async. Output Option**	**V_{REF} Option**
I/O, L28P	4	P89	XC2S50E, 100E, 200E, 300E	-
VCCINT	-	P90	-	-
VCCO	-	P91	-	-
GND	-	P92	-	-
I/O, L27N	4	P93	XC2S50E, 100E, 200E, 300E	-
I/O, L27P	4	P94	XC2S50E, 100E, 200E, 300E	XC2S100E, 150E, 200E, 300E
I/O	4	P95	-	-
I/O	4	P96	-	-
I/O, L26N_YY	4	P97	All	-
I/O, VREF Bank 4, L26P_YY	4	P98	All	All
I/O	4	P99	-	-
I/O	4	P100	-	XC2S200E, 300E
I/O, L25N_YY	4	P101	All	-
I/O, L25P_YY	4	P102	All	-
GND	-	P103	-	-
DONE	3	P104	-	-
VCCO	-	P105	-	-
$\overline{\text{PROGRAM}}$	-	P106	-	-
I/O ($\overline{\text{INIT}}$), L24N_YY	3	P107	All	-
I/O (D7), L24P_YY	3	P108	All	-
I/O	3	P109	-	XC2S200E, 300E
I/O	3	P110	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name			LVDS	
Function	**Bank**	**Pin**	**Async. Output Option**	**V_{REF} Option**
I/O, VREF Bank 3, L23N	3	P111	XC2S50E, 150E, 200E, 300E	All
I/O, L23P	3	P112	XC2S50E, 150E, 200E, 300E	-
I/O	3	P113	-	-
I/O	3	P114	-	-
I/O, L22N	3	P115	XC2S50E, 300E	XC2S100E, 150E, 200E, 300E
I/O (D6), L22P	3	P116	XC2S50E, 300E	-
GND	-	P117	-	-
VCCO	-	P118	-	-
VCCINT	-	P119	-	-
I/O (D5), L21N_YY	3	P120	All	-
I/O, L21P_YY	3	P121	All	-
I/O, L20N_YY	3	P122	All	-
I/O, L20P_YY	3	P123	All	-
GND	-	P124	-	-
I/O, VREF Bank 3, L19N	3	P125	XC2S50E, 300E	All
I/O (D4), L19P	3	P126	XC2S50E, 300E	-
I/O	3	P127	-	-
VCCINT	-	P128	-	-
I/O (TRDY)	3	P129	-	-
VCCO	-	P130	-	-
GND	-	P131	-	-
I/O (IRDY), L18N_YY	2	P132	All	-
I/O, L18P_YY	2	P133	All	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name: Function	Pad Name: Bank	Pin	LVDS Async. Output Option	V_{REF} Option
I/O (D5), L35N_YY	3	L13	All	-
I/O, L35P_YY	3	K14	All	-
I/O, L34N	3	K15	XC2S100E, 150E, 400E	-
I/O, L34P	3	K16	XC2S100E, 150E, 400E	-
I/O, L33N	3	L12	XC2S50E, 100E, 150E, 200E, 300E(1)	-
I/O, L33P	3	K12	XC2S50E, 100E, 150E, 200E, 300E(1)	-
I/O, VREF Bank 3, L32N	3	K13	XC2S50E, 300E, 400E	All
I/O (D4), L32P	3	J14	XC2S50E, 300E, 400E	-
I/O, L31N	3	J15	XC2S100E, 150E, 200E, 400E	-
I/O, L31P	3	J16	XC2S100E, 150E, 200E, 400E	XC2S400E
I/O (TRDY)	3	J13	-	-
I/O (IRDY), L30N_YY	2	H16	All	-
I/O, L30P_YY	2	G16	All	-
I/O, L29N	2	H14	XC2S100E, 150E, 200E, 400E	XC2S400E
I/O, L29P	2	H15	XC2S100E, 150E, 200E, 400E	-
I/O (D3), L28N	2	G15	XC2S50E, 300E, 400E	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name: Function	Pad Name: Bank	Pin	LVDS Async. Output Option	V_{REF} Option
I/O, VREF Bank 2, L28P	2	F16	XC2S50E, 300E, 400E	All
I/O, L27N	2	H13	XC2S50E, 100E, 150E, 200E, 300E(1)	-
I/O, L27P	2	G14	XC2S50E, 100E, 150E, 200E, 300E(2)	-
I/O, L26N	2	F15	XC2S100E, 150E, 400E	-
I/O, L26P	2	E16	XC2S100E, 150E, 400E	-
I/O, L25N_YY	2	G13	All	-
I/O (D2), L25P_YY	2	F14	All	-
I/O (D1), L24N	2	E15	XC2S50E, 300E, 400E	-
I/O, L24P	2	D16	XC2S50E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L23N	2	F13	XC2S150E, 200E, 400E	-
I/O, L23P	2	E14	XC2S150E, 200E, 400E	-
I/O, L22N	2	D15	XC2S50E, 150E, 200E, 300E, 400E	-
I/O, VREF Bank 2, L22P	2	C16	XC2S50E, 150E, 200E, 300E, 400E	All
I/O, L21N	2	G12	XC2S50E, 100E, 200E, 300E	-
I/O, L21P	2	F12	XC2S50E, 100E, 200E, 300E	-
I/O, L20N	2	E13	XC2S100E, 200E, 300E	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name				
Function	Bank	Pin	LVDS Async. Output Option	V_{REF} Option
I/O, L20P	2	D14	XC2S100E, 200E, 300E	XC2S200E, 300E, 400E
I/O (DIN, D0), L19N_YY	2	B16	All	-
I/O (DOUT, BUSY), L19P_YY	2	C15	All	-
CCLK	2	A15	-	-
TDO	2	B14	-	-
TDI	-	C13	-	-
I/O ($\overline{CS}$), L18P_YY	1	A14	All	-
I/O ($\overline{WRITE}$), L18N_YY	1	A13	All	-
I/O, L17P	1	B13	XC2S50E, 100E, 200E, 300E, 400E	XC2S200E, 300E, 400E
I/O, L17N	1	C12	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L16P_YY	1	B12	All	-
I/O, L16N_YY	1	A12	All	-
I/O, VREF Bank 1, L15P_YY	1	D12	All	All
I/O, L15N_YY	1	E11	All	-
I/O, L14P	1	D11	XC2S50E, 100E, 150E, 300E	-
I/O, L14N	1	C11	XC2S50E, 100E, 150E, 300E	-
I/O, L13P	1	B11	XC2S50E, 100E, 200E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L13N	1	A11	XC2S50E, 100E, 200E, 300E, 400E	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name				
Function	Bank	Pin	LVDS Async. Output Option	V_{REF} Option
I/O, L12P	1	E10	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L12N	1	D10	XC2S50E, 100E, 200E, 300E, 400E	-
I/O	1	C10	-	-
I/O, L11P	1	B10	XC2S50E, 200E, 300E, 400E	-
I/O, L11N	1	A10	XC2S50E, 200E, 300E, 400E	-
I/O, VREF Bank 1, L10P	1	D9	XC2S50E, 200E, 300E, 400E	All
I/O, L10N	1	C9	XC2S50E, 200E, 300E, 400E	-
I/O, L9P	1	B9	XC2S50E, 150E, 200E, 400E	-
I/O, L9N	1	A9	XC2S50E, 150E, 200E, 400E	XC2S400E
I/O (DLL), L8P	1	A8	-	-
GCK2, I	1	B8	-	-
GCK3, I	0	C8	-	-
I/O (DLL), L8N	0	D8	-	-
I/O	0	A7	-	XC2S400E
I/O, L7P	0	E7	XC2S50E, 200E, 300E, 400E	-
I/O, VREF Bank 0, L7N	0	D7	XC2S50E, 200E, 300E, 400E	All

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
TMS	-	E4	-	-	TMS	TMS	TMS	TMS	TMS	TMS
I/O	7	D3	XC2S150E	-	I/O	I/O, L113P_Y	I/O	I/O	I/O	I/O
I/O	7	C2	-	-	-	-	-	I/O	I/O	I/O
I/O	7	C1	XC2S150E	-	-	I/O, L113N_Y	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	D2	XC2S150E, 200E, 300E, 400E	-	-	I/O, L112P_Y	I/O, L119P_Y	I/O, L119P_Y	I/O, L119P_Y	I/O, L119P
I/O, L#N_Y	7	D1	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L112N_Y	I/O, L119N_Y	I/O, L119N_Y	I/O, L119N_Y	I/O, L119N
I/O, L#P_Y	7	E2	XC2S100E, 200E, 300E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L85P_Y	I/O, L111P	I/O, VREF Bank 7, L118P_Y	I/O, VREF Bank 7, L118P_Y	I/O, VREF Bank 7, L118P	I/O, VREF Bank 7, L118P_Y
I/O, L#N_Y	7	E3	XC2S100E, 200E, 300E, 600E	-	I/O, L85N_Y	I/O, L111N	I/O, L118N_Y	I/O, L118N_Y	I/O, L118N	I/O, L118N_Y
I/O	7	E1	-	-	-	-	-	I/O	I/O	I/O
I/O	7	F5	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	F4	XC2S100E, 200E, 300E, 600E	-	I/O, L84P_Y	I/O, L110P	I/O, L117P_Y	I/O, L117P_Y	I/O, L117P	I/O, L117P_Y
I/O, L#N_Y	7	F3	XC2S100E, 200E, 300E, 600E	-	I/O, L84N_Y	I/O, L110N	I/O, L117N_Y	I/O, L117N_Y	I/O, L117N	I/O, L117N_Y
I/O, VREF Bank 7, L#P_Y	7	F2	XC2S150E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 7, L83P	I/O, VREF Bank 7, L109P_Y	I/O, VREF Bank 7, L116P_Y	I/O, VREF Bank 7, L116P_Y	I/O, VREF Bank 7, L116P_Y	I/O, VREF Bank 7, L116P_Y
I/O, L#N_Y	7	F1	XC2S150E, 200E, 300E, 400E, 600E	-	I/O, L83N	I/O, L109N_Y	I/O, L116N_Y	I/O, L116N_Y	I/O, L116N_Y	I/O, L116N_Y
I/O	7	G5	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	G4	XC2S150E, 200E, 300E, 400E	-	-	I/O, L108P_Y	I/O, L115P_Y	I/O, L115P_Y	I/O, L115P_Y	I/O, L115P
I/O, L#N_Y	7	G3	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L108N_Y	I/O, L115N_Y	I/O, L115N_Y	I/O, L115N_Y	I/O, L115N
I/O, L#P_Y	7	G2	XC2S100E, 150E, 300E, 600E	XC2S600E	I/O, L82P_Y	I/O, L107P_Y	I/O, L114P	I/O, L114P_Y	I/O, L114P	I/O, VREF Bank 7, L114P_Y
I/O, L#N_Y	7	G1	XC2S100E, 150E, 300E, 600E	-	I/O, L82N_Y	I/O, L107N_Y	I/O, L114N	I/O, L114N_Y	I/O, L114N	I/O, L114N_Y

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O, L#P_YY	7	L5	All	-	I/O, L75P_YY	I/O, L99P_YY	I/O, L105P_YY	I/O, L105P_YY	I/O, L105P_YY	I/O, L105P_YY
I/O (IRDY), L#N_YY	7	L6	All	-	I/O (IRDY), L75N_YY	I/O (IRDY), L99N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY
I/O (TRDY)	6	M1	-	-	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)
I/O	6	M2	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P_Y	6	M3	XC2S200E, 300E, 600E	-	-	I/O	I/O, L104P_Y	I/O, L104P_Y	I/O, L104P	I/O, L104P_Y
I/O, L#N_Y	6	M4	XC2S100E, 150E, 200E, 300E, 600E	XC2S400E, 600E	I/O, L74P_Y	I/O, L98P_Y	I/O, L104N_Y	I/O, L104N_Y	I/O, VREF Bank 6, L104N	I/O, VREF Bank 6, L104N_Y
I/O, L#P_Y	6	M5	XC2S100E, 150E, 300E, 400E	-	I/O, L74N_Y	I/O, L98N_Y	I/O, L103P	I/O, L103P_Y	I/O, L103P_Y	I/O, L103P
I/O, L#N_Y	6	M6	XC2S300E, 400E	-	-	-	I/O, L103N	I/O, L103N_Y	I/O, L103N_Y	I/O, L103N
I/O	6	N1	-	-	-	-	-	I/O	I/O	I/O
I/O	6	N2	-	-	I/O, L73P	I/O, L97P	I/O	I/O	I/O	I/O
I/O, VREF Bank 6, L#P	6	N3	XC2S200E, 400E	All	I/O, VREF Bank 6, L73N	I/O, VREF Bank 6, L97N	I/O, VREF Bank 6, L102P_Y	I/O, VREF Bank 6, L102P	I/O, VREF Bank 6, L102P_Y	I/O, VREF Bank 6, L102P
I/O, L#N	6	N4	XC2S100E, 150E, 200E, 400E	-	I/O, L72P_Y	I/O, L96P_Y	I/O, L102N_Y	I/O, L102N	I/O, L102N_Y	I/O, L102N
I/O, L#P_Y	6	N5	XC2S100E, 150E, 300E, 600E	-	I/O, L72N_Y	I/O, L96N_Y	I/O, L101P	I/O, L101P_Y	I/O, L101P	I/O, L101P_Y
I/O, L#N_Y	6	N6	XC2S300E, 600E	-	-	-	I/O, L101N	I/O, L101N_Y	I/O, L101N	I/O, L101N_Y
I/O, L#P_Y	6	P1	XC2S150E, 200E, 300E, 600E	-	-	I/O, L95P_Y	I/O, L100P_Y	I/O, L100P_Y	I/O, L100P	I/O, L100P_Y
I/O, L#N_Y	6	P2	XC2S100E, 150E, 200E, 300E, 600E	-	I/O, L71P_Y	I/O, L95N_Y	I/O, L100N_Y	I/O, L100N_Y	I/O, L100N	I/O, L100N_Y
I/O	6	R1	XC2S100E, 150E	-	I/O, L71N_Y	I/O, L94P_Y	I/O	I/O	I/O	I/O
I/O, L#P_Y	6	P3	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L94N_Y	I/O, L99P_Y	I/O, L99P_Y	I/O,L99P_Y	I/O,L99P_Y
I/O, L#N_Y	6	P4	XC2S200E, 300E, 400E, 600E	-	-	-	I/O, L99N_Y	I/O, L99N_Y	I/O, L99N_Y	I/O, L99N_Y
I/O, L#P_YY	6	P5	All	-	I/O, L70P_YY	I/O, L93P_YY	I/O, L98P_YY	I/O, L98P_YY	I/O, L98P_YY	I/O, L98P_YY
I/O, L#N_YY	6	P6	All	-	I/O, L70N_YY	I/O, L93N_YY	I/O, L98N_YY	I/O, L98N_YY	I/O, L98N_YY	I/O, L98N_YY

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name					Device-Specific Pinouts: XC2S					
Function	Bank	Pin	LVDS Async. Output Option	V_{REF} Option	100E	150E	200E	300E	400E	600E
I/O, L#P_YY	0	A6	All	-	I/O, L2P_YY	I/O, L3P_YY	I/O, L3P_YY	I/O, L3P_YY	I/O, L3P_YY	I/O, L3P_YY
I/O, VREF Bank 0, L#N_YY	0	B6	All	All	I/O, VREF Bank 0, L2N_YY	I/O, VREF Bank 0, L3N_YY	I/O, VREF Bank 0, L3N_YY	I/O, VREF Bank 0, L3N_YY	I/O, VREF Bank 0, L3N_YY	I/O, VREF Bank 0, L3N_YY
I/O	0	C6	XC2S100E	-	I/O, L1P_Y	I/O	I/O	I/O	I/O	I/O
I/O, L#P	0	A5	XC2S100E	-	I/O, L1N_Y	I/O, L2P	I/O, L2P	I/O, L2P	I/O, L2P	I/O, L2P
I/O, L#N	0	B5	-	-	-	I/O, L2N	I/O, L2N	I/O, L2N	I/O, L2N	I/O, L2N
I/O	0	D6	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P	0	B4	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L0P_Y	I/O, L1P	I/O, L1P_Y	I/O, L1P_Y	I/O, L1P_Y	I/O, L1P_Y
I/O, L#N	0	C5	XC2S100E, 200E, 300E, 400E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L0N_Y	I/O, L1N	I/O, VREF Bank 0, L1N_Y	I/O, VREF Bank 0, L1N_Y	I/O, VREF Bank 0, L1N_Y	I/O, VREF Bank 0, L1N_Y
I/O	0	A4	-	-	I/O	I/O	I/O	I/O	I/O	I/O
I/O, L#P	0	A3	XC2S150E, 400E, 600E	-	-	I/O, L0P_Y	I/O, L0P	I/O, L0P	I/O, L0P_Y	I/O, L0P_Y
I/O, L#N	0	B3	XC2S150E, 400E, 600E	-	-	I/O, L0N_Y	I/O, L0N	I/O, L0N	I/O, L0N_Y	I/O, L0N_Y
I/O	0	C4	-	-	-	-	-	I/O	I/O	I/O
I/O	0	D5	-	-	I/O	I/O	I/O	I/O	I/O	I/O
TCK	-	E6	-	-	TCK	TCK	TCK	TCK	TCK	TCK

Notes:
1. Although designated with the _YY suffix in the XC2S100E, XC2S150E, XC2S200E, and XC2S300E, these differential pairs are not asynchronous in the XC2S400E.

FG456 Differential Clock Pins

Clock	Bank	P		N	
		Pin	Name	Pin	Name
GCK0	4	AA12	GCK0, I	Y12	I/O (DLL), L#P
GCK1	5	AB12	GCK1, I	AB11	I/O (DLL), L#N
GCK2	1	A11	GCK2, I	A12	I/O (DLL), L#P
GCK3	0	C11	GCK3, I	B11	I/O (DLL), L#N

Additional FG456 Package Pins

VCCINT Pins								
D4[(1)]	D19[(1)]	E5	E18	F6	F17	G7	G8	G15
G16	H7	H16	R7	R16	T7	T8	T15	T16
U6	U17	V5	V18	W4[(1)]	W19[(1)]	-	-	-
VCCO Bank 0 Pins								
F7	F8	G9	G10	-	-	-	-	-

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L201P	7	E4	XC2S400E	-	I/O, L201P_Y	I/O, L201P
I/O, L201N	7	F5	XC2S400E	-	I/O, L201N_Y	I/O, L201N
I/O, VREF Bank 7, L200P	7	F4	XC2S600E	All	I/O, VREF Bank 7, L200P	I/O, VREF Bank 7, L200P_Y
I/O, L200N	7	F3	XC2S600E	-	I/O, L200N	I/O, L200N_Y
I/O, L199P	7	F2	XC2S600E	-	-	I/O, L199P_Y
I/O, L199N	7	F1	XC2S600E	-	I/O	I/O, L199N_Y
I/O, L198P	7	G6	XC2S400E	-	I/O, L198P_Y	I/O, L198P
I/O, L198N	7	G5	XC2S400E	-	I/O, L198N_Y	I/O, L198N
I/O, L197P	7	G4	XC2S600E	-	I/O, L197P	I/O, L197P_Y
I/O, L197N	7	G3	XC2S600E	-	I/O, L197N	I/O, L197N_Y
I/O, VREF Bank 7, L196P_YY	7	G2	All	All	I/O, VREF Bank 7, L196P_YY	I/O, VREF Bank 7, L196P_YY
I/O, L196N_YY	7	G1	All	-	I/O, L196N_YY	I/O, L196N_YY
I/O	7	H7	-	-	I/O	I/O
I/O, L195P_YY	7	H6	All	-	I/O, L195P_YY	I/O, L195P_YY
I/O, L195N_YY	7	H5	All	-	I/O, L195N_YY	I/O, L195N_YY
I/O	7	J8	-	-	-	I/O
I/O, L194P	7	H2	XC2S400E	-	I/O, L194P_Y	I/O, L194P
I/O, L194N	7	H1	XC2S400E	-	I/O, L194N_Y	I/O, L194N
I/O, L193P	7	J7	XC2S600E	XC2S600E	I/O	I/O, VREF Bank 7, L193P_Y
I/O, L193N	7	J6	XC2S600E	-	-	I/O, L193N_Y
I/O	7	J5	-	-	I/O	I/O
I/O, L192P_YY	7	J4	All	-	I/O, L192P_YY	I/O, L192P_YY
I/O, L192N_YY	7	J3	All	-	I/O, L192N_YY	I/O, L192N_YY
I/O	7	K5	-	-	I/O	I/O
I/O, VREF Bank 7, L191P_YY	7	J2	All	All	I/O, VREF Bank 7, L191P_YY	I/O, VREF Bank 7, L191P_YY
I/O, L191N_YY	7	J1	All	-	I/O, L191N_YY	I/O, L191N_YY
I/O, L190P_YY	7	K8	All	-	I/O, L190P_YY	I/O, L190P_YY
I/O, L190N_YY	7	K7	All	-	I/O, L190N_YY	I/O, L190N_YY
I/O	7	K4	-	-	-	I/O
I/O, L189P_YY	7	K3	All	-	I/O, L189P_YY	I/O, L189P_YY
I/O, L189N_YY	7	K2	All	-	I/O, L189N_YY	I/O, L189N_YY
I/O	7	K1	-	-	-	I/O

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L39N	1	F18	XC2S600E	-	I/O, L39N	I/O, L39N_Y
I/O, L38P	1	D18	XC2S600E	XC2S600E	-	I/O, VREF Bank 1, L38P_Y
I/O, L38N	1	C18	XC2S600E	-	I/O	I/O, L38N_Y
I/O, L37P_YY	1	B18	All	-	I/O, L37P_YY	I/O, L37P_YY
I/O, L37N_YY	1	A18	All	-	I/O, L37N_YY	I/O, L37N_YY
I/O, L36P_YY	1	H17	All	-	I/O, L36P_YY	I/O, L36P_YY
I/O, L36N_YY	1	G17	All	-	I/O, L36N_YY	I/O, L36N_YY
I/O, VREF Bank 1, L35P_YY	1	E18	All	All	I/O, VREF Bank 1, L35P_YY	I/O, VREF Bank 1, L35P_YY
I/O, L35N_YY	1	E17	All	-	I/O, L35N_YY	I/O, L35N_YY
I/O, L34P_YY	1	D17	All	-	I/O, L34P_YY	I/O, L34P_YY
I/O, L34N_YY	1	C17	All	-	I/O, L34N_YY	I/O, L34N_YY
I/O	1	H16	-	-	-	I/O
I/O, L33P	1	B17	XC2S600E	-	I/O, L33P	I/O, L33P_Y
I/O, L33N	1	A17	XC2S600E	-	I/O, L33N	I/O, L33N_Y
I/O	1	G16	-	-	-	I/O
I/O, L32P_YY	1	F16	All	-	I/O, L32P_YY	I/O, L32P_YY
I/O, L32N_YY	1	E16	All	-	I/O, L32N_YY	I/O, L32N_YY
I/O, L31P_YY	1	C16	All	-	I/O, L31P_YY	I/O, L31P_YY
I/O, L31N_YY	1	B16	All	-	I/O, L31N_YY	I/O, L31N_YY
I/O	1	A16	-	-	-	I/O
I/O, L30P	1	J15	-	-	I/O, L30P	I/O, L30P
I/O, L30N	1	H15	-	-	I/O, L30N	I/O, L30N
I/O	1	G15	-	-	-	I/O
I/O, L29P_YY	1	F15	All	-	I/O, L29P_YY	I/O, L29P_YY
I/O, L29N_YY	1	E15	All	-	I/O, L29N_YY	I/O, L29N_YY
I/O, VREF Bank 1, L28P_YY	1	B15	All	All	I/O, VREF Bank 1, L28P_YY	I/O, VREF Bank 1, L28P_YY
I/O, L28N_YY	1	A15	All	-	I/O, L28N_YY	I/O, L28N_YY
I/O	1	D15	-	-	-	I/O
I/O, L27P_YY	1	J14	All	-	I/O, L27P_YY	I/O, L27P_YY
I/O, L27N_YY	1	H14	All	-	I/O, L27N_YY	I/O, L27N_YY
I/O	1	G14	-	-	-	I/O
I/O, L26P	1	F14	XC2S600E	-	I/O, L26P	I/O, L26P_Y
I/O, L26N	1	E14	XC2S600E	-	I/O, L26N	I/O, L26N_Y

Additional FG676 Package Pins *(Continued)*

GND Pins						
A1	A26	B2	B25	C3	C12	C15
C24	D4	D8	D19	D23	F10	F17
H4	H23	K6	K21	L11	L12	L13
L14	L15	L16	M3	M11	M12	M13
M14	M15	M16	M24	N11	N12	N13
N14	N15	N16	P11	P12	P13	P14
P15	P16	R3	R11	R12	R13	R14
R15	R16	R24	T11	T12	T13	T14
T15	T16	U6	U21	W4	W23	AA10
AA17	AC4	AC8	AC19	AC23	AD3	AD12
AD15	AD24	AE2	AE25	AF1	AF26	-
Not Connected Pins (XC2S400E Only)						
A12	A16	A23	B3	C1	C2	C10
C11	C25	D2	D15	D18	D24	D25
E7	E13	E19	F2	F6	F8	F12
F20	F22	G10	G14	G15	G16	G26
H10	H13	H16	H25	J6	J8	J12
J13	K1	K4	K22	K24	L3	L19
L22	L26	M4	M9	M22	N1	N4
N9	N18	N19	N23	P4	P5	P18
P19	P24	R4	R7	R19	T3	T24
U1	U4	U7	U24	U25	V8	V12
V13	V21	W12	W13	W14	W16	Y3
Y7	Y21	AA7	AA9	AA22	AB15	AB16
AB17	AB22	AC1	AC15	AC22	AC25	AC26
AD1	AD2	AD10	AD11	AD13	AD14	AE5
AE19	AE24	AF4	AF16	AF18	AF20	-