AMD Xilinx - XC2S100E-6PQG208C Datasheet

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

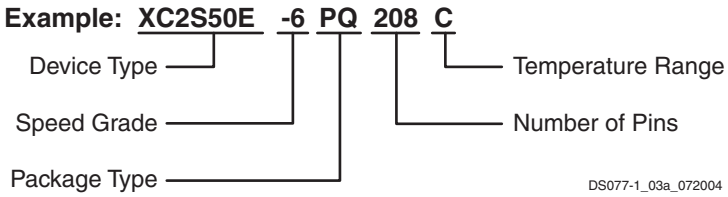
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	600
Number of Logic Elements/Cells	2700
Total RAM Bits	40960
Number of I/O	146
Number of Gates	100000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s100e-6pqg208c

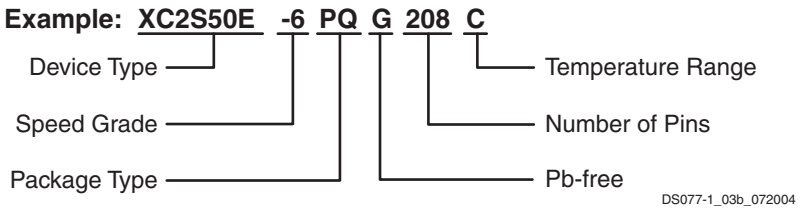
Ordering Information

Spartan-IIE devices are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a special "G" character in the ordering code.

Standard Packaging



Pb-Free Packaging



Device Ordering Options

Device
XC2S50E
XC2S100E
XC2S150E
XC2S200E
XC2S300E
XC2S400E
XC2S600E

Speed Grade	
-6	Standard Performance
-7	Higher Performance(1)

Package Type / Number of Pins	
TQ(G)144	144-pin Plastic Thin QFP
PQ(G)208	208-pin Plastic QFP
FT(G)256	256-ball Fine Pitch BGA
FG(G)456	456-ball Fine Pitch BGA
FG(G)676	676-ball Fine Pitch BGA

Temperature Range (T_J)(2)	
C = Commercial	0°C to +85°C
I = Industrial	–40°C to +100°C

Notes:
1. The -7 speed grade is exclusively available in the Commercial temperature range.
2. See www.xilinx.com for information on automotive temperature range devices.

Device Part Marking

Figure 2 is a top marking example for Spartan-IIE FPGAs in the quad-flat packages. The markings for BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator.

The "7C" and "6I" Speed Grade/Temperature Range part combinations may be dual marked as "7C/6I". Devices with the dual mark can be used as either -7C or -6I devices. Devices with a single mark are only guaranteed for the marked speed grade and temperature range.

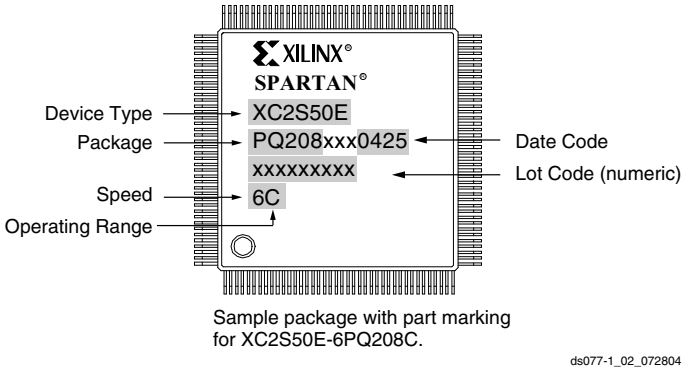


Figure 2: **Spartan-IIE QFP Marking Example**

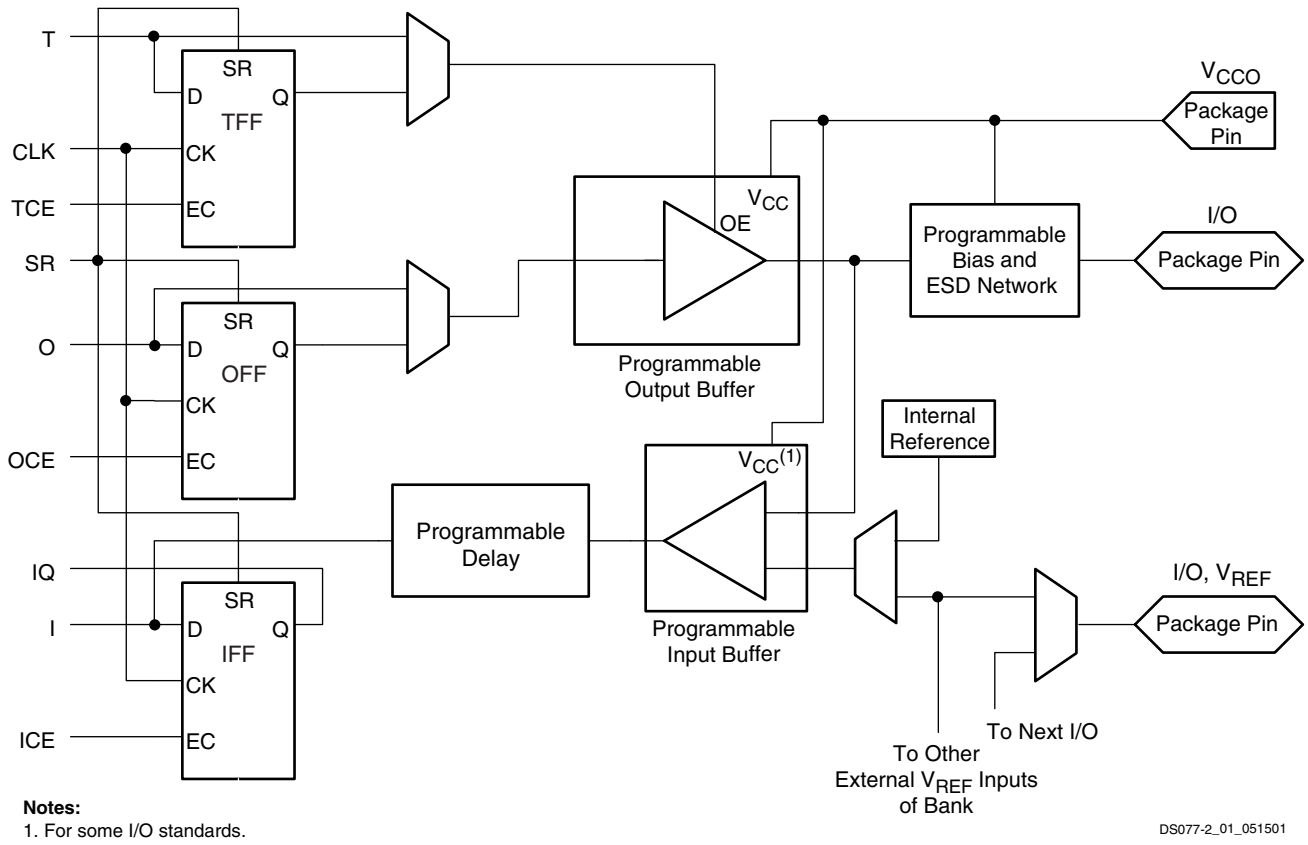


Figure 4: **Spartan-IIE Input/Output Block (IOB)**

Table 3: **Standards Supported by I/O (Typical Values)**

I/O Standard	Input Reference Voltage (V_{REF})	Input Voltage (V_{CCO})	Output Source Voltage (V_{CCO})	Board Termination Voltage (V_{TT})
LVTTL (2-24 mA)	N/A	3.3	3.3	N/A
LVCMOS2	N/A	2.5	2.5	N/A
LVCMOS18	N/A	1.8	1.8	N/A
PCI (3V, 33 MHz/66 MHz)	N/A	3.3	3.3	N/A
GTL	0.8	N/A	N/A	1.2
GTL+	1.0	N/A	N/A	1.5
HSTL Class I	0.75	N/A	1.5	0.75
HSTL Class III	0.9	N/A	1.5	1.5
HSTL Class IV	0.9	N/A	1.5	1.5
SSTL3 Class I and II	1.5	N/A	3.3	1.5
SSTL2 Class I and II	1.25	N/A	2.5	1.25
CTT	1.5	N/A	3.3	1.5
AGP	1.32	N/A	3.3	N/A
LVDS, Bus LVDS	N/A	N/A	2.5	N/A
LVPECL	N/A	N/A	3.3	N/A

Input/Output Block

The Spartan-IIE FPGA IOB, as seen in Figure 4, features inputs and outputs that support a wide variety of I/O signaling standards. These high-speed inputs and outputs are capable of supporting various state of the art memory and bus interfaces. The default standard is LVTTL. Table 3 lists several of the standards which are supported along with the required reference (V_{REF}), output (V_{CCO}) and board termination (V_{TT}) voltages needed to meet the standard. For more details on the I/O standards and termination application examples, see XAPP179, "*Using SelectIO Interfaces in Spartan-II and Spartan-IIE FPGAs*."

The three IOB registers function either as edge-triggered D-type flip-flops or as level-sensitive latches. Each IOB has a clock signal (CLK) shared by the three registers and independent Clock Enable (CE) signals for each register.

In addition to the CLK and CE control signals, the three registers share a Set/Reset (SR). For each register, this signal can be independently configured as a synchronous Set, a synchronous Reset, an asynchronous Preset, or an asynchronous Clear.

A feature not shown in the block diagram, but controlled by the software, is polarity control. The input and output buffers and all of the IOB control signals have independent polarity controls.

Configurable Logic Block

The basic building block of the Spartan-IIE FPGA CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and storage element. The output from the function generator in each LC drives the CLB output or the D input of the flip-flop. Each Spartan-IIE FPGA CLB contains four LCs, organized in two similar slices; a single slice is shown in Figure 6.

In addition to the four basic LCs, the Spartan-IIE FPGA CLB contains logic that combines function generators to provide functions of five or six inputs.

Look-Up Tables

Spartan-IIE FPGA function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16 x 1-bit dual-port synchronous RAM.

The Spartan-IIE FPGA LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

Storage Elements

Storage elements in the Spartan-IIE FPGA slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals may be configured to operate asynchronously.

All control signals are independently invertible, and are shared by the two flip-flops within the slice.

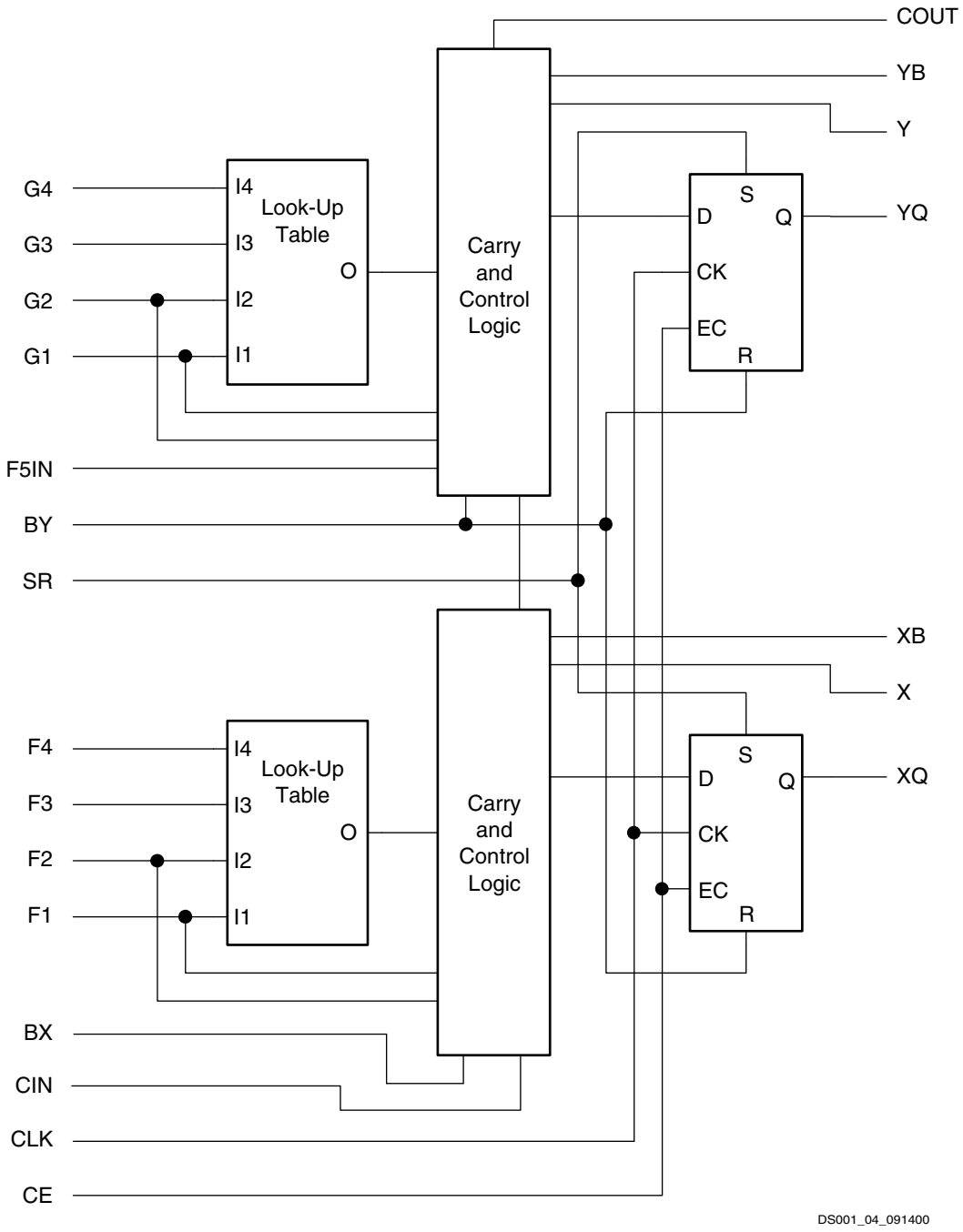


Figure 6: **Spartan-IIE CLB Slice** (two identical slices in each CLB)

Additional Logic

The F5 multiplexer in each slice combines the function generator outputs (Figure 7). This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the two F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Table 7 shows the depth and width aspect ratios for the block RAM.

Table 7: **Block RAM Port Aspect Ratios**

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

The Spartan-IIE FPGA block RAM also includes dedicated routing to provide an efficient interface with both CLBs and other block RAMs. See Xilinx Application Note XAPP173 for more information on block RAM.

Programmable Routing

It is the longest delay path that limits the speed of any design. Consequently, the Spartan-IIE FPGA routing architecture and its place-and-route software were defined jointly to minimize long-path delays and yield the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

The software automatically uses the best available routing based on user timing requirements. The details are provided here for reference.

Local Routing

The local routing resources, as shown in Figure 9, provide the following three types of connections:

- Interconnections among the LUTs, flip-flops, and General Routing Matrix (GRM), described below.
- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM

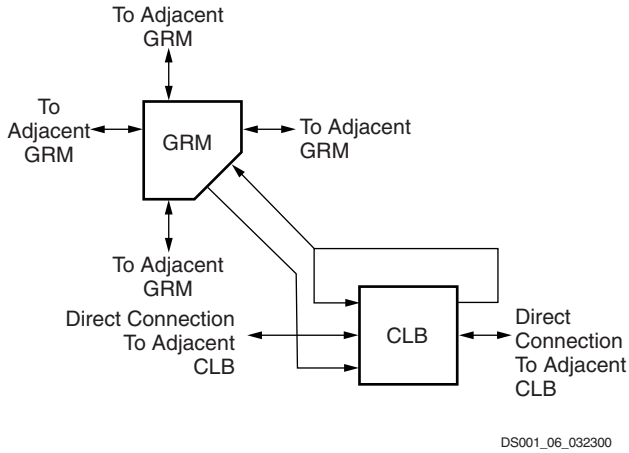


Figure 9: **Spartan-IIE Local Routing**

General Purpose Routing

Most Spartan-IIE FPGA signals are routed on the general purpose routing, and consequently, the majority of interconnect resources are associated with this level of the routing hierarchy. The general routing resources are located in horizontal and vertical routing channels associated with the rows and columns of CLBs. The general-purpose routing resources are listed below.

- Adjacent to each CLB is a General Routing Matrix (GRM). The GRM is the switch matrix through which horizontal and vertical routing resources connect, and is also the means by which the CLB gains access to the general purpose routing.
- 24 single-length lines route GRM signals to adjacent GRMs in each of the four directions.
- 96 buffered Hex lines route GRM signals to other GRMs six blocks away in each one of the four directions. Organized in a staggered pattern, Hex lines may be driven only at their endpoints. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source). One third of the Hex lines are bidirectional, while the remaining ones are unidirectional.
- 12 Longlines are buffered, bidirectional wires that distribute signals across the device quickly and efficiently. Vertical Longlines span the full height of the device, and horizontal ones span the full width of the device.

I/O Routing

Spartan-IIE devices have additional routing resources around their periphery that form an interface between the CLB array and the IOBs. This additional routing, called the VersaRing™ routing, facilitates pin-swapping and pin-locking, such that logic redesigns can adapt to existing PCB layouts. Time-to-market is reduced, since PCBs and other system components can be manufactured while the logic design is still in progress.

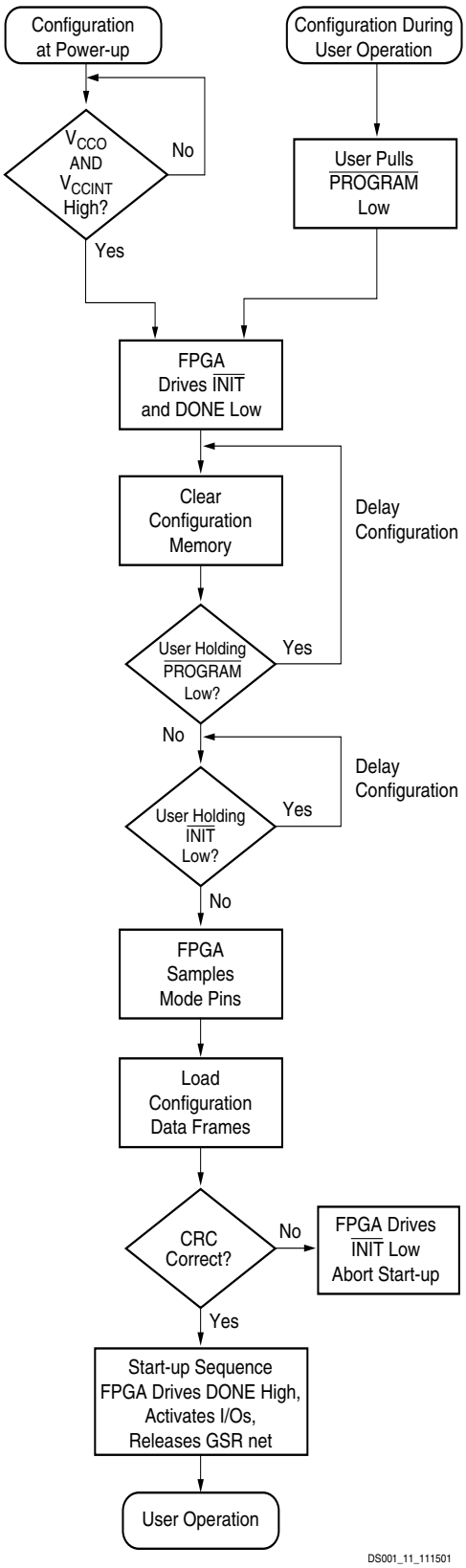


Figure 16: **Configuration Flow Diagram**

Clearing Configuration Memory

The device indicates that clearing the configuration memory is in progress by driving $\overline{\text{INIT}}$ Low.

Delaying Configuration

At this time, the user can delay configuration by holding either $\overline{\text{PROGRAM}}$ or $\overline{\text{INIT}}$ Low, which causes the device to remain in the memory clearing phase. Note that the bidirectional $\overline{\text{INIT}}$ line is driving a Low logic level during memory clearing. Thus, to avoid contention, use an open-drain driver to keep $\overline{\text{INIT}}$ Low.

With no delay in force, the device indicates that the memory is completely clear by driving $\overline{\text{INIT}}$ High. The FPGA samples its mode pins on this Low-to-High transition.

Loading Configuration Data

Once $\overline{\text{INIT}}$ is High, the user can begin loading configuration data frames into the device. The details of loading the configuration data are discussed in the sections treating the configuration modes individually. The sequence of operations necessary to load configuration data using the serial modes is shown in Figure 18. Loading data using the Slave Parallel mode is shown in Figure 21, page 28.

CRC Error Checking

After the loading of configuration data, a CRC value embedded in the configuration file is checked against a CRC value calculated within the FPGA. If the CRC values do not match, the FPGA drives $\overline{\text{INIT}}$ Low to indicate that an error has occurred and configuration is aborted. Note that attempting to load an incorrect bitstream causes configuration to fail and can damage the device.

To reconfigure the device, the $\overline{\text{PROGRAM}}$ pin should be asserted to reset the configuration logic. Recycling power also resets the FPGA for configuration. See Clearing Configuration Memory.

Start-up

The start-up sequence oversees the transition of the FPGA from the configuration state to full user operation. A match of CRC values, indicating a successful loading of the configuration data, initiates the sequence.

If CCLK is slower than F_{CCNH}, the FPGA will never assert BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

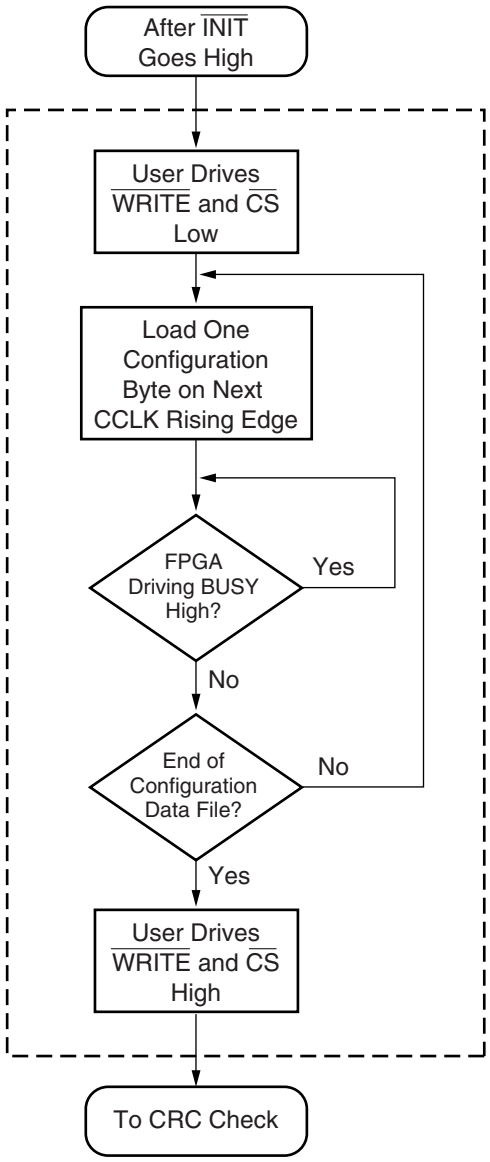


Figure 21: **Loading Configuration Data for the Slave Parallel Mode**

A configuration packet does not have to be written in one continuous stretch, rather it can be split into many write sequences. Each sequence would involve assertion of $\overline{CS}$.

In applications where multiple clock cycles may be required to access the configuration data before each byte can be loaded into the Slave Parallel interface, a new byte of data may not be ready for each consecutive CCLK edge. In such a case the $\overline{CS}$ signal may be deasserted until the next byte is valid on D0-D7. While $\overline{CS}$ is High, the Slave Parallel interface does not expect any data and ignores all CCLK transitions. However, to avoid aborting configuration, $\overline{WRITE}$ must continue to be asserted while $\overline{CS}$ is asserted during CCLK transitions.

Abort

To abort configuration during a write sequence, deassert $\overline{WRITE}$ while holding $\overline{CS}$ Low. The abort operation is initiated at the rising edge of CCLK. The device will remain BUSY until the aborted operation is complete. After aborting configuration, data is assumed to be unaligned to word boundaries and the FPGA requires a new synchronization word prior to accepting any new packets.

Boundary-Scan Configuration Mode

In the boundary-scan mode, no nondedicated pins are required, configuration being done entirely through the IEEE 1149.1 Test Access Port (TAP).

Configuration through the TAP uses the special CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port.

1. Load the CFG_IN instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a standard configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the JSTART instruction into IR
6. Enter the SDR state
7. Clock TCK (if selected) through the startup sequence (the length is programmable)
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode simply locks out the other modes. The boundary-scan mode is selected by a <10x> on the mode pins (M0, M1, M2). Note that the $\overline{PROGRAM}$ pin must be pulled High prior to reconfiguration. A Low on the $\overline{PROGRAM}$ pin resets the TAP controller and no boundary scan operations can be performed. See Xilinx Application Note XAPP188 for more information on boundary-scan configuration.

Readback

The configuration data stored in the Spartan-IIE FPGA configuration memory can be read back for verification. Along with the configuration data it is possible to read back the contents of all flip-flops/latches, LUT RAMs, and block RAMs. This capability is used for real-time debugging.

For more detailed information see Xilinx Application Note XAPP176, *Configuration and Readback of the Spartan-II and Spartan-IIE FPGA Families.*

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
T_J	Junction temperature	Commercial	0	85	°C
		Industrial	–40	100	°C
V_{CCINT}	Supply voltage relative to GND(1)	Commercial	1.8 – 5%	1.8 + 5%	V
		Industrial	1.8 – 5%	1.8 + 5%	V
V_{CCO}	Supply voltage relative to GND(2)	Commercial	1.2	3.6	V
		Industrial	1.2	3.6	V
T_{IN}	Input signal transition time(3)		-	250	ns

Notes:
1. Functional operation is guaranteed down to a minimum V_{CCINT} of 1.62V (Nominal V_{CCINT} –10%). For every 50 mV reduction in V_{CCINT} below 1.71V (nominal V_{CCINT} –5%), all delay parameters increase by approximately 3%.
2. Minimum and maximum values for V_{CCO} vary according to the I/O standard selected.
3. Input and output measurement threshold is ~50% of V_{CCO}. See Delay Measurement Methodology, page 41 for specific details.

DC Characteristics Over Operating Conditions

Symbol	Description			Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data may be lost)			1.5	-	-	V
V_{DRIO}	Data retention V_{CCO} voltage (below which configuration data may be lost)			1.2	-	-	V
I_{CCINTQ}	Quiescent V_{CCINT} supply current(1)	XC2S50E	Commercial	-	10	200	mA
			Industrial	-	10	200	mA
		XC2S100E	Commercial	-	10	200	mA
			Industrial	-	10	200	mA
		XC2S150E	Commercial	-	10	300	mA
			Industrial	-	10	300	mA
		XC2S200E	Commercial	-	10	300	mA
			Industrial	-	10	300	mA
		XC2S300E	Commercial	-	12	300	mA
			Industrial	-	12	300	mA
		XC2S400E	Commercial	-	15	300	mA
			Industrial	-	15	300	mA
		XC2S600E	Commercial	-	15	400	mA
			Industrial	-	15	400	mA
I_{CCOQ}	Quiescent V_{CCO} supply current(1)			-	-	2	mA
I_{REF}	V_{REF} current per V_{REF} pin			-	-	20	µA
I_L	Input or output leakage current per pin			–10	-	+10	µA
C_{IN}	Input capacitance (sample tested)	TQ, PQ, FG, FT packages		-	-	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V (sample tested)(2)			-	-	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.6V (sample tested)(2)			-	-	0.25	mA

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not provide valid logic levels when input pins are connected to other circuits.

Global Clock Setup and Hold for LVTTL Standard, *with* DLL (Pin-to-Pin)

Symbol	Description	Speed Grade		Units
		-7	-6	
		Min	Min	
T_{PSDLL} / T_{PHDLL}	Input setup and hold time relative to global clock input signal for LVTTL standard, no delay, IFF,(1) *with* DLL	1.6 / 0	1.7 / 0	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DLL output jitter is already included in the timing calculation.
4. For data input with different standards, adjust the setup time delay by the values shown in IOB Input Delay Adjustments for Different Standards, page 38. For a global clock input with standards other than LVTTL, adjust delays with values from the I/O Standard Global Clock Input Adjustments, page 42.
5. A zero hold time listing indicates no hold time or a negative hold time.

Global Clock Setup and Hold for LVTTL Standard, *without* DLL (Pin-to-Pin)

Symbol	Description	Device	Speed Grade		Units
			-7	-6	
			Min	Min	
T_{PSFD} / T_{PHFD}	Input setup and hold time relative to global clock input signal for LVTTL standard, with delay, IFF,(1) *without* DLL	XC2S50E	1.8 / 0	1.8 / 0	ns
		XC2S100E	1.8 / 0	1.8 / 0	ns
		XC2S150E	1.9 / 0	1.9 / 0	ns
		XC2S200E	1.9 / 0	1.9 / 0	ns
		XC2S300E	2.0 / 0	2.0 / 0	ns
		XC2S400E	2.0 / 0	2.0 / 0	ns
		XC2S600E	2.1 / 0	2.1 / 0	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. For data input with different standards, adjust the setup time delay by the values shown in IOB Input Delay Adjustments for Different Standards, page 38. For a global clock input with standards other than LVTTL, adjust delays with values from the I/O Standard Global Clock Input Adjustments, page 42.

Calculation of T_{IOOP} as a Function of Capacitance

T_{IOOP} is the propagation delay from the O Input of the IOB to the pad. The values for T_{IOOP} are based on the standard capacitive load (C_{SL}) for each I/O standard as listed in the table Constants for Calculating T_{IOOP}, below.

For other capacitive loads, use the formulas below to calculate an adjusted propagation delay, T_{IOOP1}.

$$T_{IOOP1} = T_{IOOP} + Adj + (C_{LOAD} - C_{SL}) * F_L$$

Where:

- Adj — is selected from IOB Output Delay Adjustments for Different Standards(1), page 40, according to the I/O standard used
- C_{LOAD} — is the capacitive load for the design
- F_L — is the capacitance scaling factor

Delay Measurement Methodology

Standard	V_L(1)	V_H(1)	Meas. Point	V_{REF} Typ(2)
LVTTL	0	3	1.4	-
LVCMOS2	0	2.5	1.125	-
PCI33_3	Per PCI Spec			-
PCI66_3	Per PCI Spec			-
GTL	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.80
GTL+	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.0
HSTL Class I	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL Class III	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL Class IV	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
SSTL3 I and II	V_{REF} – 1.0	V_{REF} + 1.0	V_{REF}	1.5
SSTL2 I and II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
CTT	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.5
AGP	V_{REF} – (0.2xV_{CCO})	V_{REF} + (0.2xV_{CCO})	V_{REF}	Per AGP Spec
LVDS	1.2 – 0.125	1.2 + 0.125	1.2	
LVPECL	1.6 – 0.3	1.6 + 0.3	1.6	

Notes:

1. Input waveform switches between V_L and V_H.
2. Measurements are made at V_{REF} Typ, Maximum, and Minimum. Worst-case values are reported.
3. I/O parameter measurements are made with the capacitance values shown in the following table, Constants for Calculating T_{IOOP}. Refer to Application Note XAPP179 for appropriate terminations.
4. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Constants for Calculating T_{IOOP}

Standard	C_{SL}(1) (pF)	F_L (ns/pF)
LVTTL Fast Slew Rate, 2 mA drive	35	0.41
LVTTL Fast Slew Rate, 4 mA drive	35	0.20
LVTTL Fast Slew Rate, 6 mA drive	35	0.13
LVTTL Fast Slew Rate, 8 mA drive	35	0.079
LVTTL Fast Slew Rate, 12 mA drive	35	0.044
LVTTL Fast Slew Rate, 16 mA drive	35	0.043
LVTTL Fast Slew Rate, 24 mA drive	35	0.033
LVTTL Slow Slew Rate, 2 mA drive	35	0.41
LVTTL Slow Slew Rate, 4 mA drive	35	0.20
LVTTL Slow Slew Rate, 6 mA drive	35	0.100
LVTTL Slow Slew Rate, 8 mA drive	35	0.086
LVTTL Slow Slew Rate, 12 mA drive	35	0.058
LVTTL Slow Slew Rate, 16 mA drive	35	0.050
LVTTL Slow Slew Rate, 24 mA drive	35	0.048
LVCMOS2	35	0.041
LVCMOS18	35	0.050
PCI 33 MHz 3.3V	10	0.050
PCI 66 MHz 3.3V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

Notes:

1. I/O parameter measurements are made with the capacitance values shown above. Refer to Application Note XAPP179 for appropriate terminations.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L28P	4	P89	XC2S50E, 100E, 200E, 300E	-
VCCINT	-	P90	-	-
VCCO	-	P91	-	-
GND	-	P92	-	-
I/O, L27N	4	P93	XC2S50E, 100E, 200E, 300E	-
I/O, L27P	4	P94	XC2S50E, 100E, 200E, 300E	XC2S100E, 150E, 200E, 300E
I/O	4	P95	-	-
I/O	4	P96	-	-
I/O, L26N_YY	4	P97	All	-
I/O, VREF Bank 4, L26P_YY	4	P98	All	All
I/O	4	P99	-	-
I/O	4	P100	-	XC2S200E, 300E
I/O, L25N_YY	4	P101	All	-
I/O, L25P_YY	4	P102	All	-
GND	-	P103	-	-
DONE	3	P104	-	-
VCCO	-	P105	-	-
$\overline{\text{PROGRAM}}$	-	P106	-	-
I/O ($\overline{\text{INIT}}$), L24N_YY	3	P107	All	-
I/O (D7), L24P_YY	3	P108	All	-
I/O	3	P109	-	XC2S200E, 300E
I/O	3	P110	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 3, L23N	3	P111	XC2S50E, 150E, 200E, 300E	All
I/O, L23P	3	P112	XC2S50E, 150E, 200E, 300E	-
I/O	3	P113	-	-
I/O	3	P114	-	-
I/O, L22N	3	P115	XC2S50E, 300E	XC2S100E, 150E, 200E, 300E
I/O (D6), L22P	3	P116	XC2S50E, 300E	-
GND	-	P117	-	-
VCCO	-	P118	-	-
VCCINT	-	P119	-	-
I/O (D5), L21N_YY	3	P120	All	-
I/O, L21P_YY	3	P121	All	-
I/O, L20N_YY	3	P122	All	-
I/O, L20P_YY	3	P123	All	-
GND	-	P124	-	-
I/O, VREF Bank 3, L19N	3	P125	XC2S50E, 300E	All
I/O (D4), L19P	3	P126	XC2S50E, 300E	-
I/O	3	P127	-	-
VCCINT	-	P128	-	-
I/O (TRDY)	3	P129	-	-
VCCO	-	P130	-	-
GND	-	P131	-	-
I/O (IRDY), L18N_YY	2	P132	All	-
I/O, L18P_YY	2	P133	All	-

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O, L#P_YY	7	L5	All	-	I/O, L75P_YY	I/O, L99P_YY	I/O, L105P_YY	I/O, L105P_YY	I/O, L105P_YY	I/O, L105P_YY
I/O (IRDY), L#N_YY	7	L6	All	-	I/O (IRDY), L75N_YY	I/O (IRDY), L99N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY
I/O (TRDY)	6	M1	-	-	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)
I/O	6	M2	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P_Y	6	M3	XC2S200E, 300E, 600E	-	-	I/O	I/O, L104P_Y	I/O, L104P_Y	I/O, L104P	I/O, L104P_Y
I/O, L#N_Y	6	M4	XC2S100E, 150E, 200E, 300E, 600E	XC2S400E, 600E	I/O, L74P_Y	I/O, L98P_Y	I/O, L104N_Y	I/O, L104N_Y	I/O, VREF Bank 6, L104N	I/O, VREF Bank 6, L104N_Y
I/O, L#P_Y	6	M5	XC2S100E, 150E, 300E, 400E	-	I/O, L74N_Y	I/O, L98N_Y	I/O, L103P	I/O, L103P_Y	I/O, L103P_Y	I/O, L103P
I/O, L#N_Y	6	M6	XC2S300E, 400E	-	-	-	I/O, L103N	I/O, L103N_Y	I/O, L103N_Y	I/O, L103N
I/O	6	N1	-	-	-	-	-	I/O	I/O	I/O
I/O	6	N2	-	-	I/O, L73P	I/O, L97P	I/O	I/O	I/O	I/O
I/O, VREF Bank 6, L#P	6	N3	XC2S200E, 400E	All	I/O, VREF Bank 6, L73N	I/O, VREF Bank 6, L97N	I/O, VREF Bank 6, L102P_Y	I/O, VREF Bank 6, L102P	I/O, VREF Bank 6, L102P_Y	I/O, VREF Bank 6, L102P
I/O, L#N	6	N4	XC2S100E, 150E, 200E, 400E	-	I/O, L72P_Y	I/O, L96P_Y	I/O, L102N_Y	I/O, L102N	I/O, L102N_Y	I/O, L102N
I/O, L#P_Y	6	N5	XC2S100E, 150E, 300E, 600E	-	I/O, L72N_Y	I/O, L96N_Y	I/O, L101P	I/O, L101P_Y	I/O, L101P	I/O, L101P_Y
I/O, L#N_Y	6	N6	XC2S300E, 600E	-	-	-	I/O, L101N	I/O, L101N_Y	I/O, L101N	I/O, L101N_Y
I/O, L#P_Y	6	P1	XC2S150E, 200E, 300E, 600E	-	-	I/O, L95P_Y	I/O, L100P_Y	I/O, L100P_Y	I/O, L100P	I/O, L100P_Y
I/O, L#N_Y	6	P2	XC2S100E, 150E, 200E, 300E, 600E	-	I/O, L71P_Y	I/O, L95N_Y	I/O, L100N_Y	I/O, L100N_Y	I/O, L100N	I/O, L100N_Y
I/O	6	R1	XC2S100E, 150E	-	I/O, L71N_Y	I/O, L94P_Y	I/O	I/O	I/O	I/O
I/O, L#P_Y	6	P3	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L94N_Y	I/O, L99P_Y	I/O, L99P_Y	I/O, L99P_Y	I/O, L99P_Y
I/O, L#N_Y	6	P4	XC2S200E, 300E, 400E, 600E	-	-	-	I/O, L99N_Y	I/O, L99N_Y	I/O, L99N_Y	I/O, L99N_Y
I/O, L#P_YY	6	P5	All	-	I/O, L70P_YY	I/O, L93P_YY	I/O, L98P_YY	I/O, L98P_YY	I/O, L98P_YY	I/O, L98P_YY
I/O, L#N_YY	6	P6	All	-	I/O, L70N_YY	I/O, L93N_YY	I/O, L98N_YY	I/O, L98N_YY	I/O, L98N_YY	I/O, L98N_YY

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O, L#P	2	L17	XC2S100E, 150E, 200E, 300E, 600E	XC2S400E, 600E	I/O, L29N_Y	I/O, L40N_Y	I/O, L43P_Y	I/O, L43P_Y	I/O, VREF Bank 2, L43P	I/O, VREF Bank 2, L43P_Y
I/O, L#N	2	K22	XC2S100E, 150E, 300E, 400E	-	I/O, L29P_Y	I/O, L40P_Y	I/O, L42N	I/O, L42N_Y	I/O, L42N_Y	I/O, L42N
I/O, L#P	2	K21	XC2S300E, 400E	-	-	-	I/O, L42P	I/O, L42P_Y	I/O, L42P_Y	I/O, L42P
I/O	2	K20	-	-	-	-	-	I/O	I/O	I/O
I/O (D3)	2	K19	-	-	I/O (D3)	I/O (D3), L39N	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)
I/O, VREF Bank 2, L#N	2	K18	XC2S100E, 200E, 400E	All	I/O, VREF Bank 2, L28N_Y	I/O, VREF Bank 2, L39P	I/O, VREF Bank 2, L41N_Y	I/O, VREF Bank 2, L41N	I/O, VREF Bank 2, L41N_Y	I/O, VREF Bank 2, L41N
I/O, L#P	2	K17	XC2S100, 150E, 200E, 400E	-	I/O, L28P_Y	I/O, L38N_Y	I/O, L41P_Y	I/O, L41P	I/O, L41P_Y	I/O, L41P
I/O, L#N	2	J22	XC2S150E, 300E, 600E	-	I/O	I/O, L38P_Y	I/O, L40N	I/O, L40N_Y	I/O, L40N	I/O, L40N_Y
I/O, L#P	2	J21	XC2S300E, 600E	-	-	-	I/O, L40P	I/O, L40P_Y	I/O, L40P	I/O, L40P_Y
I/O, L#N	2	J20	XC2S150E, 200E, 300E, 600E	-	-	I/O, L37N_Y	I/O, L39N_Y	I/O, L39N_Y	I/O, L39N	I/O, L39N_Y
I/O, L#P	2	J19	XC2S100E, 150E, 200E, 300E, 600E	-	I/O, L27N_Y	I/O, L37P_Y	I/O, L39P_Y	I/O, L39P_Y	I/O, L39P	I/O, L39P_Y
I/O	2	H22	XC2S100E, 150E	-	I/O, L27P_Y	I/O, L36N_Y	I/O	I/O	I/O	I/O
I/O, L#N	2	J18	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L36P_Y	I/O, L38N_Y	I/O, L38N_Y	I/O, L38N_Y	I/O, L38N_Y
I/O, L#P	2	J17	XC2S200E, 300E, 400E, 600E	-	-	-	I/O, L38P_Y	I/O, L38P_Y	I/O, L38P_Y	I/O, L38P_Y
I/O, L#N	2	H21	XC2S150E, 200E, 300E, 400E, 600E	-	I/O	I/O, L35N_Y	I/O, L37N_Y	I/O, L37N_Y	I/O, L37N_Y	I/O, L37N_Y
I/O (D2), L#P	2	H20	XC2S150E, 200E, 300E, 400E, 600E	-	I/O (D2)	I/O (D2), L35P_Y	I/O (D2), L37P_Y	I/O (D2), L37P_Y	I/O (D2), L37P_Y	I/O (D2), L37P_Y
I/O (D1), L#N	2	H19	XC2S300E, 400E, 600E	-	I/O (D1), L26N	I/O (D1), L34N	I/O (D1), L36N	I/O (D1), L36N_Y	I/O (D1), L36N_Y	I/O (D1), L36N_Y
I/O, VREF Bank 2, L#P	2	H18	XC2S300E, 400E, 600E	All	I/O, VREF Bank 2, L26P	I/O, VREF Bank 2, L34P	I/O, VREF Bank 2, L36P	I/O, VREF Bank 2, L36P_Y	I/O, VREF Bank 2, L36P_Y	I/O, VREF Bank 2, L36P_Y
I/O	2	G22	-	-	-	-	-	I/O	I/O	I/O
I/O	2	F22	-	-	I/O	I/O	I/O	I/O	I/O	I/O

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O (WRITE), L#N_YY	1	A20	All	-	I/O (WRITE), L20N_YY	I/O (WRITE), L26N_YY	I/O (WRITE), L28N_YY	I/O (WRITE), L28N_YY	I/O (WRITE), L28N_YY	I/O (WRITE), L28N_YY
I/O	1	D18	-	-	-	-	-	I/O	I/O	I/O
I/O	1	C18	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P	1	B19	XC2S200E, 300E, 400E, 600E	-	-	I/O, L25P	I/O, L27P_Y	I/O, L27P_Y	I/O, L27P_Y	I/O, L27P_Y
I/O, L#N	1	A19	XC2S200E, 300E, 400E, 600E	-	I/O	I/O, L25N	I/O, L27N_Y	I/O, L27N_Y	I/O, L27N_Y	I/O, L27N_Y
I/O, L#P	1	B18	XC2S100E, 200E, 300E, 400E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L19P_Y	I/O, L24P	I/O, VREF Bank 1, L26P_Y	I/O, VREF Bank 1, L26P_Y	I/O, VREF Bank 1, L26P_Y	I/O, VREF Bank 1, L26P_Y
I/O, L#N	1	A18	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L19N_Y	I/O, L24N	I/O, L26N_Y	I/O, L26N_Y	I/O, L26N_Y	I/O, L26N_Y
I/O	1	D17	-	-	-	-	-	I/O	I/O	I/O
I/O	1	C17	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P_YY	1	B17	All	-	I/O, L18P_YY	I/O, L23P_YY	I/O, L25P_YY	I/O, L25P_YY	I/O, L25P_YY	I/O, L25P_YY
I/O, L#N_YY	1	A17	All	-	I/O, L18N_YY	I/O, L23N_YY	I/O, L25N_YY	I/O, L25N_YY	I/O, L25N_YY	I/O, L25N_YY
I/O, VREF Bank 1, L#P_YY	1	E16	All	All	I/O, VREF Bank 1, L17P_YY	I/O, VREF Bank 1, L22P_YY	I/O, VREF Bank 1, L24P_YY	I/O, VREF Bank 1, L24P_YY	I/O, VREF Bank 1, L24P_YY	I/O, VREF Bank 1, L24P_YY
I/O, L#N_YY	1	E17	All	-	I/O, L17N_YY	I/O, L22N_YY	I/O, L24N_YY	I/O, L24N_YY	I/O, L24N_YY	I/O, L24N_YY
I/O	1	E15	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P	1	D16	XC2S300E, 600E	-	-	I/O, L21P	I/O, L23P	I/O, L23P_Y	I/O, L23P	I/O, L23P_Y
I/O, L#N	1	C16	XC2S300E, 600E	-	I/O	I/O, L21N	I/O, L23N	I/O, L23N_Y	I/O, L23N	I/O, L23N_Y
I/O, L#P	1	B16	XC2S100E, 300E, 600E	XC2S600E	I/O, L16P_Y	I/O, L20P	I/O, L22P	I/O, L22P_Y	I/O, L22P	I/O, VREF Bank 1, L22P_Y
I/O, L#N	1	A16	XC2S100E, 300E, 600E	-	I/O, L16N_Y	I/O, L20N	I/O, L22N	I/O, L22N_Y	I/O, L22N	I/O, L22N_Y
I/O	1	F14	-	-	-	-	-	I/O	I/O	I/O
I/O, VREF Bank 1, L#P	1	D15	XC2S100E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 1, L15P_Y	I/O, VREF Bank 1, L19P	I/O, VREF Bank 1, L21P_Y	I/O, VREF Bank 1, L21P_Y	I/O, VREF Bank 1, L21P_Y	I/O, VREF Bank 1, L21P_Y
I/O, L#N	1	C15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L15N_Y	I/O, L19N	I/O, L21N_Y	I/O, L21N_Y	I/O, L21N_Y	I/O, L21N_Y
I/O, L#P	1	B15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L14P_Y	I/O, L18P	I/O, L20P_Y	I/O, L20P_Y	I/O, L20P_Y	I/O, L20P_Y

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O, L#N	1	A15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L14N_Y	I/O, L18N	I/O, L20N_Y	I/O, L20N_Y	I/O, L20N_Y	I/O, L20N_Y
I/O	1	E14	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#P	1	D14	XC2S150E, 300E, 400E, 600E	-	-	I/O, L17P_Y	I/O, L19P	I/O, L19P_Y	I/O, L19P_Y	I/O, L19P_Y
I/O, L#N	1	C14	XC2S100E, 150E, 300E, 400E, 600E	-	I/O, L13P_Y	I/O, L17N_Y	I/O, L19N	I/O, L19N_Y	I/O, L19N_Y	I/O, L19N_Y
I/O, L#P	1	B14	XC2S100E, 150E, 300E, 400E, 600E	-	I/O, L13N_Y	I/O, L16P_Y	I/O, L18P	I/O, L18P_Y	I/O, L18P_Y	I/O, L18P_Y
I/O, L#N	1	A14	XC2S150E, 300E, 400E, 600E	-	-	I/O, L16N_Y	I/O, L18N	I/O, L18N_Y	I/O, L18N_Y	I/O, L18N_Y
I/O	1	E13	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#P	1	D13	XC2S200E, 300E, 400E, 600E	-	I/O, L12P	I/O, L15P	I/O, L17P_Y	I/O, L17P_Y	I/O, L17P_Y	I/O, L17P_Y
I/O, L#N	1	C13	XC2S200E, 300E, 400E, 600E	-	I/O, L12N	I/O, L15N	I/O, L17N_Y	I/O, L17N_Y	I/O, L17N_Y	I/O, L17N_Y
I/O, VREF Bank 1, L#P	1	B13	XC2S200E, 300E, 400E, 600E	All	I/O, VREF Bank 1, L11P	I/O, VREF Bank 1, L14P	I/O, VREF Bank 1, L16P_Y	I/O, VREF Bank 1, L16P_Y	I/O, VREF Bank 1, L16P_Y	I/O, VREF Bank 1, L16P_Y
I/O, L#N	1	A13	XC2S200E, 300E, 400E, 600E	-	I/O, L11N	I/O, L14N	I/O, L16N_Y	I/O, L16N_Y	I/O, L16N_Y	I/O, L16N_Y
I/O	1	F13	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P	1	C12	XC2S300E, 600E	-	-	-	I/O, L15P	I/O, L15P_Y	I/O, L15P	I/O, L15P_Y
I/O, L#N	1	B12	XC2S300E, 600E	-	I/O, L10P	I/O	I/O, L15N	I/O, L15N_Y	I/O, L15N	I/O, L15N_Y
I/O, L#P	1	D12	XC2S150E, 300E, 600E	XC2S400E, 600E	I/O, L10N	I/O, L13P_Y	I/O, L14P	I/O, L14P_Y	I/O, VREF Bank 1, L14P	I/O, VREF Bank 1, L14P_Y
I/O, L#N	1	E12	XC2S150E, 300E, 600E	-	-	I/O, L13N_Y	I/O, L14N	I/O, L14N_Y	I/O, L14N	I/O, L14N_Y
I/O	1	F12	-	-	-	-	-	I/O	I/O	I/O
I/O (DLL), L#P	1	A12	-	-	I/O (DLL), L9P	I/O (DLL), L12P	I/O (DLL), L13P	I/O (DLL), L13P	I/O (DLL), L13P	I/O (DLL), L13P
GCK2, I	1	A11	-	-	GCK2, I	GCK2, I	GCK2, I	GCK2, I	GCK2, I	GCK2, I
GCK3, I	0	C11	-	-	GCK3, I	GCK3, I	GCK3, I	GCK3, I	GCK3, I	GCK3, I
I/O (DLL), L#N	0	B11	-	-	I/O (DLL), L9N	I/O (DLL), L12N	I/O (DLL), L13N	I/O (DLL), L13N	I/O (DLL), L13N	I/O (DLL), L13N
I/O	0	D11	-	-	-	-	-	I/O	I/O	I/O

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L164N	6	W2	XC2S600E	XC2S600E	I/O, L164N	I/O, VREF Bank 6, L164N_Y
I/O, L163P	6	W5	XC2S400E	-	I/O, L163P_Y	I/O, L163P
I/O, L163N	6	W6	XC2S400E	-	I/O, L163N_Y	I/O, L163N
I/O	6	W7	-	-	I/O	I/O
I/O, L162P_YY	6	Y1	All	-	I/O, L162P_YY	I/O, L162P_YY
I/O, L162N_YY	6	Y2	All	-	I/O, L162N_YY	I/O, L162N_YY
I/O	6	Y3	-	-	-	I/O
I/O, L161P_YY	6	Y4	All	-	I/O, L161P_YY	I/O, L161P_YY
I/O, VREF Bank 6, L161N_YY	6	Y5	All	All	I/O, VREF Bank 6, L161N_YY	I/O, VREF Bank 6, L161N_YY
I/O	6	Y6	-	-	I/O	I/O
I/O, L160P_YY	6	AA1	All	-	I/O, L160P_YY	I/O, L160P_YY
I/O, L160N_YY	6	AA2	All	-	I/O, L160N_YY	I/O, L160N_YY
I/O, L159P	6	AA3	XC2S600E	-	I/O, L159P	I/O, L159P_Y
I/O, L159N	6	AA4	XC2S600E	-	I/O, L159N	I/O, L159N_Y
I/O	6	Y7	-	-	-	I/O
I/O, L158P	6	AA5	XC2S600E	-	I/O, L158P	I/O, L158P_Y
I/O, VREF Bank 6, L158N	6	AB5	XC2S600E	All	I/O, VREF Bank 6, L158N	I/O, VREF Bank 6, L158N_Y
I/O, L157P	6	AB1	XC2S400E	-	I/O, L157P_Y	I/O, L157P
I/O, L157N	6	AB2	XC2S400E	-	I/O, L157N_Y	I/O, L157N
I/O, L156P	6	AC1	XC2S600E	-	-	I/O, L156P_Y
I/O, L156N	6	AC2	XC2S600E	-	I/O	I/O, L156N_Y
I/O, L155P_YY	6	AC3	All	-	I/O, L155P_YY	I/O, L155P_YY
I/O, L155N_YY	6	AB4	All	-	I/O, L155N_YY	I/O, L155N_YY
I/O, L154P	6	AD1	-	-	-	I/O, L154P
I/O, L154N	6	AD2	-	-	-	I/O, L154N
I/O, L153P_YY	6	AE1	All	-	I/O, L153P_YY	I/O, L153P_YY
I/O, L153N_YY	6	AF2	All	-	I/O, L153N_YY	I/O, L153N_YY
M1	-	AE3	-	-	M1	M1
M0	-	AF3	-	-	M0	M0
M2	-	AD4	-	-	M2	M2

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O	3	N18	-	-	-	I/O
I/O (TRDY)	3	N24	-	-	I/O (TRDY)	I/O (TRDY)
I/O (IRDY), L75N_YY	2	N26	All	-	I/O (IRDY), L75N_YY	I/O (IRDY), L75N_YY
I/O, L75P_YY	2	N25	All	-	I/O, L75P_YY	I/O, L75P_YY
I/O	2	N19	-	-	-	I/O
I/O, L74N	2	N23	XC2S600E	-	-	I/O, L74N_Y
I/O, L74P	2	N22	XC2S600E	-	I/O	I/O, L74P_Y
I/O	2	M23	-	-	I/O	I/O
I/O, L73N	2	N21	XC2S600E	-	I/O, L73N	I/O, L73N_Y
I/O, VREF Bank 2, L73P	2	N20	XC2S600E	All	I/O, VREF Bank 2, L73P	I/O, VREF Bank 2, L73P_Y
I/O, L72N	2	M26	XC2S400E	-	I/O, L72N_Y	I/O, L72N
I/O, L72P	2	M25	XC2S400E	-	I/O, L72P_Y	I/O, L72P
I/O	2	M22	-	-	-	I/O
I/O, L71N_YY	2	M21	All	-	I/O, L71N_YY	I/O, L71N_YY
I/O, L71P_YY	2	M20	All	-	I/O, L71P_YY	I/O, L71P_YY
I/O	2	L26	-	-	-	I/O
I/O (D3), L70N_YY	2	M19	All	-	I/O (D3), L70N_YY	I/O (D3), L70N_YY
I/O, VREF Bank 2, L70P_YY	2	M18	All	All	I/O, VREF Bank 2, L70P_YY	I/O, VREF Bank 2, L70P_YY
I/O, L69N	2	L25	XC2S600E	-	I/O, L69N	I/O, L69N_Y
I/O, L69P	2	L24	XC2S600E	-	I/O, L69P	I/O, L69P_Y
I/O	2	L22	-	-	-	I/O
I/O, L68N	2	L21	XC2S600E	-	I/O, L68N	I/O, L68N_Y
I/O, L68P	2	L20	XC2S600E	-	I/O, L68P	I/O, L68P_Y
I/O	2	L19	-	-	-	I/O
I/O, L67N	2	K26	XC2S600E	-	I/O, L67N	I/O, L67N_Y
I/O, L67P	2	K25	XC2S600E	-	I/O, L67P	I/O, L67P_Y
I/O, L66N	2	K24	-	-	-	I/O, L66N
I/O, L66P	2	K23	-	-	I/O	I/O, L66P
I/O	2	K22	-	-	-	I/O
I/O, L65N	2	K20	XC2S600E	-	I/O	I/O, L65N_Y
I/O, L65P	2	K19	XC2S600E	-	I/O	I/O, L65P_Y
I/O	2	J26	-	-	I/O	I/O

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L51N	2	D24	-	-	-	I/O, L51N
I/O, L51P	2	C25	-	-	-	I/O, L51P
I/O (DIN, D0), L50N_YY	2	C26	All	-	I/O (DIN, D0), L50N_YY	I/O (DIN, D0), L50N_YY
I/O (DOUT, BUSY), L50P_YY	2	B26	All	-	I/O (DOUT, BUSY), L50P_YY	I/O (DOUT, BUSY), L50P_YY
CCLK	2	A25	-	-	CCLK	CCLK
TDO	2	C23	-	-	TDO	TDO
TDI	-	D22	-	-	TDI	TDI
I/O ($\overline{CS}$), L49P_YY	1	B24	All	-	I/O ($\overline{CS}$), L49P_YY	I/O ($\overline{CS}$), L49P_YY
I/O ($\overline{WRITE}$), L49N_YY	1	A24	All	-	I/O ($\overline{WRITE}$), L49N_YY	I/O ($\overline{WRITE}$), L49N_YY
I/O, L48P	1	B23	-	-	I/O	I/O, L48P
I/O, L48N	1	A23	-	-	-	I/O, L48N
I/O, L47P	1	B22	XC2S400E	-	I/O, L47P_Y	I/O, L47P
I/O, L47N	1	A22	XC2S400E	-	I/O, L47N_Y	I/O, L47N
I/O, L46P_YY	1	D21	All	-	I/O, L46P_YY	I/O, L46P_YY
I/O, L46N_YY	1	C21	All	-	I/O, L46N_YY	I/O, L46N_YY
I/O, VREF Bank 1, L45P_YY	1	B21	All	All	I/O, VREF Bank 1, L45P_YY	I/O, VREF Bank 1, L45P_YY
I/O, L45N_YY	1	A21	All	-	I/O, L45N_YY	I/O, L45N_YY
I/O, L44P	1	F20	XC2S600E	-	-	I/O, L44P_Y
I/O, L44N	1	E20	XC2S600E	-	I/O	I/O, L44N_Y
I/O, L43P_YY	1	D20	All	-	I/O, L43P_YY	I/O, L43P_YY
I/O, L43N_YY	1	C20	All	-	I/O, L43N_YY	I/O, L43N_YY
I/O, L42P_YY	1	B20	All	-	I/O, L42P_YY	I/O, L42P_YY
I/O, L42N_YY	1	A20	All	-	I/O, L42N_YY	I/O, L42N_YY
I/O, VREF Bank 1, L41P_YY	1	G19	All	All	I/O, VREF Bank 1, L41P_YY	I/O, VREF Bank 1, L41P_YY
I/O, L41N_YY	1	F19	All	-	I/O, L41N_YY	I/O, L41N_YY
I/O	1	E19	-	-	-	I/O
I/O, L40P_YY	1	B19	All	-	I/O, L40P_YY	I/O, L40P_YY
I/O, L40N_YY	1	A19	All	-	I/O, L40N_YY	I/O, L40N_YY
I/O	1	H18	-	-	I/O	I/O
I/O, L39P	1	G18	XC2S600E	-	I/O, L39P	I/O, L39P_Y