AMD Xilinx - XC2S100E-6TQ144C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	600
Number of Logic Elements/Cells	2700
Total RAM Bits	40960
Number of I/O	102
Number of Gates	100000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s100e-6tq144c

Optional pull-up and pull-down resistors and an optional weak-keeper circuit are attached to each user I/O pad. Prior to configuration all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but inputs may optionally be pulled up. The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins will float. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. After configuration, clamping diodes are connected to V_{CCO} for LVTTL, PCI, HSTL, SSTL, CTT, and AGP standards.

All Spartan-IIE FPGA IOBs support IEEE 1149.1-compatible boundary scan testing.

Input Path

A buffer in the IOB input path routes the input signal directly to internal logic and through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can used in close proximity to each other. See I/O Banking.

There are optional pull-up and pull-down resistors at each input for use after configuration.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. Each output buffer can source up to 24 mA and sink up to 48 mA. Drive strength and slew rate controls minimize bus transients. The default output driver is LVTTL with 12 mA drive strength and slow slew rate.

In most signaling standards, the output high voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See I/O Banking.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way helps eliminate bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signaling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks (see Figure 5). The pinout tables show the bank affiliation of each I/O (see Pinout Tables, page 53). Each bank has multiple V_{CCO} pins which must be connected to the same voltage. Voltage requirements are determined by the output standards in use.

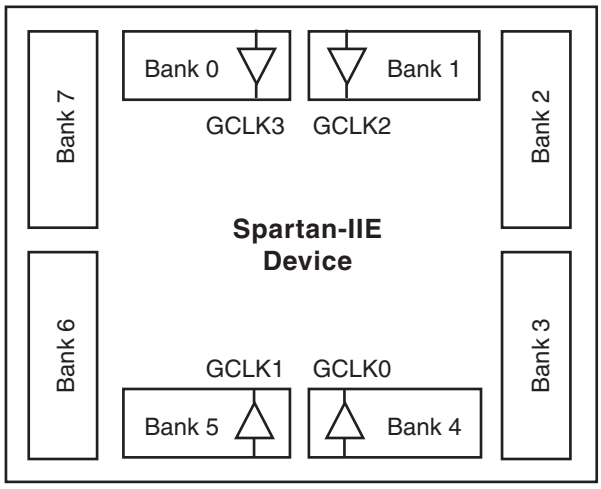


Figure 5: **Spartan-IIE I/O Banks**

In the TQ144 and PQ208 packages, the eight banks have V_{CCO} connected together. Thus, only one V_{CCO} level is allowed in these packages, although different V_{REF} values are allowed in each of the eight banks.

Within a bank, standards may be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 4. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO}. Note that V_{CCO}

Dedicated Routing

Some classes of signal require dedicated routing resources to maximize performance. In the Spartan-IIE FPGA architecture, dedicated routing resources are provided for two classes of signal.

- Horizontal routing resources are provided for on-chip 3-state busses. Four partitionable bus lines are provided per CLB row, permitting multiple busses within a row, as shown in Figure 10.
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.

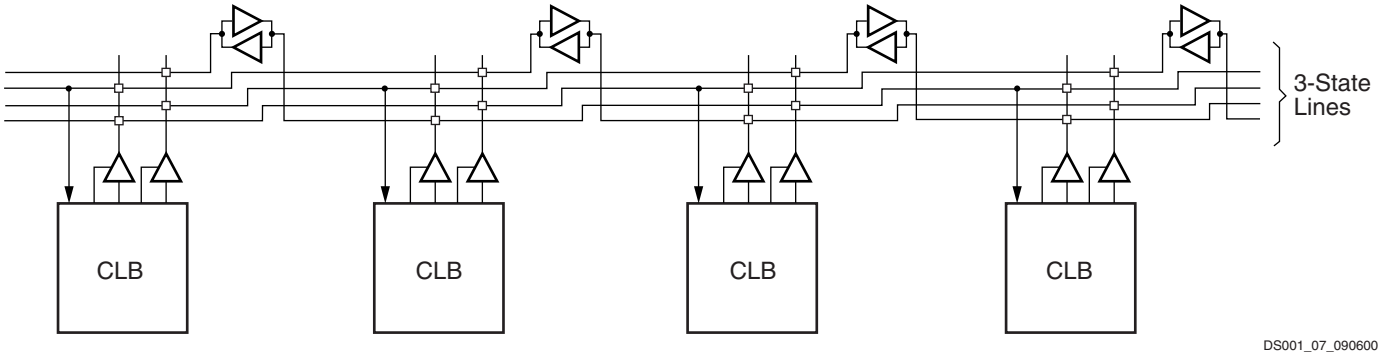


Figure 10: **BUFT Connections to Dedicated Horizontal Bus Lines**

Global Routing

Global Routing resources distribute clocks and other signals with very high fanout throughout the device. Spartan-IIE devices include two tiers of global routing resources referred to as primary and secondary global routing resources.

- The primary global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The primary global nets may only be driven by global buffers. There are four global buffers, one for each global net.
- The secondary global routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across the bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These secondary resources are more flexible than the primary resources since they are not restricted to routing only to clock pins.

Clock Distribution

The Spartan-IIE family provides high-speed, low-skew clock distribution through the primary global routing resources described above. A typical clock distribution net is shown in Figure 11.

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four primary global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing.

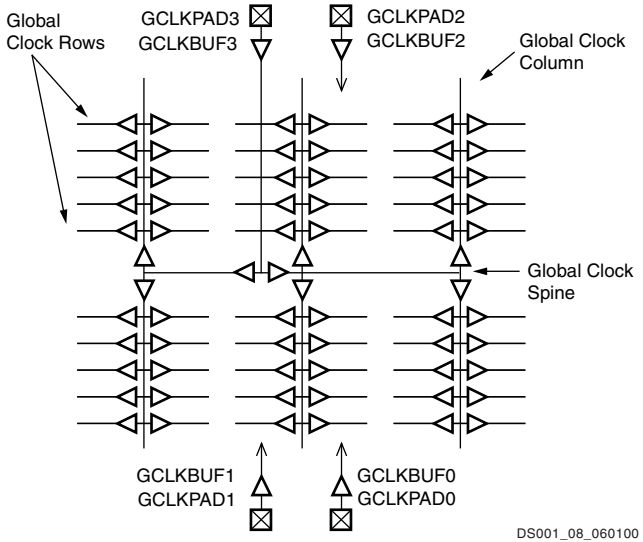


Figure 11: **Global Clock Distribution Network**

Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element (Figure 12). Additional delay is introduced such that clock edges reach internal flip-flops exactly one clock period after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock

Table 11: **Configuration Modes**

Configuration Mode	Preconfiguration Pull-ups	M0	M1	M2	CCLK Direction	Data Width	Serial D_{OUT}
Master Serial mode	No	0	0	0	Out	1	Yes
	Yes	0	0	1			
Slave Parallel mode (SelectMAP)	Yes	0	1	0	In	8	No
	No	0	1	1			
Boundary-Scan mode	Yes	1	0	0	N/A	1	No
	No	1	0	1			
Slave Serial mode	Yes	1	1	0	In	1	Yes
	No	1	1	1			

Notes:
1. During power-on and throughout configuration, the I/O drivers will be in a high-impedance state. After configuration, all unused I/Os (those not assigned signals) will remain in a high-impedance state. Pins used as outputs may pulse High at the end of configuration (see Answer 10504).
2. If the Mode pins are set for preconfiguration pull-ups, those resistors go into effect once the rising edge of INIT samples the Mode pins. They will stay in effect until GTS is released during startup, after which the UnusedPin bitstream generator option will determine whether the unused I/Os have a pull-up, pull-down, or no resistor.

Signals

There are two kinds of pins that are used to configure Spartan-IIE devices: Dedicated pins perform only specific configuration-related functions; the other pins can serve as general purpose I/Os once user operation has begun.

The dedicated pins comprise the mode pins (M2, M1, M0), the configuration clock pin (CCLK), the $\overline{\text{PROGRAM}}$ pin, the DONE pin and the boundary-scan pins (TDI, TDO, TMS, TCK). Depending on the selected configuration mode, CCLK may be an output generated by the FPGA, or may be generated externally, and provided to the FPGA as an input.

Note that some configuration pins can act as outputs. For correct operation, these pins require a V_{CCO} of 3.3V to drive an LVTTL signal or 2.5V to drive an LVCMOS signal. All the relevant pins fall in banks 2 or 3. The $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$ pins for Slave Parallel mode are located in bank 1.

For a more detailed description than that given below, see ***Module 1*** and XAPP176***,*** *Configuration and Readback of the Spartan-II and Spartan-IIE FPGA Families.*

The Process

The sequence of steps necessary to configure Spartan-IIE devices are shown in Figure 16. The overall flow can be divided into three different phases.

- Initiating configuration
- Configuration memory clear
- Loading data frames
- Start-up

The memory clearing and start-up phases are the same for all configuration modes; however, the steps for the loading of data frames are different. Thus, the details for data frame loading are described separately in the sections devoted to each mode.

Initiating Configuration

There are two different ways to initiate the configuration process: applying power to the device or asserting the $\overline{\text{PROGRAM}}$ input.

Configuration on power-up occurs automatically unless it is delayed by the user, as described in a separate section below. The waveform for configuration on power-up is shown in Configuration Switching Characteristics, page 48. Before configuration can begin, V_{CCO} Bank 2 must be greater than 1.0V. Furthermore, all V_{CCINT} power pins must be connected to a 1.8V supply. For more information on delaying configuration, see Clearing Configuration Memory, page 23.

Once in user operation, the device can be re-configured simply by pulling the $\overline{\text{PROGRAM}}$ pin Low. The device acknowledges the beginning of the configuration process by driving DONE Low, then enters the memory-clearing phase.

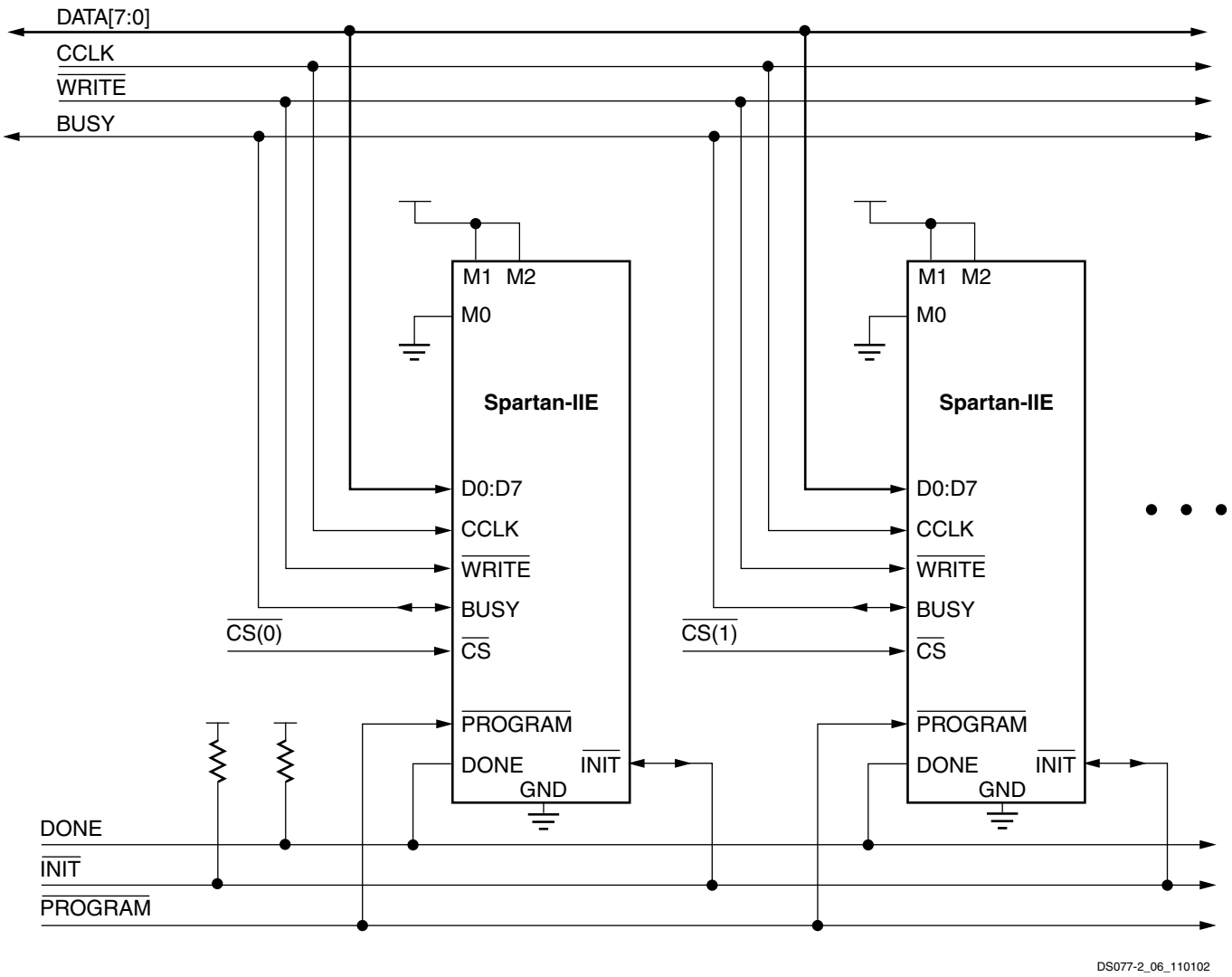


Figure 20: **Slave Parallel Configuration Circuit Diagram**

Multiple Spartan-IIE FPGAs can be configured using the Slave Parallel mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, $\overline{\text{WRITE}}$, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the $\overline{\text{CS}}$ pin of each device in turn and writing the appropriate data. Sync-to-DONE start-up timing is used to ensure that the start-up sequence does not begin until all the FPGAs have been loaded. See Start-up, page 23.

Write

When using the Slave Parallel Mode, write operations send packets of byte-wide configuration data into the FPGA. Figure 21, page 28 shows a flowchart of the write sequence used to load data into the Spartan-IIE FPGA. This is an expansion of the "Load Configuration Data Frames" block in Figure 16, page 23.

The timing for Slave Parallel mode is shown in Figure 26, page 50.

For the present example, the user holds $\overline{\text{WRITE}}$ and $\overline{\text{CS}}$ Low throughout the sequence of write operations. Note that when $\overline{\text{CS}}$ is asserted on successive CCLKs, $\overline{\text{WRITE}}$ must remain either asserted or deasserted. Otherwise an abort will be initiated, as in the next section.

1. Drive data onto D0-D7. Note that to avoid contention, the data source should not be enabled while $\overline{\text{CS}}$ is Low and $\overline{\text{WRITE}}$ is High. Similarly, while $\overline{\text{WRITE}}$ is High, no more than one device's $\overline{\text{CS}}$ should be asserted.
2. On the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this happens.
3. Repeat steps 1 and 2 until all the data has been sent.
4. Deassert $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$.

If CCLK is slower than F_{CCNH}, the FPGA will never assert BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

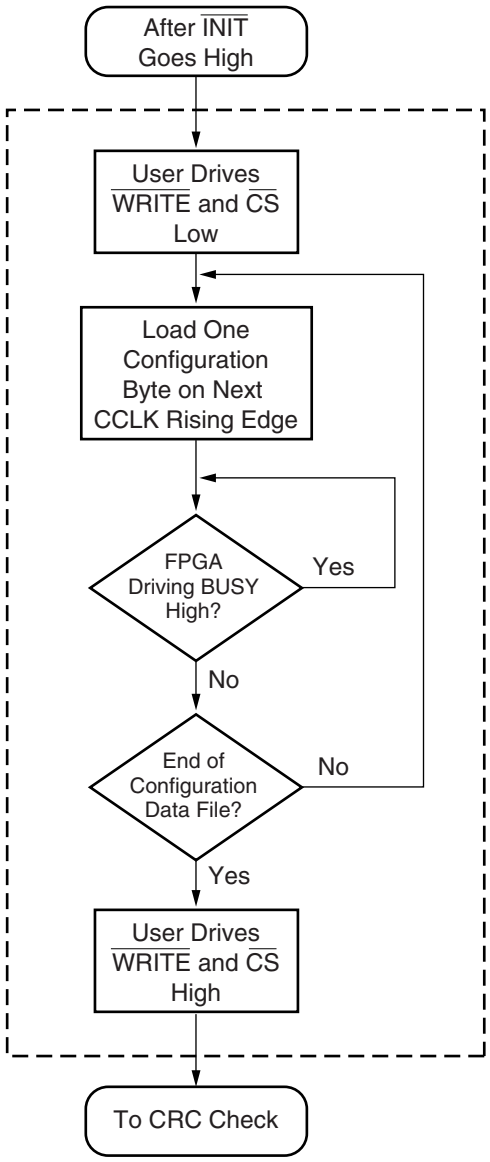


Figure 21: **Loading Configuration Data for the Slave Parallel Mode**

A configuration packet does not have to be written in one continuous stretch, rather it can be split into many write sequences. Each sequence would involve assertion of $\overline{CS}$.

In applications where multiple clock cycles may be required to access the configuration data before each byte can be loaded into the Slave Parallel interface, a new byte of data may not be ready for each consecutive CCLK edge. In such a case the $\overline{CS}$ signal may be deasserted until the next byte is valid on D0-D7. While $\overline{CS}$ is High, the Slave Parallel interface does not expect any data and ignores all CCLK transitions. However, to avoid aborting configuration, $\overline{WRITE}$ must continue to be asserted while $\overline{CS}$ is asserted during CCLK transitions.

Abort

To abort configuration during a write sequence, deassert $\overline{WRITE}$ while holding $\overline{CS}$ Low. The abort operation is initiated at the rising edge of CCLK. The device will remain BUSY until the aborted operation is complete. After aborting configuration, data is assumed to be unaligned to word boundaries and the FPGA requires a new synchronization word prior to accepting any new packets.

Boundary-Scan Configuration Mode

In the boundary-scan mode, no nondedicated pins are required, configuration being done entirely through the IEEE 1149.1 Test Access Port (TAP).

Configuration through the TAP uses the special CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port.

1. Load the CFG_IN instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a standard configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the JSTART instruction into IR
6. Enter the SDR state
7. Clock TCK (if selected) through the startup sequence (the length is programmable)
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode simply locks out the other modes. The boundary-scan mode is selected by a <10x> on the mode pins (M0, M1, M2). Note that the $\overline{PROGRAM}$ pin must be pulled High prior to reconfiguration. A Low on the $\overline{PROGRAM}$ pin resets the TAP controller and no boundary scan operations can be performed. See Xilinx Application Note XAPP188 for more information on boundary-scan configuration.

Readback

The configuration data stored in the Spartan-IIE FPGA configuration memory can be read back for verification. Along with the configuration data it is possible to read back the contents of all flip-flops/latches, LUT RAMs, and block RAMs. This capability is used for real-time debugging.

For more detailed information see Xilinx Application Note XAPP176, *Configuration and Readback of the Spartan-II and Spartan-IIE FPGA Families.*

Calculation of T_{IOOP} as a Function of Capacitance

T_{IOOP} is the propagation delay from the O Input of the IOB to the pad. The values for T_{IOOP} are based on the standard capacitive load (C_{SL}) for each I/O standard as listed in the table Constants for Calculating T_{IOOP}, below.

For other capacitive loads, use the formulas below to calculate an adjusted propagation delay, T_{IOOP1}.

$$T_{IOOP1} = T_{IOOP} + Adj + (C_{LOAD} - C_{SL}) * F_L$$

Where:

- Adj — is selected from IOB Output Delay Adjustments for Different Standards(1), page 40, according to the I/O standard used
- C_{LOAD} — is the capacitive load for the design
- F_L — is the capacitance scaling factor

Delay Measurement Methodology

Standard	V_L(1)	V_H(1)	Meas. Point	V_{REF} Typ(2)
LVTTL	0	3	1.4	-
LVCMOS2	0	2.5	1.125	-
PCI33_3	Per PCI Spec			-
PCI66_3	Per PCI Spec			-
GTL	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.80
GTL+	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.0
HSTL Class I	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL Class III	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL Class IV	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
SSTL3 I and II	V_{REF} – 1.0	V_{REF} + 1.0	V_{REF}	1.5
SSTL2 I and II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
CTT	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.5
AGP	V_{REF} – (0.2xV_{CCO})	V_{REF} + (0.2xV_{CCO})	V_{REF}	Per AGP Spec
LVDS	1.2 – 0.125	1.2 + 0.125	1.2	
LVPECL	1.6 – 0.3	1.6 + 0.3	1.6	

Notes:

1. Input waveform switches between V_L and V_H.
2. Measurements are made at V_{REF} Typ, Maximum, and Minimum. Worst-case values are reported.
3. I/O parameter measurements are made with the capacitance values shown in the following table, Constants for Calculating T_{IOOP}. Refer to Application Note XAPP179 for appropriate terminations.
4. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Constants for Calculating T_{IOOP}

Standard	C_{SL}(1) (pF)	F_L (ns/pF)
LVTTL Fast Slew Rate, 2 mA drive	35	0.41
LVTTL Fast Slew Rate, 4 mA drive	35	0.20
LVTTL Fast Slew Rate, 6 mA drive	35	0.13
LVTTL Fast Slew Rate, 8 mA drive	35	0.079
LVTTL Fast Slew Rate, 12 mA drive	35	0.044
LVTTL Fast Slew Rate, 16 mA drive	35	0.043
LVTTL Fast Slew Rate, 24 mA drive	35	0.033
LVTTL Slow Slew Rate, 2 mA drive	35	0.41
LVTTL Slow Slew Rate, 4 mA drive	35	0.20
LVTTL Slow Slew Rate, 6 mA drive	35	0.100
LVTTL Slow Slew Rate, 8 mA drive	35	0.086
LVTTL Slow Slew Rate, 12 mA drive	35	0.058
LVTTL Slow Slew Rate, 16 mA drive	35	0.050
LVTTL Slow Slew Rate, 24 mA drive	35	0.048
LVCMOS2	35	0.041
LVCMOS18	35	0.050
PCI 33 MHz 3.3V	10	0.050
PCI 66 MHz 3.3V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

Notes:

1. I/O parameter measurements are made with the capacitance values shown above. Refer to Application Note XAPP179 for appropriate terminations.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Clock Distribution Switching Characteristics

T_{GPIO} is specified for LVTTL levels. For other standards, adjust T_{GPIO} with the values shown in I/O Standard Global Clock Input Adjustments.

Symbol	Description	Speed Grade		Units
		-7	-6	
		Max	Max	
GCLK IOB and Buffer				
T_{GPIO}	Global clock pad to output	0.7	0.7	ns
T_{GIO}	Global clock buffer I input to O output	0.45	0.5	ns

I/O Standard Global Clock Input Adjustments

Delays associated with a global clock input pad are specified for LVTTL levels. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade		Units
			-7	-6	
Data Input Delay Adjustments					
$T_{GPLVTTL}$	Standard-specific global clock input delay adjustments	LVTTL	0	0	ns
$T_{GPLVCMOS2}$		LVCMOS2	0	0	ns
$T_{GPLVCMOS18}$		LVCMOS18	0.2	0.2	ns
$T_{GPLVCDS}$		LVDS	0.38	0.38	ns
$T_{GPLVPECL}$		LVCPECL	0.38	0.38	ns
$T_{GPPCI33\_3}$		PCI, 33 MHz, 3.3V	0.08	0.08	ns
$T_{GPPCI66\_3}$		PCI, 66 MHz, 3.3V	–0.11	–0.11	ns
T_{GPGTL}		GTL	0.37	0.37	ns
T_{GPGTLP}		GTL+	0.37	0.37	ns
T_{GPHSTL}		HSTL	0.27	0.27	ns
$T_{GPSSTL2}$		SSTL2	0.27	0.27	ns
$T_{GPSSTL3}$		SSTL3	0.27	0.27	ns
T_{GPCTT}		CTT	0.33	0.33	ns
T_{GPAGP}		AGP	0.27	0.27	ns

Notes:
1. Input timing for GPLVTTL is measured at 1.4V. For other I/O standards, see the table Delay Measurement Methodology, page 41.

DLL Timing Parameters

Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Symbol	Description	F_{CLKIN}	Speed Grade				Units
			-7		-6		
			Min	Max	Min	Max	
$F_{CLKINHF}$	Input clock frequency (CLKDLLHF)	-	60	320	60	275	MHz
$F_{CLKINLF}$	Input clock frequency (CLKDLL)	-	25	160	25	135	MHz
T_{DLLPW}	Input clock pulse width	≥25 MHz	5.0	-	5.0	-	ns
		≥50 MHz	3.0	-	3.0	-	ns
		≥100 MHz	2.4	-	2.4	-	ns
		≥150 MHz	2.0	-	2.0	-	ns
		≥200 MHz	1.8	-	1.8	-	ns
		≥250 MHz	1.5	-	1.5	-	ns
		≥300 MHz	1.3	-	NA	-	

DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications were determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers. Figure 22, page 44, provides definitions for various parameters in the table below.

Symbol	Description	F_{CLKIN}	CLKDLLHF		CLKDLL		Units
			Min	Max	Min	Max	
T_{IPTOL}	Input clock period tolerance		-	1.0	-	1.0	ns
T_{IJITCC}	Input clock jitter tolerance (cycle-to-cycle)		-	±150	-	±300	ps
T_{LOCK}	Time required for DLL to acquire lock(1)	> 60 MHz	-	20	-	20	µs
		50-60 MHz	-	-	-	25	µs
		40-50 MHz	-	-	-	50	µs
		30-40 MHz	-	-	-	90	µs
		25-30 MHz	-	-	-	120	µs
T_{OJITCC}	Output jitter (cycle-to-cycle) for any DLL clock output(2)		-	±60	-	±60	ps
T_{PHIO}	Phase offset between CLKIN and CLKO(3)		-	±100	-	±100	ps
T_{PHOO}	Phase offset between clock outputs on the DLL(4)		-	±140	-	±140	ps
T_{PHIOM}	Phase difference between CLKIN and CLKO(5)		-	±160	-	±160	ps
T_{PHOOM}	Phase difference between clock outputs on the DLL(6)		-	±200	-	±200	ps

Notes:

1. Commercial operating conditions. Add 30% for Industrial operating conditions.
2. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
3. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* output jitter and input clock jitter.
4. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* output jitter and input clock jitter.
5. **Maximum Phase Difference between CLKIN and CLKO** is the sum of output jitter and phase offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
6. **Maximum Phase Difference between Clock Outputs on the DLL** is the sum of output jitter and phase offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).

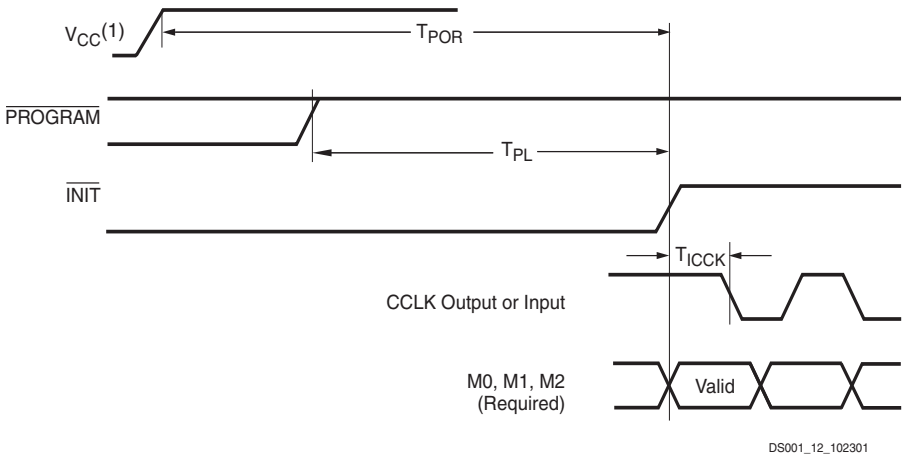
TBUF Switching Characteristics

Symbol	Description	Speed Grade		Units
		-7	-6	
		Max	Max	
T_{IO}	IN input to OUT output	0	0	ns
T_{OFF}	TRI input to OUT output high impedance	0.1	0.11	ns
T_{ON}	TRI input to valid data on OUT output	0.1	0.11	ns

JTAG Test Access Port Switching Characteristics

Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Setup/Hold Times with Respect to TCK						
T_{TAPTCK} / T_{TCKTAP}	TMS and TDI setup times and hold times	4.0 / 2.0	-	4.0 / 2.0	-	ns
Sequential Delays						
T_{TCKTDO}	Output delay from clock TCK to output TDO	-	11.0	-	11.0	ns
FTCK	TCK clock frequency	-	33	-	33	MHz

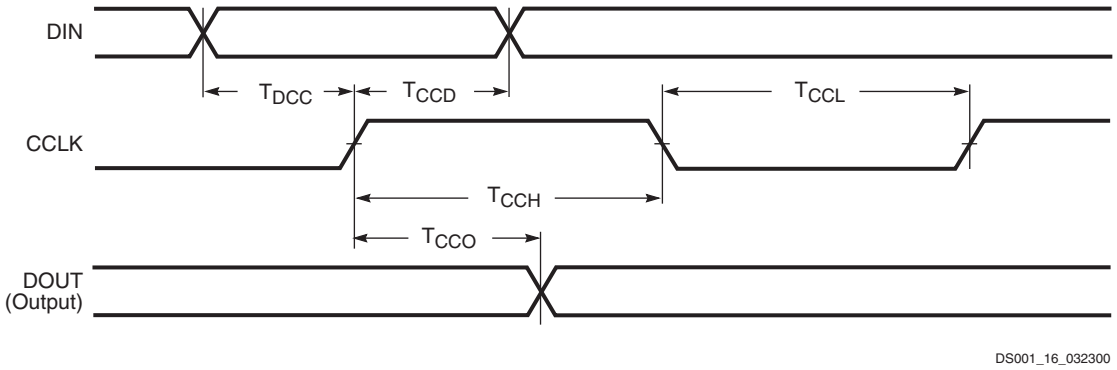
Configuration Switching Characteristics



Symbol	Description	All Devices		Units
		Min	Max	
T_{POR}	Power-on reset	-	2	ms
T_{PL}	Program latency	-	100	µs
T_{ICCK}	CCLK output delay (Master serial mode only)	0.5	4	µs
$T_{PROGRAM}$	Program pulse width	300	-	ns

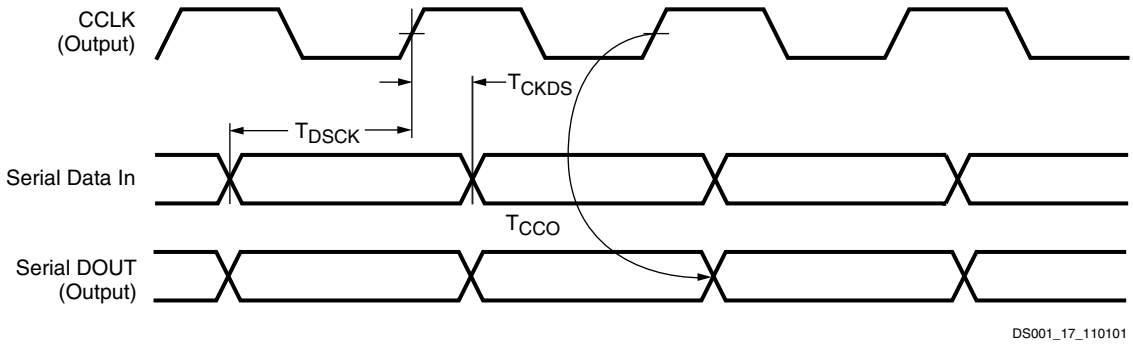
Notes:
1. Before configuration can begin, V_{CCINT} and V_{CCO} Bank 2 must reach the recommended operating voltage.

Figure 23: **Configuration Timing on Power-Up**



Symbol		Description	All Devices		Units
			Min	Max	
T_{DCC} / T_{CCD}	CCLK	DIN setup/hold	5 / 0	-	ns
T_{CCO}		DOUT	-	12	ns
T_{CCH}		High time	5	-	ns
T_{CCL}		Low time	5	-	ns
F_{CC}		Maximum frequency	-	66	MHz

Figure 24: **Slave Serial Mode Timing**



Symbol		Description	All Devices		Units
			Min	Max	
T_{DSCK} / T_{CKDS}	CCLK	DIN setup/hold	5 / 0	-	ns
T_{CCO}		DOUT	-	12	ns
F_{CC}		Frequency tolerance with respect to nominal	–30%	+45%	-

Figure 25: **Master Serial Mode Timing**

Revision History

Date	Version	Description
11/15/2001	1.0	Initial Xilinx release.
06/28/2002	1.1	Added -7 speed grade and extended DLL specs to Industrial.
11/18/2002	2.0	Added XC2S400E and XC2S600E. Added minimum specifications. Added reference to XAPP450 for Power-On Requirements. Removed Preliminary designation.
07/09/2003	2.1	Added I_{CCINTQ} typical values. Reduced ICCPO power-on current requirements. Relaxed TCCPO power-on ramp requirements. Added IHSPO to describe current in hot-swap applications. Updated TPSFD / TPHFD description to indicate use of delay element.
06/18/2008	2.3	Updated I/O measurement thresholds. Updated all modules for continuous page, figure, and table numbering. Updated links. Synchronized all modules to v2.3.
08/09/2013	3.0	This product is obsolete/discontinued per XCN12026.

In the PQ208 package, all VCCO pins must be connected to the same voltage.

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
GND	-	P1	-	-
TMS	-	P2	-	-
I/O	7	P3	-	-
I/O	7	P4	-	XC2S200E, 300E
I/O	7	P5	-	-
I/O, VREF Bank 7, L49P	7	P6	XC2S50E, 150E, 200E, 300E	All
I/O, L49N	7	P7	XC2S50E, 150E, 200E, 300E	-
I/O	7	P8	-	-
I/O	7	P9	-	-
I/O, L48P	7	P10	XC2S50E, 300E	XC2S100E, 150E, 200E, 300E
I/O, L48N	7	P11	XC2S50E, 300E	-
GND	-	P12	-	-
VCCO	-	P13	-	-
VCCINT	-	P14	-	-
I/O, L47P_YY	7	P15	All	-
I/O, L47N_YY	7	P16	All	-
I/O, L46P_YY	7	P17	All	-
I/O, L46N_YY	7	P18	All	-
GND	-	P19	-	-
I/O, VREF Bank 7, L45P	7	P20	XC2S50E, 300E	All
I/O, L45N	7	P21	XC2S50E, 300E	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O	7	P22	-	-
I/O, L44P_YY	7	P23	All	-
I/O (IRDY), L44N_YY	7	P24	All	-
GND	-	P25	-	-
VCCO	-	P26	-	-
I/O (TRDY)	6	P27	-	-
VCCINT	-	P28	-	-
I/O	6	P29	-	-
I/O, L43P	6	P30	XC2S50E, 300E	-
I/O, VREF Bank 6, L43N	6	P31	XC2S50E, 300E	All
GND	-	P32	-	-
I/O, L42P_YY	6	P33	All	-
I/O, L42N_YY	6	P34	All	-
I/O, L41P_YY	6	P35	All	-
I/O, L41N_YY	6	P36	All	-
VCCINT	-	P37	-	-
VCCO	-	P38	-	-
GND	-	P39	-	-
I/O, L40P	6	P40	XC2S50E, 300E	-
I/O, L40N	6	P41	XC2S50E, 300E	XC2S100E, 150E, 200E, 300E
I/O	6	P42	-	-
I/O	6	P43	-	-
I/O	6	P44	-	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L20P	2	D14	XC2S100E, 200E, 300E	XC2S200E, 300E, 400E
I/O (DIN, D0), L19N_YY	2	B16	All	-
I/O (DOUT, BUSY), L19P_YY	2	C15	All	-
CCLK	2	A15	-	-
TDO	2	B14	-	-
TDI	-	C13	-	-
I/O ($\overline{CS}$), L18P_YY	1	A14	All	-
I/O ($\overline{WRITE}$), L18N_YY	1	A13	All	-
I/O, L17P	1	B13	XC2S50E, 100E, 200E, 300E, 400E	XC2S200E, 300E, 400E
I/O, L17N	1	C12	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L16P_YY	1	B12	All	-
I/O, L16N_YY	1	A12	All	-
I/O, VREF Bank 1, L15P_YY	1	D12	All	All
I/O, L15N_YY	1	E11	All	-
I/O, L14P	1	D11	XC2S50E, 100E, 150E, 300E	-
I/O, L14N	1	C11	XC2S50E, 100E, 150E, 300E	-
I/O, L13P	1	B11	XC2S50E, 100E, 200E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L13N	1	A11	XC2S50E, 100E, 200E, 300E, 400E	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L12P	1	E10	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L12N	1	D10	XC2S50E, 100E, 200E, 300E, 400E	-
I/O	1	C10	-	-
I/O, L11P	1	B10	XC2S50E, 200E, 300E, 400E	-
I/O, L11N	1	A10	XC2S50E, 200E, 300E, 400E	-
I/O, VREF Bank 1, L10P	1	D9	XC2S50E, 200E, 300E, 400E	All
I/O, L10N	1	C9	XC2S50E, 200E, 300E, 400E	-
I/O, L9P	1	B9	XC2S50E, 150E, 200E, 400E	-
I/O, L9N	1	A9	XC2S50E, 150E, 200E, 400E	XC2S400E
I/O (DLL), L8P	1	A8	-	-
GCK2, I	1	B8	-	-
GCK3, I	0	C8	-	-
I/O (DLL), L8N	0	D8	-	-
I/O	0	A7	-	XC2S400E
I/O, L7P	0	E7	XC2S50E, 200E, 300E, 400E	-
I/O, VREF Bank 0, L7N	0	D7	XC2S50E, 200E, 300E, 400E	All

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
TMS	-	E4	-	-	TMS	TMS	TMS	TMS	TMS	TMS
I/O	7	D3	XC2S150E	-	I/O	I/O, L113P_Y	I/O	I/O	I/O	I/O
I/O	7	C2	-	-	-	-	-	I/O	I/O	I/O
I/O	7	C1	XC2S150E	-	-	I/O, L113N_Y	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	D2	XC2S150E, 200E, 300E, 400E	-	-	I/O, L112P_Y	I/O, L119P_Y	I/O, L119P_Y	I/O, L119P_Y	I/O, L119P
I/O, L#N_Y	7	D1	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L112N_Y	I/O, L119N_Y	I/O, L119N_Y	I/O, L119N_Y	I/O, L119N
I/O, L#P_Y	7	E2	XC2S100E, 200E, 300E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L85P_Y	I/O, L111P	I/O, VREF Bank 7, L118P_Y	I/O, VREF Bank 7, L118P_Y	I/O, VREF Bank 7, L118P	I/O, VREF Bank 7, L118P_Y
I/O, L#N_Y	7	E3	XC2S100E, 200E, 300E, 600E	-	I/O, L85N_Y	I/O, L111N	I/O, L118N_Y	I/O, L118N_Y	I/O, L118N	I/O, L118N_Y
I/O	7	E1	-	-	-	-	-	I/O	I/O	I/O
I/O	7	F5	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	F4	XC2S100E, 200E, 300E, 600E	-	I/O, L84P_Y	I/O, L110P	I/O, L117P_Y	I/O, L117P_Y	I/O, L117P	I/O, L117P_Y
I/O, L#N_Y	7	F3	XC2S100E, 200E, 300E, 600E	-	I/O, L84N_Y	I/O, L110N	I/O, L117N_Y	I/O, L117N_Y	I/O, L117N	I/O, L117N_Y
I/O, VREF Bank 7, L#P_Y	7	F2	XC2S150E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 7, L83P	I/O, VREF Bank 7, L109P_Y	I/O, VREF Bank 7, L116P_Y	I/O, VREF Bank 7, L116P_Y	I/O, VREF Bank 7, L116P_Y	I/O, VREF Bank 7, L116P_Y
I/O, L#N_Y	7	F1	XC2S150E, 200E, 300E, 400E, 600E	-	I/O, L83N	I/O, L109N_Y	I/O, L116N_Y	I/O, L116N_Y	I/O, L116N_Y	I/O, L116N_Y
I/O	7	G5	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	G4	XC2S150E, 200E, 300E, 400E	-	-	I/O, L108P_Y	I/O, L115P_Y	I/O, L115P_Y	I/O, L115P_Y	I/O, L115P
I/O, L#N_Y	7	G3	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L108N_Y	I/O, L115N_Y	I/O, L115N_Y	I/O, L115N_Y	I/O, L115N
I/O, L#P_Y	7	G2	XC2S100E, 150E, 300E, 600E	XC2S600E	I/O, L82P_Y	I/O, L107P_Y	I/O, L114P	I/O, L114P_Y	I/O, L114P	I/O, VREF Bank 7, L114P_Y
I/O, L#N_Y	7	G1	XC2S100E, 150E, 300E, 600E	-	I/O, L82N_Y	I/O, L107N_Y	I/O, L114N	I/O, L114N_Y	I/O, L114N	I/O, L114N_Y

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L201P	7	E4	XC2S400E	-	I/O, L201P_Y	I/O, L201P
I/O, L201N	7	F5	XC2S400E	-	I/O, L201N_Y	I/O, L201N
I/O, VREF Bank 7, L200P	7	F4	XC2S600E	All	I/O, VREF Bank 7, L200P	I/O, VREF Bank 7, L200P_Y
I/O, L200N	7	F3	XC2S600E	-	I/O, L200N	I/O, L200N_Y
I/O, L199P	7	F2	XC2S600E	-	-	I/O, L199P_Y
I/O, L199N	7	F1	XC2S600E	-	I/O	I/O, L199N_Y
I/O, L198P	7	G6	XC2S400E	-	I/O, L198P_Y	I/O, L198P
I/O, L198N	7	G5	XC2S400E	-	I/O, L198N_Y	I/O, L198N
I/O, L197P	7	G4	XC2S600E	-	I/O, L197P	I/O, L197P_Y
I/O, L197N	7	G3	XC2S600E	-	I/O, L197N	I/O, L197N_Y
I/O, VREF Bank 7, L196P_YY	7	G2	All	All	I/O, VREF Bank 7, L196P_YY	I/O, VREF Bank 7, L196P_YY
I/O, L196N_YY	7	G1	All	-	I/O, L196N_YY	I/O, L196N_YY
I/O	7	H7	-	-	I/O	I/O
I/O, L195P_YY	7	H6	All	-	I/O, L195P_YY	I/O, L195P_YY
I/O, L195N_YY	7	H5	All	-	I/O, L195N_YY	I/O, L195N_YY
I/O	7	J8	-	-	-	I/O
I/O, L194P	7	H2	XC2S400E	-	I/O, L194P_Y	I/O, L194P
I/O, L194N	7	H1	XC2S400E	-	I/O, L194N_Y	I/O, L194N
I/O, L193P	7	J7	XC2S600E	XC2S600E	I/O	I/O, VREF Bank 7, L193P_Y
I/O, L193N	7	J6	XC2S600E	-	-	I/O, L193N_Y
I/O	7	J5	-	-	I/O	I/O
I/O, L192P_YY	7	J4	All	-	I/O, L192P_YY	I/O, L192P_YY
I/O, L192N_YY	7	J3	All	-	I/O, L192N_YY	I/O, L192N_YY
I/O	7	K5	-	-	I/O	I/O
I/O, VREF Bank 7, L191P_YY	7	J2	All	All	I/O, VREF Bank 7, L191P_YY	I/O, VREF Bank 7, L191P_YY
I/O, L191N_YY	7	J1	All	-	I/O, L191N_YY	I/O, L191N_YY
I/O, L190P_YY	7	K8	All	-	I/O, L190P_YY	I/O, L190P_YY
I/O, L190N_YY	7	K7	All	-	I/O, L190N_YY	I/O, L190N_YY
I/O	7	K4	-	-	-	I/O
I/O, L189P_YY	7	K3	All	-	I/O, L189P_YY	I/O, L189P_YY
I/O, L189N_YY	7	K2	All	-	I/O, L189N_YY	I/O, L189N_YY
I/O	7	K1	-	-	-	I/O

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L188P	7	L8	XC2S400E	-	I/O, L188P_Y	I/O, L188P
I/O, L188N	7	L7	XC2S400E	-	I/O, L188N_Y	I/O, L188N
I/O, L187P	7	L6	XC2S600E	-	I/O, L187P	I/O, L187P_Y
I/O, L187N	7	L5	XC2S600E	-	I/O, L187N	I/O, L187N_Y
I/O	7	L3	-	-	-	I/O
I/O, L186P	7	L2	XC2S600E	-	I/O, L186P	I/O, L186P_Y
I/O, L186N	7	L1	XC2S600E	-	I/O, L186N	I/O, L186N_Y
I/O	7	M9	-	-	-	I/O
I/O, L185P	7	M8	XC2S600E	-	I/O, L185P	I/O, L185P_Y
I/O, L185N	7	M7	XC2S600E	-	I/O, L185N	I/O, L185N_Y
I/O, VREF Bank 7, L184P_YY	7	M6	All	All	I/O, VREF Bank 7, L184P_YY	I/O, VREF Bank 7, L184P_YY
I/O, L184N_YY	7	M5	All	-	I/O, L184N_YY	I/O, L184N_YY
I/O	7	M4	-	-	-	I/O
I/O, L183P_YY	7	M2	All	-	I/O, L183P_YY	I/O, L183P_YY
I/O, L183N_YY	7	M1	All	-	I/O, L183N_YY	I/O, L183N_YY
I/O	7	N9	-	-	-	I/O
I/O, L182P	7	N8	XC2S400E	-	I/O, L182P_Y	I/O, L182P
I/O, L182N	7	N7	XC2S400E	-	I/O, L182N_Y	I/O, L182N
I/O, VREF Bank 7, L181P	7	N6	XC2S600E	All	I/O, VREF Bank 7, L181P	I/O, VREF Bank 7, L181P_Y
I/O, L181N	7	N5	XC2S600E	-	I/O, L181N	I/O, L181N_Y
I/O	7	N4	-	-	-	I/O
I/O, L180P_YY	7	N3	All	-	I/O, L180P_YY	I/O, L180P_YY
I/O, L180N_YY	7	N2	All	-	I/O, L180N_YY	I/O, L180N_YY
I/O	7	N1	-	-	-	I/O
I/O, L179P_YY	7	P1	All	-	I/O, L179P_YY	I/O, L179P_YY
I/O (IRDY), L179N_YY	7	P2	All	-	I/O (IRDY), L179N_YY	I/O (IRDY), L179N_YY
I/O (TRDY), L178P	6	P3	XC2S600E	-	I/O (TRDY)	I/O (TRDY), L178P_Y
I/O, L178N	6	P4	XC2S600E	-	-	I/O, L178N_Y
I/O, L177P	6	P5	XC2S600E	-	-	I/O, L177P_Y
I/O, L177N	6	P6	XC2S600E	-	I/O	I/O, L177N_Y
I/O	6	P7	-	-	I/O	I/O
I/O, L176P	6	P8	XC2S600E	-	I/O, L176P	I/O, L176P_Y

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
DONE	3	AE26	-	-	DONE	DONE
$\overline{\text{PROGRAM}}$	-	AC24	-	-	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$
I/O ($\overline{\text{INIT}}$), L101N_YY	3	AD25	All	-	I/O ($\overline{\text{INIT}}$), L101N_YY	I/O ($\overline{\text{INIT}}$), L101N_YY
I/O (D7), L101P_YY	3	AD26	All	-	I/O (D7), L101P_YY	I/O (D7), L101P_YY
I/O, L100N	3	AC25	-	-	-	I/O, L100N
I/O, L100P	3	AC26	-	-	-	I/O, L100P
I/O, L99N	3	AB22	XC2S600E	-	-	I/O, L99N_Y
I/O, L99P	3	AB23	XC2S600E	-	I/O	I/O, L99P_Y
I/O, L98N_YY	3	AB25	All	-	I/O, L98N_YY	I/O, L98N_YY
I/O, L98P_YY	3	AB26	All	-	I/O, L98P_YY	I/O, L98P_YY
I/O, L97N	3	AA23	-	-	I/O, L97N_Y	I/O, L97N
I/O, L97P	3	AA24	-	-	I/O, L97P_Y	I/O, L97P
I/O, VREF Bank 3, L96N	3	AA25	XC2S600E	All	I/O, VREF Bank 3, L96N	I/O, VREF Bank 3, L96N_Y
I/O, L96P	3	AA26	XC2S600E	-	I/O, L96P	I/O, L96P_Y
I/O, L95N	3	AA22	XC2S600E	-	-	I/O, L95N_Y
I/O, L95P	3	Y22	XC2S600E	-	I/O	I/O, L95P_Y
I/O, L94N	3	Y23	XC2S400E	-	I/O, L94N_Y	I/O, L94N
I/O, L94P	3	Y24	XC2S400E	-	I/O, L94P_Y	I/O, L94P
I/O, L93N	3	Y25	XC2S600E	-	I/O, L93N	I/O, L93N_Y
I/O, L93P	3	Y26	XC2S600E	-	I/O, L93P	I/O, L93P_Y
I/O, VREF Bank 3, L92N_YY	3	W21	All	All	I/O, VREF Bank 3, L92N_YY	I/O, VREF Bank 3, L92N_YY
I/O, L92P_YY	3	W22	All	-	I/O, L92P_YY	I/O, L92P_YY
I/O	3	Y21	-	-	-	I/O
I/O, L91N_YY	3	W25	All	-	I/O, L91N_YY	I/O, L91N_YY
I/O, L91P_YY	3	W26	All	-	I/O, L91P_YY	I/O, L91P_YY
I/O	3	W20	-	-	I/O	I/O
I/O, L90N	3	V19	XC2S400E	-	I/O, L90N_Y	I/O, L90N
I/O, L90P	3	V20	XC2S400E	-	I/O, L90P_Y	I/O, L90P
I/O, L89N	3	V21	XC2S600E	XC2S600E	-	I/O, VREF Bank 3, L89N_Y
I/O, L89P	3	V22	XC2S600E	-	I/O	I/O, L89P_Y
I/O	3	V23	-	-	I/O	I/O
I/O, L88N_YY	3	V24	All	-	I/O, L88N_YY	I/O, L88N_YY

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, VREF Bank 1, L25P	1	D14	XC2S600E	All	I/O, VREF Bank 1, L25P	I/O, VREF Bank 1, L25P_Y
I/O, L25N	1	C14	XC2S600E	-	I/O, L25N	I/O, L25N_Y
I/O	1	J13	-	-	-	I/O
I/O, L24P	1	C13	-	-	I/O, L24P	I/O, L24P
I/O, L24N	1	D13	-	-	I/O, L24N	I/O, L24N
I/O	1	H13	-	-	-	I/O
I/O (DLL), L23P	1	B14	-	-	I/O (DLL), L23P	I/O (DLL), L23P
GCK2, I	1	A14	-	-	GCK2, I	GCK2, I
GCK3, I	0	A13	-	-	GCK3, I	GCK3, I
I/O (DLL), L23N	0	B13	-	-	I/O (DLL), L23N	I/O (DLL), L23N
I/O	0	E13	-	-	-	I/O
I/O, L22P_YY	0	F13	All	-	I/O, L22P_YY	I/O, L22P_YY
I/O, L22N_YY	0	G13	All	-	I/O, L22N_YY	I/O, L22N_YY
I/O, L21P	0	A12	XC2S600E	-	-	I/O, L21P_Y
I/O, VREF Bank 0, L21N	0	B12	XC2S600E	All	I/O, VREF Bank 0	I/O, VREF Bank 0, L21N_Y
I/O, L20P	0	D12	XC2S600E	-	I/O, L20P	I/O, L20P_Y
I/O, L20N	0	E12	XC2S600E	-	I/O, L20N	I/O, L20N_Y
I/O	0	F12	-	-	-	I/O
I/O, L19P_YY	0	G12	All	-	I/O, L19P_YY	I/O, L19P_YY
I/O, L19N_YY	0	H12	All	-	I/O, L19N_YY	I/O, L19N_YY
I/O	0	J12	-	-	-	I/O
I/O, L18P_YY	0	A11	All	-	I/O, L18P_YY	I/O, L18P_YY
I/O, VREF Bank 0, L18N_YY	0	B11	All	All	I/O, VREF Bank 0, L18N_YY	I/O, VREF Bank 0, L18N_YY
I/O, L17P_YY	0	E11	All	-	I/O, L17P_YY	I/O, L17P_YY
I/O, L17N_YY	0	F11	All	-	I/O, L17N_YY	I/O, L17N_YY
I/O	0	C11	-	-	-	I/O
I/O, L16P	0	G11	-	-	I/O, L16P	I/O, L16P
I/O, L16N	0	H11	-	-	I/O, L16N	I/O, L16N
I/O	0	C10	-	-	-	I/O
I/O, L15P_YY	0	A10	All	-	I/O, L15P_YY	I/O, L15P_YY
I/O, L15N_YY	0	B10	All	-	I/O, L15N_YY	I/O, L15N_YY
I/O, L14P_YY	0	D10	All	-	I/O, L14P_YY	I/O, L14P_YY

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L14N_YY	0	E10	All	-	I/O, L14N_YY	I/O, L14N_YY
I/O	0	G10	-	-	-	I/O
I/O, L13P	0	A9	XC2S600E	-	I/O, L13P	I/O, L13P_Y
I/O, L13N	0	B9	XC2S600E	-	I/O, L13N	I/O, L13N_Y
I/O	0	H10	-	-	-	I/O
I/O, L12P_YY	0	C9	All	-	I/O, L12P_YY	I/O, L12P_YY
I/O, L12N_YY	0	D9	All	-	I/O, L12N_YY	I/O, L12N_YY
I/O	0	E9	-	-	I/O	I/O
I/O, VREF Bank 0, L11P	0	F9	-	All	I/O, VREF Bank 0, L11P	I/O, VREF Bank 0, L11P
I/O, L11N	0	G9	-	-	I/O, L11N	I/O, L11N
I/O, L10P	0	A8	-	-	I/O, L10P	I/O, L10P
I/O, L10N	0	B8	-	-	I/O, L10N	I/O, L10N
I/O	0	H9	-	-	I/O	I/O
I/O, L9P	0	E8	XC2S600E	-	I/O	I/O, L9P_Y
I/O, L9N	0	F8	XC2S600E	XC2S600E	-	I/O, VREF Bank 0, L9N_Y
I/O, L8P	0	A7	XC2S600E	-	I/O, L8P	I/O, L8P_Y
I/O, L8N	0	B7	XC2S600E	-	I/O, L8N	I/O, L8N_Y
I/O	0	G8	-	-	I/O	I/O
I/O, L7P_YY	0	C7	All	-	I/O, L7P_YY	I/O, L7P_YY
I/O, L7N_YY	0	D7	All	-	I/O, L7N_YY	I/O, L7N_YY
I/O	0	E7	-	-	-	I/O
I/O, L6P_YY	0	F7	All	-	I/O, L6P_YY	I/O, L6P_YY
I/O, VREF Bank 0, L6N_YY	0	G7	All	All	I/O, VREF Bank 0, L6N_YY	I/O, VREF Bank 0, L6N_YY
I/O	0	A6	-	-	I/O	I/O
I/O, L5P	0	B6	-	-	I/O, L5P	I/O, L5P
I/O, L5N	0	C6	-	-	I/O, L5N	I/O, L5N
I/O, L4P	0	D6	-	-	I/O, L4P	I/O, L4P
I/O, L4N	0	E6	-	-	I/O, L4N	I/O, L4N
I/O	0	F6	-	-	-	I/O
I/O, L3P_YY	0	A5	All	-	I/O, L3P_YY	I/O, L3P_YY
I/O, VREF Bank 0, L3N_YY	0	B5	All	All	I/O, VREF Bank 0, L3N_YY	I/O, VREF Bank 0, L3N_YY
I/O, L2P_YY	0	D5	All	-	I/O, L2P_YY	I/O, L2P_YY

Revision History

Date	Version	Description
11/15/2001	1.0	Initial Xilinx release.
12/20/2001	1.1	Corrected differential pin pair designations.
11/18/2002	2.0	Added XC2S400E and XC2S600E and FG676. Removed L37 designation from FT256 pinouts. Minor corrections and clarifications to pinout definitions. Removed Preliminary designation.
02/14/2003	2.1	Added differential pairs table on page 57, fixed 3 P/N designation typos introduced in v2.0. Clarified that XC2S50E has two VREF pins per bank.
06/18/2008	2.3	Added Package Overview section. Updated all modules for continuous page, figure, and table numbering. Updated links. Synchronized all modules to v2.3.
08/09/2013	3.0	This product is obsolete/discontinued per XCN12026.