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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 600 |
| Number of Logic Elements/Cells | 2700 |
| Total RAM Bits | 40960 |
| Number of I/O | 102 |
| Number of Gates | 100000 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2s100e-6tqg144c |

# Spartan-IIE FPGA Family: Introduction and Ordering Information

DS077-1 (v3.0) August 9, 2013

**Product Specification**

## Introduction

The Spartan®-IIE Field-Programmable Gate Array family gives users high performance, abundant logic resources, and a rich feature set, all at an exceptionally low price. The seven-member family offers densities ranging from 50,000 to 600,000 system gates, as shown in Table 1. System performance is supported beyond 200 MHz.

Features include block RAM (to 288K bits), distributed RAM (to 221,184 bits), 19 selectable I/O standards, and four DLLs (Delay-Locked Loops). Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

The Spartan-IIE family is a superior alternative to mask-programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary (impossible with ASICs).

## Features

- Second generation ASIC replacement technology
  - Densities as high as 15,552 logic cells with up to 600,000 system gates
  - Streamlined features based on Virtex®-E FPGA architecture
  - Unlimited in-system reprogrammability
  - Very low cost
  - Cost-effective 0.15 micron technology
- System level features
  - SelectRAM™ hierarchical memory:
    - 16 bits/LUT distributed RAM
    - Configurable 4K-bit true dual-port block RAM
    - Fast interfaces to external RAM
  - Fully 3.3V PCI compliant to 64 bits at 66 MHz and CardBus compliant
  - Low-power segmented routing architecture
  - Dedicated carry logic for high-speed arithmetic
  - Efficient multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with enable, set, reset
  - Four dedicated DLLs for advanced clock control
    - Eliminate clock distribution delay
    - Multiply, divide, or phase shift
  - Four primary low-skew global clock distribution nets
  - IEEE 1149.1 compatible boundary scan logic
- Versatile I/O and packaging
  - Pb-free package options
  - Low-cost packages available in all densities
  - Family footprint compatibility in common packages
  - 19 high-performance interface standards
    - LVTTL, LVCMOS, HSTL, SSTL, AGP, CTT, GTL
    - LVDS and LVPECL differential I/O
  - Up to 205 differential I/O pairs that can be input, output, or bidirectional
  - Hot swap I/O (CompactPCI friendly)
- Core logic powered at 1.8V and I/Os powered at 1.5V, 2.5V, or 3.3V
- Fully supported by powerful Xilinx® ISE® development system
  - Fully automatic mapping, placement, and routing
  - Integrated with design entry and verification tools
  - Extensive IP library including DSP functions and soft processors

*Table 1:* **Spartan-IIE FPGA Family Members**

| Device | Logic Cells | Typical System Gate Range (Logic and RAM) | CLB Array (R x C) | Total CLBs | Maximum Available User I/O(1) | Maximum Differential I/O Pairs | Distributed RAM Bits | Block RAM Bits |
|---|---|---|---|---|---|---|---|---|
| XC2S50E | 1,728 | 23,000 - 50,000 | 16 x 24 | 384 | 182 | 83 | 24,576 | 32K |
| XC2S100E | 2,700 | 37,000 - 100,000 | 20 x 30 | 600 | 202 | 86 | 38,400 | 40K |
| XC2S150E | 3,888 | 52,000 - 150,000 | 24 x 36 | 864 | 265 | 114 | 55,296 | 48K |
| XC2S200E | 5,292 | 71,000 - 200,000 | 28 x 42 | 1,176 | 289 | 120 | 75,264 | 56K |
| XC2S300E | 6,912 | 93,000 - 300,000 | 32 x 48 | 1,536 | 329 | 120 | 98,304 | 64K |
| XC2S400E | 10,800 | 145,000 - 400,000 | 40 x 60 | 2,400 | 410 | 172 | 153,600 | 160K |
| XC2S600E | 15,552 | 210,000 - 600,000 | 48 x 72 | 3,456 | 514 | 205 | 221,184 | 288K |

**Notes:**

1. User I/O counts include the four global clock/user input pins. See details in Table 2, page 5

## Spartan-IIE Product Availability

Table 2 shows the maximum user I/Os available on the device and the number of user I/Os available for each device/package combination.

*Table 2:* **Spartan-IIE FPGA User I/O Chart**

| Device | Maximum User I/O | Available User I/O According to Package Type | | | | |
|---|---|---|---|---|---|---|
| | | TQ144 TQG144 | PQ208 PQG208 | FT256 FTG256 | FG456 FGG456 | FG676 FGG676 |
| XC2S50E | 182 | 102 | 146 | 182 | - | - |
| XC2S100E | 202 | 102 | 146 | 182 | 202 | - |
| XC2S150E | 265 | - | 146 | 182 | 265 | - |
| XC2S200E | 289 | - | 146 | 182 | 289 | - |
| XC2S300E | 329 | - | 146 | 182 | 329 | - |
| XC2S400E | 410 | - | - | 182 | 329 | 410 |
| XC2S600E | 514 | - | - | - | 329 | 514 |

**Notes:**
1. User I/O counts include the four global clock/user input pins.

*Table 8:* **Boundary-Scan Instructions *(Continued)***

| Boundary-Scan Command | Binary Code[4:0] | Description |
|---|---|---|
| INTEST | 00111 | Enables boundary-scan INTEST operation |
| USERCODE | 01000 | Enables shifting out USER code |
| IDCODE | 01001 | Enables shifting out of ID Code |
| HIGHZ | 01010 | Disables output pins while enabling the Bypass Register |
| JSTART | 01100 | Clock the start-up sequence when StartupClk is TCK |
| BYPASS | 11111 | Enables BYPASS |
| RESERVED | All other codes | Xilinx reserved instructions |

The public boundary-scan instructions are available prior to configuration, except for USER1 and USER2. After configuration, the public instructions remain available together with any USERCODE instructions installed during the configuration. While the SAMPLE/PRELOAD and BYPASS instructions are available during configuration, it is recommended that boundary-scan operations not be performed during this transitional period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

To facilitate internal scan chains, the User Register provides three outputs (Reset, Update, and Shift) that represent the corresponding states in the boundary-scan internal state machine.

Figure 14 is a diagram of the Spartan-IIE family boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

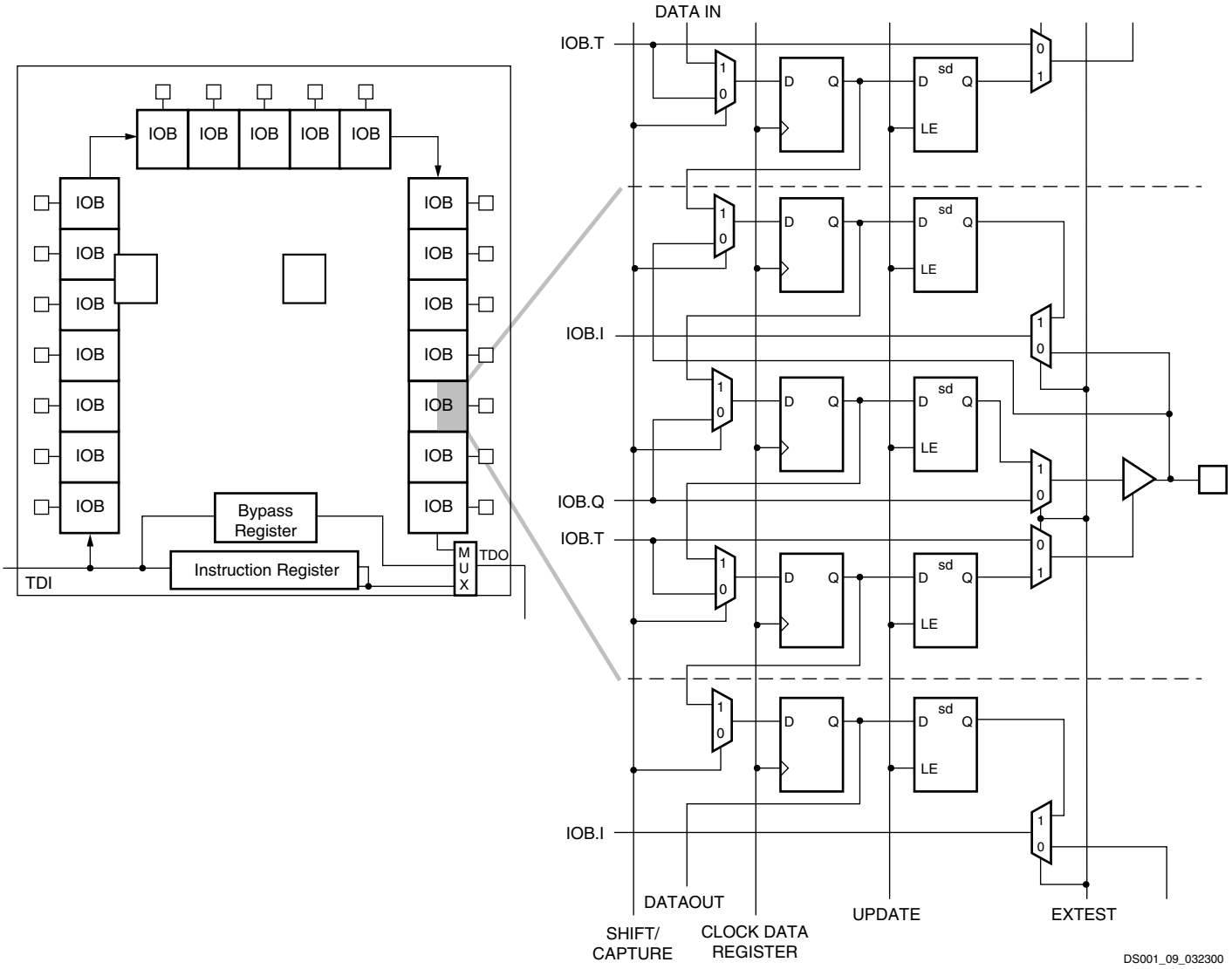


*Figure 14:* **Spartan-IIE Family Boundary Scan Logic**

## Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRACE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-IIE devices unless otherwise noted.

### Global Clock Input to Output Delay for LVTTL, *with* DLL (Pin-to-Pin)(1)

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | All | -7 | -6 | |
| | | Min | Max | Max | |
| $T_{ICKOFDLL}$ | LVTTL global clock input to output delay using output flip-flop for LVTTL, 12 mA, fast slew rate, *with* DLL. | 1.0 | 3.1 | 3.1 | ns |

**Notes:**
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables Constants for Calculating $T_{IOOP}$ and Delay Measurement Methodology, page 41.
3. DLL output jitter is already included in the timing calculation.
4. For data *output* with different standards, adjust delays with the values shown in IOB Output Delay Adjustments for Different Standards(1), page 40. For a global clock input with standards other than LVTTL, adjust delays with values from the I/O Standard Global Clock Input Adjustments, page 42.

### Global Clock Input to Output Delay for LVTTL, *without* DLL (Pin-to-Pin)(1)

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | All | -7 | -6 | |
| | | | Min | Max | Max | |
| $T_{ICKOF}$ | LVTTL global clock input to output delay using output flip-flop for LVTTL, 12 mA, fast slew rate, *without* DLL. | XC2S50E | 1.5 | 4.4 | 4.6 | ns |
| | | XC2S100E | 1.5 | 4.4 | 4.6 | ns |
| | | XC2S150E | 1.5 | 4.5 | 4.7 | ns |
| | | XC2S200E | 1.5 | 4.5 | 4.7 | ns |
| | | XC2S300E | 1.5 | 4.5 | 4.7 | ns |
| | | XC2S400E | 1.5 | 4.6 | 4.8 | ns |
| | | XC2S600E | 1.6 | 4.7 | 4.9 | ns |

**Notes:**
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables Constants for Calculating $T_{IOOP}$ and Delay Measurement Methodology, page 41.
3. For data *output* with different standards, adjust delays with the values shown in IOB Output Delay Adjustments for Different Standards(1), page 40. For a global clock input with standards other than LVTTL, adjust delays with values from the I/O Standard Global Clock Input Adjustments, page 42.

## CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -7 | | -6 | | |
| | | Min | Max | Min | Max | |
| **Combinatorial Delays** | | | | | | |
| $T_{ILO}$ | 4-input function: F/G inputs to X/Y outputs | 0.18 | 0.42 | 0.18 | 0.47 | ns |
| $T_{IF5}$ | 5-input function: F/G inputs to F5 output | 0.3 | 0.8 | 0.3 | 0.9 | ns |
| $T_{IF5X}$ | 5-input function: F/G inputs to X output | 0.3 | 0.8 | 0.3 | 0.9 | ns |
| $T_{IF6Y}$ | 6-input function: F/G inputs to Y output via F6 MUX | 0.3 | 0.9 | 0.3 | 1.0 | ns |
| $T_{F5INY}$ | 6-input function: F5IN input to Y output | 0.04 | 0.2 | 0.04 | 0.22 | ns |
| $T_{IFNCTL}$ | Incremental delay routing through transparent latch to XQ/YQ outputs | - | 0.7 | - | 0.8 | ns |
| $T_{BYYB}$ | BY input to YB output | 0.18 | 0.46 | 0.18 | 0.51 | ns |
| **Sequential Delays** | | | | | | |
| $T_{CKO}$ | FF clock CLK to XQ/YQ outputs | 0.3 | 0.9 | 0.3 | 1.0 | ns |
| $T_{CKLO}$ | Latch clock CLK to XQ/YQ outputs | 0.3 | 0.9 | 0.3 | 1.0 | ns |
| **Setup/Hold Times with Respect to Clock CLK** | | | | | | |
| $T_{ICK}$ / $T_{CKI}$ | 4-input function: F/G inputs | 1.0 / 0 | - | 1.1 / 0 | - | ns |
| $T_{IF5CK}$ / $T_{CKIF5}$ | 5-input function: F/G inputs | 1.4 / 0 | - | 1.5 / 0 | - | ns |
| $T_{F5INCK}$ / $T_{CKF5IN}$ | 6-input function: F5IN input | 0.8 / 0 | - | 0.8 / 0 | - | ns |
| $T_{IF6CK}$ / $T_{CKIF6}$ | 6-input function: F/G inputs via F6 MUX | 1.5 / 0 | - | 1.6 / 0 | - | ns |
| $T_{DICK}$ / $T_{CKDI}$ | BX/BY inputs | 0.7 / 0 | - | 0.8 / 0 | - | ns |
| $T_{CECK}$ / $T_{CKCE}$ | CE input | 0.7 / 0 | - | 0.7 / 0 | - | ns |
| $T_{RCK}$ / $T_{CKR}$ | SR/BY inputs (synchronous) | 0.52 / 0 | - | 0.6 / 0 | - | ns |
| **Clock CLK** | | | | | | |
| $T_{CH}$ | Pulse width, High | 1.3 | - | 1.4 | - | ns |
| $T_{CL}$ | Pulse width, Low | 1.3 | - | 1.4 | - | ns |
| **Set/Reset** | | | | | | |
| $T_{RPW}$ | Pulse width, SR/BY inputs | 2.1 | - | 2.4 | - | ns |
| $T_{RQ}$ | Delay from SR/BY inputs to XQ/YQ outputs (asynchronous) | 0.3 | 0.9 | 0.3 | 1.0 | ns |
| $F_{TOG}$ | Toggle frequency (for export control) | - | 400 | - | 357 | MHz |

# Spartan-IIE FPGA Family: Pinout Tables

DS077-4 (v3.0) August 9, 2013

**Product Specification**

## Introduction

This section describes how the various pins on a Spartan®-IIE FPGA connect within the supported component packages, and provides device-specific thermal characteristics. Spartan-IIE FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a “G” to the middle of the package code. Except for the thermal characteristics, all information for the standard package applies equally to the Pb-free package.

## Pin Types

Most pins on a Spartan-IIE FPGA are general-purpose, user-defined I/O pins. There are, however, different functional types of pins on Spartan-IIE FPGA packages, as outlined below.

## Pin Definitions

| Pad Name | Dedicated Pin | Direction | Description |
|---|---|---|---|
| GCK0, GCK1, GCK2, GCK3 | No | Input | Clock input pins that connect to Global Clock buffers or DLL inputs. These pins become user inputs when not needed for clocks. |
| DLL | No | Input | Clock input pins that connect to DLL input or feedback clocks. Differential clock input (N input of pair) when paired with adjacent GCK input. Becomes a user I/O when not needed for clocks. |
| M0, M1, M2 | Yes | Input | Mode pins used to specify the configuration mode. |
| CCLK | Yes | Input or Output | The configuration Clock I/O pin. It is an input for Slave Parallel and Slave Serial modes, and output in Master Serial mode. After configuration, it is an input only with Don’t Care logic levels. |
| $\overline{\text{PROGRAM}}$ | Yes | Input | Initiates a configuration sequence when asserted Low. |
| DONE | Yes | Bidirectional | Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output may be open drain. |
| $\overline{\text{INIT}}$ | No | Bidirectional (Open-drain) | When Low, indicates that the configuration memory is being cleared. Goes High to indicate the end of initialization. Goes back Low to indicate a CRC error. This pin becomes a user I/O after configuration. |
| DOUT/BUSY | No | Output | In Slave Parallel mode, BUSY controls the rate at which configuration data can be loaded. It is not needed below 50 MHz. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.<br>In serial modes, DOUT provides configuration data to downstream devices in a daisy-chain. This pin becomes a user I/O after configuration. |

## TQ144 Pinouts (XC2S50E and XC2S100E) *(Continued)*

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| | | | | |
| I/O ($\overline{CS}$), L5P_YY | 1 | P112 | All | - |
| I/O ($\overline{WRITE}$), L5N_YY | 1 | P113 | All | - |
| I/O | 1 | P114 | - | - |
| I/O, VREF Bank 1 | 1 | P115 | - | All |
| I/O | 1 | P116 | - | - |
| I/O, L4P_YY | 1 | P117 | All | XC2S100E |
| I/O, L4N_YY | 1 | P118 | All | - |
| GND | - | P119 | - | - |
| VCCINT | - | P120 | - | - |
| I/O, L3P_YY | 1 | P121 | All | - |
| I/O, L3N_YY | 1 | P122 | All | - |
| I/O, VREF Bank 1 | 1 | P123 | - | All |
| I/O | 1 | P124 | - | - |
| I/O (DLL), L2P | 1 | P125 | - | - |
| GCK2, I | 1 | P126 | - | - |
| GND | - | P127 | - | - |
| VCCO | - | P128 | - | - |
| | | | | |
| GCK3, I | 0 | P129 | - | - |
| VCCINT | - | P130 | - | - |
| I/O (DLL), L2N | 0 | P131 | - | - |
| I/O, VREF Bank 0 | 0 | P132 | - | All |
| I/O, L1P_YY | 0 | P133 | All | - |
| I/O, L1N_YY | 0 | P134 | All | - |
| VCCINT | - | P135 | - | - |
| GND | - | P136 | - | - |
| I/O, L0P_YY | 0 | P137 | All | - |
| I/O, L0N_YY | 0 | P138 | All | XC2S100E |

## TQ144 Pinouts (XC2S50E and XC2S100E) *(Continued)*

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| I/O | 0 | P139 | - | - |
| I/O, VREF Bank 0 | 0 | P140 | - | All |
| I/O | 0 | P141 | - | - |
| I/O | 0 | P142 | - | - |
| TCK | - | P143 | - | - |
| VCCO | - | P144 | - | - |

## TQ144 Differential Clock Pins

| Clock | Bank | P | | N | |
|---|---|---|---|---|---|
| | | Pin | Name | Pin | Name |
| GCK0 | 4 | P55 | GCK0, I | P56 | I/O (DLL), L17P |
| GCK1 | 5 | P52 | GCK1, I | P50 | I/O (DLL), L17N |
| GCK2 | 1 | P126 | GCK2, I | P125 | I/O (DLL), L2P |
| GCK3 | 0 | P129 | GCK3, I | P131 | I/O (DLL), L2N |

In the PQ208 package, all VCCO pins must be connected to the same voltage.

## PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| GND | - | P1 | - | - |
| TMS | - | P2 | - | - |
| I/O | 7 | P3 | - | - |
| I/O | 7 | P4 | - | XC2S200E, 300E |
| I/O | 7 | P5 | - | - |
| I/O, VREF Bank 7, L49P | 7 | P6 | XC2S50E, 150E, 200E, 300E | All |
| I/O, L49N | 7 | P7 | XC2S50E, 150E, 200E, 300E | - |
| I/O | 7 | P8 | - | - |
| I/O | 7 | P9 | - | - |
| I/O, L48P | 7 | P10 | XC2S50E, 300E | XC2S100E, 150E, 200E, 300E |
| I/O, L48N | 7 | P11 | XC2S50E, 300E | - |
| GND | - | P12 | - | - |
| VCCO | - | P13 | - | - |
| VCCINT | - | P14 | - | - |
| I/O, L47P_YY | 7 | P15 | All | - |
| I/O, L47N_YY | 7 | P16 | All | - |
| I/O, L46P_YY | 7 | P17 | All | - |
| I/O, L46N_YY | 7 | P18 | All | - |
| GND | - | P19 | - | - |
| I/O, VREF Bank 7, L45P | 7 | P20 | XC2S50E, 300E | All |
| I/O, L45N | 7 | P21 | XC2S50E, 300E | - |

## PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| I/O | 7 | P22 | - | - |
| I/O, L44P_YY | 7 | P23 | All | - |
| I/O (IRDY), L44N_YY | 7 | P24 | All | - |
| GND | - | P25 | - | - |
| VCCO | - | P26 | - | - |
| | | | | |
| I/O (TRDY) | 6 | P27 | - | - |
| VCCINT | - | P28 | - | - |
| I/O | 6 | P29 | - | - |
| I/O, L43P | 6 | P30 | XC2S50E, 300E | - |
| I/O, VREF Bank 6, L43N | 6 | P31 | XC2S50E, 300E | All |
| GND | - | P32 | - | - |
| I/O, L42P_YY | 6 | P33 | All | - |
| I/O, L42N_YY | 6 | P34 | All | - |
| I/O, L41P_YY | 6 | P35 | All | - |
| I/O, L41N_YY | 6 | P36 | All | - |
| VCCINT | - | P37 | - | - |
| VCCO | - | P38 | - | - |
| GND | - | P39 | - | - |
| I/O, L40P | 6 | P40 | XC2S50E, 300E | - |
| I/O, L40N | 6 | P41 | XC2S50E, 300E | XC2S100E, 150E, 200E, 300E |
| I/O | 6 | P42 | - | - |
| I/O | 6 | P43 | - | - |
| I/O | 6 | P44 | - | - |

## FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E)

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| TMS | - | B1 | - | - |
| I/O | 7 | D3 | - | - |
| I/O, L83P | 7 | C2 | XC2S100E, 150E | - |
| I/O, L83N | 7 | C1 | XC2S100E, 150E | XC2S200E, 300E, 400E |
| I/O, L82P_YY | 7 | D2 | All | - |
| I/O, L82N_YY | 7 | D1 | All | - |
| I/O, VREF Bank 7, L81P | 7 | E3 | XC2S50E, 150E, 200E, 300E, 400E | All |
| I/O, L81N | 7 | E4 | XC2S50E, 150E, 200E, 300E, 400E | - |
| I/O, L80P | 7 | E2 | XC2S200E, 400E | - |
| I/O, L80N | 7 | E1 | XC2S200E, 400E | - |
| I/O, L79P | 7 | F4 | XC2S50E, 300E, 400E | XC2S100E, 150E, 200E, 300E, 400E |
| I/O, L79N | 7 | F3 | XC2S50E, 300E, 400E | - |
| I/O, L78P_YY | 7 | F2 | All | - |
| I/O, L78N_YY | 7 | F1 | All | - |
| I/O, L77P | 7 | F5 | XC2S100E, 150E | - |
| I/O, L77N | 7 | G5 | XC2S100E, 150E | - |
| I/O, L76P_YY | 7 | G3 | All | - |
| I/O, L76N_YY | 7 | G4 | All | - |
| I/O, VREF Bank 7, L75P | 7 | G2 | XC2S50E, 300E, 400E | All |
| I/O, L75N | 7 | G1 | XC2S50E, 300E, 400E | - |

## FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| I/O, L74P | 7 | H4 | XC2S100E, 150E, 200E | - |
| I/O, L74N | 7 | H3 | XC2S100E, 150E, 200E | XC2S400E |
| I/O, L73P_YY | 7 | H2 | All | - |
| I/O (IRDY), L73N_YY | 7 | H1 | All | - |
| | | | | |
| I/O (TRDY) | 6 | J4 | - | - |
| I/O, L72P | 6 | J2 | XC2S100E, 150E, 200E, 400E | XC2S400E |
| I/O, L72N | 6 | J3 | XC2S100E, 150E, 200E, 400E | - |
| I/O, L71P | 6 | J1 | XC2S50E, 300E, 400E | - |
| I/O, VREF Bank 6, L71N | 6 | K1 | XC2S50E, 300E, 400E | All |
| I/O, L70P_YY | 6 | K2 | All | - |
| I/O, L70N_YY | 6 | K3 | All | - |
| I/O, L69P | 6 | L1 | XC2S100E, 150E, 400E | - |
| I/O, L69N | 6 | L2 | XC2S100E, 150E, 400E | - |
| I/O, L68P_YY | 6 | K4 | All | - |
| I/O, L68N_YY | 6 | K5 | All | - |
| I/O, L67P | 6 | L3 | XC2S50E, 300E, 400E | - |
| I/O, L67N | 6 | M2 | XC2S50E, 300E, 400E | XC2S100E, 150E, 200E, 300E, 400E |
| I/O, L66P | 6 | M1 | XC2S150E, 200E, 400E | - |
| I/O, L66N | 6 | N1 | XC2S150E, 200E, 400E | - |

## FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| I/O (D5), L35N_YY | 3 | L13 | All | - |
| I/O, L35P_YY | 3 | K14 | All | - |
| I/O, L34N | 3 | K15 | XC2S100E, 150E, 400E | - |
| I/O, L34P | 3 | K16 | XC2S100E, 150E, 400E | - |
| I/O, L33N | 3 | L12 | XC2S50E, 100E, 150E, 200E, 300E(1) | - |
| I/O, L33P | 3 | K12 | XC2S50E, 100E, 150E, 200E, 300E(1) | - |
| I/O, VREF Bank 3, L32N | 3 | K13 | XC2S50E, 300E, 400E | All |
| I/O (D4), L32P | 3 | J14 | XC2S50E, 300E, 400E | - |
| I/O, L31N | 3 | J15 | XC2S100E, 150E, 200E, 400E | - |
| I/O, L31P | 3 | J16 | XC2S100E, 150E, 200E, 400E | XC2S400E |
| I/O (TRDY) | 3 | J13 | - | - |
| | | | | |
| I/O (IRDY), L30N_YY | 2 | H16 | All | - |
| I/O, L30P_YY | 2 | G16 | All | - |
| I/O, L29N | 2 | H14 | XC2S100E, 150E, 200E, 400E | XC2S400E |
| I/O, L29P | 2 | H15 | XC2S100E, 150E, 200E, 400E | - |
| I/O (D3), L28N | 2 | G15 | XC2S50E, 300E, 400E | - |

## FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| I/O, VREF Bank 2, L28P | 2 | F16 | XC2S50E, 300E, 400E | All |
| I/O, L27N | 2 | H13 | XC2S50E, 100E, 150E, 200E, 300E(1) | - |
| I/O, L27P | 2 | G14 | XC2S50E, 100E, 150E, 200E, 300E(2) | - |
| I/O, L26N | 2 | F15 | XC2S100E, 150E, 400E | - |
| I/O, L26P | 2 | E16 | XC2S100E, 150E, 400E | - |
| I/O, L25N_YY | 2 | G13 | All | - |
| I/O (D2), L25P_YY | 2 | F14 | All | - |
| I/O (D1), L24N | 2 | E15 | XC2S50E, 300E, 400E | - |
| I/O, L24P | 2 | D16 | XC2S50E, 300E, 400E | XC2S100E, 150E, 200E, 300E, 400E |
| I/O, L23N | 2 | F13 | XC2S150E, 200E, 400E | - |
| I/O, L23P | 2 | E14 | XC2S150E, 200E, 400E | - |
| I/O, L22N | 2 | D15 | XC2S50E, 150E, 200E, 300E, 400E | - |
| I/O, VREF Bank 2, L22P | 2 | C16 | XC2S50E, 150E, 200E, 300E, 400E | All |
| I/O, L21N | 2 | G12 | XC2S50E, 100E, 200E, 300E | - |
| I/O, L21P | 2 | F12 | XC2S50E, 100E, 200E, 300E | - |
| I/O, L20N | 2 | E13 | XC2S100E, 200E, 300E | - |

## FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| I/O, L20P | 2 | D14 | XC2S100E, 200E, 300E | XC2S200E, 300E, 400E |
| I/O (DIN, D0), L19N_YY | 2 | B16 | All | - |
| I/O (DOUT, BUSY), L19P_YY | 2 | C15 | All | - |
| CCLK | 2 | A15 | - | - |
| TDO | 2 | B14 | - | - |
| TDI | - | C13 | - | - |
| | | | | |
| I/O ($\overline{CS}$), L18P_YY | 1 | A14 | All | - |
| I/O ($\overline{WRITE}$), L18N_YY | 1 | A13 | All | - |
| I/O, L17P | 1 | B13 | XC2S50E, 100E, 200E, 300E, 400E | XC2S200E, 300E, 400E |
| I/O, L17N | 1 | C12 | XC2S50E, 100E, 200E, 300E, 400E | - |
| I/O, L16P_YY | 1 | B12 | All | - |
| I/O, L16N_YY | 1 | A12 | All | - |
| I/O, VREF Bank 1, L15P_YY | 1 | D12 | All | All |
| I/O, L15N_YY | 1 | E11 | All | - |
| I/O, L14P | 1 | D11 | XC2S50E, 100E, 150E, 300E | - |
| I/O, L14N | 1 | C11 | XC2S50E, 100E, 150E, 300E | - |
| I/O, L13P | 1 | B11 | XC2S50E, 100E, 200E, 300E, 400E | XC2S100E, 150E, 200E, 300E, 400E |
| I/O, L13N | 1 | A11 | XC2S50E, 100E, 200E, 300E, 400E | - |

## FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| I/O, L12P | 1 | E10 | XC2S50E, 100E, 200E, 300E, 400E | - |
| I/O, L12N | 1 | D10 | XC2S50E, 100E, 200E, 300E, 400E | - |
| I/O | 1 | C10 | - | - |
| I/O, L11P | 1 | B10 | XC2S50E, 200E, 300E, 400E | - |
| I/O, L11N | 1 | A10 | XC2S50E, 200E, 300E, 400E | - |
| I/O, VREF Bank 1, L10P | 1 | D9 | XC2S50E, 200E, 300E, 400E | All |
| I/O, L10N | 1 | C9 | XC2S50E, 200E, 300E, 400E | - |
| I/O, L9P | 1 | B9 | XC2S50E, 150E, 200E, 400E | - |
| I/O, L9N | 1 | A9 | XC2S50E, 150E, 200E, 400E | XC2S400E |
| I/O (DLL), L8P | 1 | A8 | - | - |
| GCK2, I | 1 | B8 | - | - |
| | | | | |
| GCK3, I | 0 | C8 | - | - |
| I/O (DLL), L8N | 0 | D8 | - | - |
| I/O | 0 | A7 | - | XC2S400E |
| I/O, L7P | 0 | E7 | XC2S50E, 200E, 300E, 400E | - |
| I/O, VREF Bank 0, L7N | 0 | D7 | XC2S50E, 200E, 300E, 400E | All |

## FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option | Device-Specific Pinouts: XC2S | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Function | Bank | | | | 100E | 150E | 200E | 300E | 400E | 600E |
| TMS | - | E4 | - | - | TMS | TMS | TMS | TMS | TMS | TMS |
| I/O | 7 | D3 | XC2S150E | - | I/O | I/O, L113P_Y | I/O | I/O | I/O | I/O |
| I/O | 7 | C2 | - | - | - | - | - | I/O | I/O | I/O |
| I/O | 7 | C1 | XC2S150E | - | - | I/O, L113N_Y | I/O | I/O | I/O | I/O |
| I/O, L#P_Y | 7 | D2 | XC2S150E, 200E, 300E, 400E | - | - | I/O, L112P_Y | I/O, L119P_Y | I/O, L119P_Y | I/O, L119P_Y | I/O, L119P |
| I/O, L#N_Y | 7 | D1 | XC2S150E, 200E, 300E, 400E | - | I/O | I/O, L112N_Y | I/O, L119N_Y | I/O, L119N_Y | I/O, L119N_Y | I/O, L119N |
| I/O, L#P_Y | 7 | E2 | XC2S100E, 200E, 300E, 600E | XC2S200E, 300E, 400E, 600E | I/O, L85P_Y | I/O, L111P | I/O, VREF Bank 7, L118P_Y | I/O, VREF Bank 7, L118P_Y | I/O, VREF Bank 7, L118P | I/O, VREF Bank 7, L118P_Y |
| I/O, L#N_Y | 7 | E3 | XC2S100E, 200E, 300E, 600E | - | I/O, L85N_Y | I/O, L111N | I/O, L118N_Y | I/O, L118N_Y | I/O, L118N | I/O, L118N_Y |
| I/O | 7 | E1 | - | - | - | - | - | I/O | I/O | I/O |
| I/O | 7 | F5 | - | - | - | I/O | I/O | I/O | I/O | I/O |
| I/O, L#P_Y | 7 | F4 | XC2S100E, 200E, 300E, 600E | - | I/O, L84P_Y | I/O, L110P | I/O, L117P_Y | I/O, L117P_Y | I/O, L117P | I/O, L117P_Y |
| I/O, L#N_Y | 7 | F3 | XC2S100E, 200E, 300E, 600E | - | I/O, L84N_Y | I/O, L110N | I/O, L117N_Y | I/O, L117N_Y | I/O, L117N | I/O, L117N_Y |
| I/O, VREF Bank 7, L#P_Y | 7 | F2 | XC2S150E, 200E, 300E, 400E, 600E | All | I/O, VREF Bank 7, L83P | I/O, VREF Bank 7, L109P_Y | I/O, VREF Bank 7, L116P_Y | I/O, VREF Bank 7, L116P_Y | I/O, VREF Bank 7, L116P_Y | I/O, VREF Bank 7, L116P_Y |
| I/O, L#N_Y | 7 | F1 | XC2S150E, 200E, 300E, 400E, 600E | - | I/O, L83N | I/O, L109N_Y | I/O, L116N_Y | I/O, L116N_Y | I/O, L116N_Y | I/O, L116N_Y |
| I/O | 7 | G5 | - | - | - | I/O | I/O | I/O | I/O | I/O |
| I/O, L#P_Y | 7 | G4 | XC2S150E, 200E, 300E, 400E | - | - | I/O, L108P_Y | I/O, L115P_Y | I/O, L115P_Y | I/O, L115P_Y | I/O, L115P |
| I/O, L#N_Y | 7 | G3 | XC2S150E, 200E, 300E, 400E | - | I/O | I/O, L108N_Y | I/O, L115N_Y | I/O, L115N_Y | I/O, L115N_Y | I/O, L115N |
| I/O, L#P_Y | 7 | G2 | XC2S100E, 150E, 300E, 600E | XC2S600E | I/O, L82P_Y | I/O, L107P_Y | I/O, L114P | I/O, L114P_Y | I/O, L114P | I/O, VREF Bank 7, L114P_Y |
| I/O, L#N_Y | 7 | G1 | XC2S100E, 150E, 300E, 600E | - | I/O, L82N_Y | I/O, L107N_Y | I/O, L114N | I/O, L114N_Y | I/O, L114N | I/O, L114N_Y |

## FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

| Pad Name | | | LVDS Async. Output Option | $V_{REF}$ Option | Device-Specific Pinouts: XC2S | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Function | Bank | Pin | | | 100E | 150E | 200E | 300E | 400E | 600E |
| I/O, L#P_YY | 7 | L5 | All | - | I/O, L75P_YY | I/O, L99P_YY | I/O, L105P_YY | I/O, L105P_YY | I/O, L105P_YY | I/O, L105P_YY |
| I/O (IRDY), L#N_YY | 7 | L6 | All | - | I/O (IRDY), L75N_YY | I/O (IRDY), L99N_YY | I/O (IRDY), L105N_YY | I/O (IRDY), L105N_YY | I/O (IRDY), L105N_YY | I/O (IRDY), L105N_YY |
| | | | | | | | | | | |
| I/O (TRDY) | 6 | M1 | - | - | I/O (TRDY) | I/O (TRDY) | I/O (TRDY) | I/O (TRDY) | I/O (TRDY) | I/O (TRDY) |
| I/O | 6 | M2 | - | - | - | - | - | I/O | I/O | I/O |
| I/O, L#P_Y | 6 | M3 | XC2S200E, 300E, 600E | - | - | I/O | I/O, L104P_Y | I/O, L104P_Y | I/O, L104P | I/O, L104P_Y |
| I/O, L#N_Y | 6 | M4 | XC2S100E, 150E, 200E, 300E, 600E | XC2S400E, 600E | I/O, L74P_Y | I/O, L98P_Y | I/O, L104N_Y | I/O, L104N_Y | I/O, VREF Bank 6, L104N | I/O, VREF Bank 6, L104N_Y |
| I/O, L#P_Y | 6 | M5 | XC2S100E, 150E, 300E, 400E | - | I/O, L74N_Y | I/O, L98N_Y | I/O, L103P | I/O, L103P_Y | I/O, L103P_Y | I/O, L103P |
| I/O, L#N_Y | 6 | M6 | XC2S300E, 400E | - | - | - | I/O, L103N | I/O, L103N_Y | I/O, L103N_Y | I/O, L103N |
| I/O | 6 | N1 | - | - | - | - | - | I/O | I/O | I/O |
| I/O | 6 | N2 | - | - | I/O, L73P | I/O, L97P | I/O | I/O | I/O | I/O |
| I/O, VREF Bank 6, L#P | 6 | N3 | XC2S200E, 400E | All | I/O, VREF Bank 6, L73N | I/O, VREF Bank 6, L97N | I/O, VREF Bank 6, L102P_Y | I/O, VREF Bank 6, L102P | I/O, VREF Bank 6, L102P_Y | I/O, VREF Bank 6, L102P |
| I/O, L#N | 6 | N4 | XC2S100E, 150E, 200E, 400E | - | I/O, L72P_Y | I/O, L96P_Y | I/O, L102N_Y | I/O, L102N | I/O, L102N_Y | I/O, L102N |
| I/O, L#P_Y | 6 | N5 | XC2S100E, 150E, 300E, 600E | - | I/O, L72N_Y | I/O, L96N_Y | I/O, L101P | I/O, L101P_Y | I/O, L101P | I/O, L101P_Y |
| I/O, L#N_Y | 6 | N6 | XC2S300E, 600E | - | - | - | I/O, L101N | I/O, L101N_Y | I/O, L101N | I/O, L101N_Y |
| I/O, L#P_Y | 6 | P1 | XC2S150E, 200E, 300E, 600E | - | - | I/O, L95P_Y | I/O, L100P_Y | I/O, L100P_Y | I/O, L100P | I/O, L100P_Y |
| I/O, L#N_Y | 6 | P2 | XC2S100E, 150E, 200E, 300E, 600E | - | I/O, L71P_Y | I/O, L95N_Y | I/O, L100N_Y | I/O, L100N_Y | I/O, L100N | I/O, L100N_Y |
| I/O | 6 | R1 | XC2S100E, 150E | - | I/O, L71N_Y | I/O, L94P_Y | I/O | I/O | I/O | I/O |
| I/O, L#P_Y | 6 | P3 | XC2S150E, 200E, 300E, 400E, 600E | - | - | I/O, L94N_Y | I/O, L99P_Y | I/O, L99P_Y | I/O, L99P_Y | I/O, L99P_Y |
| I/O, L#N_Y | 6 | P4 | XC2S200E, 300E, 400E, 600E | - | - | - | I/O, L99N_Y | I/O, L99N_Y | I/O, L99N_Y | I/O, L99N_Y |
| I/O, L#P_YY | 6 | P5 | All | - | I/O, L70P_YY | I/O, L93P_YY | I/O, L98P_YY | I/O, L98P_YY | I/O, L98P_YY | I/O, L98P_YY |
| I/O, L#N_YY | 6 | P6 | All | - | I/O, L70N_YY | I/O, L93N_YY | I/O, L98N_YY | I/O, L98N_YY | I/O, L98N_YY | I/O, L98N_YY |

## FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

| Pad Name | | | LVDS Async. Output Option | $V_{REF}$ Option | Device-Specific Pinouts: XC2S | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Function | Bank | Pin | | | 100E | 150E | 200E | 300E | 400E | 600E |
| I/O, L#P_Y | 6 | R2 | XC2S300E, 400E, 600E | - | I/O, L69P | I/O, L92P | I/O, L97P | I/O, L97P_Y | I/O, L97P_Y | I/O, L97P_Y |
| I/O, VREF Bank 6, L#N_Y | 6 | R3 | XC2S300E, 400E, 600E | All | I/O, VREF Bank 6, L69N | I/O, VREF Bank 6, L92N | I/O, VREF Bank 6, L97N | I/O, VREF Bank 6, L97N_Y | I/O, VREF Bank 6, L97N_Y | I/O, VREF Bank 6, L97N_Y |
| I/O | 6 | R4 | - | - | - | - | - | I/O | I/O | I/O |
| I/O | 6 | R5 | - | - | I/O | I/O | I/O | I/O | I/O | I/O |
| I/O, L#P | 6 | T2 | XC2S200E, 400E, 600E | XC2S600E | I/O, L68P | I/O, L91P | I/O, L96P_Y | I/O, L96P | I/O, L96P_Y | I/O, VREF Bank 6, L96P_Y |
| I/O, L#N | 6 | T3 | XC2S200E, 400E, 600E | - | I/O, L68N | I/O, L91N | I/O, L96N_Y | I/O, L96N | I/O, L96N_Y | I/O, L96N_Y |
| I/O, L#P_Y | 6 | T4 | XC2S150E, 300E, 400E | - | - | I/O, L90P_Y | I/O, L95P | I/O, L95P_Y | I/O, L95P_Y | I/O, L95P |
| I/O, L#N_Y | 6 | T5 | XC2S150E, 300E, 400E | - | - | I/O, L90N_Y | I/O, L95N | I/O, L95N_Y | I/O, L95N_Y | I/O, L95N |
| I/O, L#P_Y | 6 | T1 | XC2S150E, 200E, 300E, 400E, 600E | - | I/O, L67P | I/O, L89P_Y | I/O, L94P_Y | I/O, L94P_Y | I/O, L94P_Y | I/O, L94P_Y |
| I/O, VREF Bank 6, L#N_Y | 6 | U1 | XC2S150E, 200E, 300E, 400E, 600E | All | I/O, VREF Bank 6, L67N | I/O, VREF Bank 6, L89N_Y | I/O, VREF Bank 6, L94N_Y | I/O, VREF Bank 6, L94N_Y | I/O, VREF Bank 6, L94N_Y | I/O, VREF Bank 6, L94N_Y |
| I/O | 6 | U2 | XC2S100E | - | I/O, L66P_Y | I/O | I/O | I/O | I/O | I/O |
| I/O, L#P_Y | 6 | U3 | XC2S100E, 150E, 200E, 300E, 400E, 600E | - | I/O, L66N_Y | I/O, L88P_Y | I/O, L93P_Y | I/O, L93P_Y | I/O, L93P_Y | I/O, L93P_Y |
| I/O, L#N_Y | 6 | U4 | XC2S150E, 200E, 300E, 400E, 600E | - | - | I/O, L88N_Y | I/O, L93N_Y | I/O, L93N_Y | I/O, L93N_Y | I/O, L93N_Y |
| I/O | 6 | V1 | - | - | - | - | - | I/O | I/O | I/O |
| I/O, L#P_Y | 6 | W1 | XC2S100E, 200E, 300E, 600E | - | I/O, L65P_Y | I/O, L87P | I/O, L92P_Y | I/O, L92P_Y | I/O, L92P | I/O, L92P_Y |
| I/O, L#N_Y | 6 | V2 | XC2S100E, 200E, 300E, 600E | XC2S200E, 300E, 400E, 600E | I/O, L65N_Y | I/O, L87N | I/O, VREF Bank 6, L92N_Y | I/O, VREF Bank 6, L92N_Y | I/O, VREF Bank 6, L92N | I/O, VREF Bank 6, L92N_Y |
| I/O | 6 | W2 | - | - | I/O | I/O | I/O | I/O | I/O | I/O |
| I/O, L#P_Y | 6 | V3 | XC2S200E, 300E, 400E | - | - | I/O, L86P | I/O, L91P_Y | I/O, L91P_Y | I/O, L91P_Y | I/O, L91P |
| I/O, L#N_Y | 6 | V4 | XC2S200E, 300E, 400E | - | - | I/O, L86N | I/O, L91N_Y | I/O, L91N_Y | I/O, L91N_Y | I/O, L91N |
| I/O | 6 | Y1 | - | - | - | - | - | I/O | I/O | I/O |
| I/O, L#P_YY | 6 | Y2 | All | - | I/O, L64P_YY | I/O, L85P_YY | I/O, L90P_YY | I/O, L90P_YY | I/O, L90P_YY | I/O, L90P_YY |
| I/O, L#N_YY | 6 | W3 | All | - | I/O, L64N_YY | I/O, L85N_YY | I/O, L90N_YY | I/O, L90N_YY | I/O, L90N_YY | I/O, L90N_YY |
| M1 | - | U5 | - | - | M1 | M1 | M1 | M1 | M1 | M1 |

## Additional FG456 Package Pins *(Continued)*

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **VCCO Bank 1 Pins** | | | | | | | | |
| F15 | F16 | G13 | G14 | - | - | - | - | - |
| **VCCO Bank 2 Pins** | | | | | | | | |
| G17 | H17 | J16 | K16 | - | - | - | - | - |
| **VCCO Bank 3 Pins** | | | | | | | | |
| N16 | P16 | R17 | T17 | - | - | - | - | - |
| **VCCO Bank 4 Pins** | | | | | | | | |
| T13 | T14 | U15 | U16 | - | - | - | - | - |
| **VCCO Bank 5 Pins** | | | | | | | | |
| T9 | T10 | U7 | U8 | - | - | - | - | - |
| **VCCO Bank 6 Pins** | | | | | | | | |
| N7 | P7 | R6 | T6 | - | - | - | - | - |
| **VCCO Bank 7 Pins** | | | | | | | | |
| G6 | H6 | J7 | K7 | - | - | - | - | - |
| **GND Pins** | | | | | | | | |
| A1 | A2(2) | A22 | B1(2) | B2 | B21 | C3 | C20 | G11 |
| G12 | J9 | J10 | J11 | J12 | J13 | J14 | K9 | K10 |
| K11 | K12 | K13 | K14 | L7 | L9 | L10 | L11 | L12 |
| L13 | L14 | L16 | M7 | M9 | M10 | M11 | M12 | M13 |
| M14 | M16 | N9 | N10 | N11 | N12 | N13 | N14 | P9 |
| P10 | P11 | P12 | P13 | P14 | T11 | T12 | Y20 | Y3 |
| Y4(2) | AA2 | AA4(2) | AA21 | AA22(2) | AB1 | AB22 | - | - |
| **Not Connected Pins** | | | | | | | | |
| A2(2) | B1(2) | D4(1) | D19(1) | W4(1) | W19(1) | Y4(2) | AA4(2) | AA22(2) |

**Notes:**
1. VCCINT connections in XC2S400E and XC2S600E. No Connects (no internal connection) in XC2S100E, XC2S150E, XC2S200E, and XC2S300E.
2. GND connections in XC2S400E and XC2S600E. No Connects (no internal connection) in XC2S100E, XC2S150E, XC2S200E, and XC2S300E

## FG676 Pinouts (XC2S400E, XC2S600E)

| Pad Name | | Pin | LVDS Async. Output Option | VREF Option | Device-Specific Pinouts | |
|---|---|---|---|---|---|---|
| Function | Bank | | | | XC2S400E | XC2S600E |
| TMS | - | B1 | - | - | TMS | TMS |
| I/O | 7 | D3 | - | - | I/O | I/O |
| I/O, L204P | 7 | C2 | - | - | - | I/O, L204P |
| I/O, L204N | 7 | C1 | - | - | - | I/O, L204N |
| I/O, L203P | 7 | D2 | XC2S600E | - | - | I/O, L203P_Y |
| I/O, L203N | 7 | D1 | XC2S600E | - | I/O | I/O, L203N_Y |
| I/O, L202P_YY | 7 | E2 | All | - | I/O, L202P_YY | I/O, L202P_YY |
| I/O, L202N_YY | 7 | E1 | All | - | I/O, L202N_YY | I/O, L202N_YY |

## FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

| Pad Name | | Pin | LVDS Async. Output Option | VREF Option | Device-Specific Pinouts | |
|---|---|---|---|---|---|---|
| Function | Bank | | | | XC2S400E | XC2S600E |
| I/O, L201P | 7 | E4 | XC2S400E | - | I/O, L201P_Y | I/O, L201P |
| I/O, L201N | 7 | F5 | XC2S400E | - | I/O, L201N_Y | I/O, L201N |
| I/O, VREF Bank 7, L200P | 7 | F4 | XC2S600E | All | I/O, VREF Bank 7, L200P | I/O, VREF Bank 7, L200P_Y |
| I/O, L200N | 7 | F3 | XC2S600E | - | I/O, L200N | I/O, L200N_Y |
| I/O, L199P | 7 | F2 | XC2S600E | - | - | I/O, L199P_Y |
| I/O, L199N | 7 | F1 | XC2S600E | - | I/O | I/O, L199N_Y |
| I/O, L198P | 7 | G6 | XC2S400E | - | I/O, L198P_Y | I/O, L198P |
| I/O, L198N | 7 | G5 | XC2S400E | - | I/O, L198N_Y | I/O, L198N |
| I/O, L197P | 7 | G4 | XC2S600E | - | I/O, L197P | I/O, L197P_Y |
| I/O, L197N | 7 | G3 | XC2S600E | - | I/O, L197N | I/O, L197N_Y |
| I/O, VREF Bank 7, L196P_YY | 7 | G2 | All | All | I/O, VREF Bank 7, L196P_YY | I/O, VREF Bank 7, L196P_YY |
| I/O, L196N_YY | 7 | G1 | All | - | I/O, L196N_YY | I/O, L196N_YY |
| I/O | 7 | H7 | - | - | I/O | I/O |
| I/O, L195P_YY | 7 | H6 | All | - | I/O, L195P_YY | I/O, L195P_YY |
| I/O, L195N_YY | 7 | H5 | All | - | I/O, L195N_YY | I/O, L195N_YY |
| I/O | 7 | J8 | - | - | - | I/O |
| I/O, L194P | 7 | H2 | XC2S400E | - | I/O, L194P_Y | I/O, L194P |
| I/O, L194N | 7 | H1 | XC2S400E | - | I/O, L194N_Y | I/O, L194N |
| I/O, L193P | 7 | J7 | XC2S600E | XC2S600E | I/O | I/O, VREF Bank 7, L193P_Y |
| I/O, L193N | 7 | J6 | XC2S600E | - | - | I/O, L193N_Y |
| I/O | 7 | J5 | - | - | I/O | I/O |
| I/O, L192P_YY | 7 | J4 | All | - | I/O, L192P_YY | I/O, L192P_YY |
| I/O, L192N_YY | 7 | J3 | All | - | I/O, L192N_YY | I/O, L192N_YY |
| I/O | 7 | K5 | - | - | I/O | I/O |
| I/O, VREF Bank 7, L191P_YY | 7 | J2 | All | All | I/O, VREF Bank 7, L191P_YY | I/O, VREF Bank 7, L191P_YY |
| I/O, L191N_YY | 7 | J1 | All | - | I/O, L191N_YY | I/O, L191N_YY |
| I/O, L190P_YY | 7 | K8 | All | - | I/O, L190P_YY | I/O, L190P_YY |
| I/O, L190N_YY | 7 | K7 | All | - | I/O, L190N_YY | I/O, L190N_YY |
| I/O | 7 | K4 | - | - | - | I/O |
| I/O, L189P_YY | 7 | K3 | All | - | I/O, L189P_YY | I/O, L189P_YY |
| I/O, L189N_YY | 7 | K2 | All | - | I/O, L189N_YY | I/O, L189N_YY |
| I/O | 7 | K1 | - | - | - | I/O |

## FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

| Pad Name | | Pin | LVDS Async. Output Option | VREF Option | Device-Specific Pinouts | |
|---|---|---|---|---|---|---|
| Function | Bank | | | | XC2S400E | XC2S600E |
| I/O, VREF Bank 6, L176N | 6 | P9 | XC2S600E | All | I/O, VREF Bank 6, L176N | I/O, VREF Bank 6, L176N_Y |
| I/O, L175P | 6 | R1 | XC2S400E | - | I/O, L175P_Y | I/O, L175P |
| I/O, L175N | 6 | R2 | XC2S400E | - | I/O, L175N_Y | I/O, L175N |
| I/O | 6 | R4 | - | - | - | I/O |
| I/O, L174P_YY | 6 | R5 | All | - | I/O, L174P_YY | I/O, L174P_YY |
| I/O, L174N_YY | 6 | R6 | All | - | I/O, L174N_YY | I/O, L174N_YY |
| I/O | 6 | R7 | - | - | - | I/O |
| I/O, L173P_YY | 6 | R8 | All | - | I/O, L173P_YY | I/O, L173P_YY |
| I/O, VREF Bank 6, L173N_YY | 6 | R9 | All | All | I/O, VREF Bank 6, L173N_YY | I/O, VREF Bank 6, L173N_YY |
| I/O, L172P | 6 | T1 | XC2S600E | - | I/O, L172P | I/O, L172P_Y |
| I/O, L172N | 6 | T2 | XC2S600E | - | I/O, L172N | I/O, L172N_Y |
| I/O | 6 | T3 | - | - | - | I/O |
| I/O, L171P | 6 | T5 | XC2S600E | - | I/O, L171P | I/O, L171P_Y |
| I/O, L171N | 6 | T6 | XC2S600E | - | I/O, L171N | I/O, L171N_Y |
| I/O | 6 | U1 | - | - | - | I/O |
| I/O, L170P | 6 | T7 | XC2S600E | - | I/O, L170P | I/O, L170P_Y |
| I/O, L170N | 6 | T8 | XC2S600E | - | I/O, L170N | I/O, L170N_Y |
| I/O, L169P | 6 | U2 | XC2S400E | - | I/O, L169P_Y | I/O, L169P |
| I/O, L169N | 6 | U3 | XC2S400E | - | I/O, L169N_Y | I/O, L169N |
| I/O | 6 | U7 | - | - | - | I/O |
| I/O, L168P | 6 | U4 | XC2S600E | - | - | I/O, L168P_Y |
| I/O, L168N | 6 | U5 | XC2S600E | - | I/O | I/O, L168N_Y |
| I/O | 6 | U8 | - | - | I/O | I/O |
| I/O, L167P_YY | 6 | V1 | All | - | I/O, L167P_YY | I/O, L167P_YY |
| I/O, L167N_YY | 6 | V2 | All | - | I/O, L167N_YY | I/O, L167N_YY |
| I/O | 6 | V3 | - | - | I/O | I/O |
| I/O, VREF Bank 6, L166P_YY | 6 | V4 | All | All | I/O, VREF Bank 6, L166P_YY | I/O, VREF Bank 6, L166P_YY |
| I/O, L166N_YY | 6 | V5 | All | - | I/O, L166N_YY | I/O, L166N_YY |
| I/O, L165P_YY | 6 | V6 | All | - | I/O, L165P_YY | I/O, L165P_YY |
| I/O, L165N_YY | 6 | V7 | All | - | I/O, L165N_YY | I/O, L165N_YY |
| I/O | 6 | V8 | - | - | - | I/O |
| I/O, L164P | 6 | W1 | XC2S600E | - | I/O, L164P | I/O, L164P_Y |

## FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

| Pad Name | | Pin | LVDS Async. Output Option | VREF Option | Device-Specific Pinouts | |
|---|---|---|---|---|---|---|
| Function | Bank | | | | XC2S400E | XC2S600E |
| I/O, L51N | 2 | D24 | - | - | - | I/O, L51N |
| I/O, L51P | 2 | C25 | - | - | - | I/O, L51P |
| I/O (DIN, D0), L50N_YY | 2 | C26 | All | - | I/O (DIN, D0), L50N_YY | I/O (DIN, D0), L50N_YY |
| I/O (DOUT, BUSY), L50P_YY | 2 | B26 | All | - | I/O (DOUT, BUSY), L50P_YY | I/O (DOUT, BUSY), L50P_YY |
| CCLK | 2 | A25 | - | - | CCLK | CCLK |
| TDO | 2 | C23 | - | - | TDO | TDO |
| TDI | - | D22 | - | - | TDI | TDI |
| | | | | | | |
| I/O ($\overline{CS}$), L49P_YY | 1 | B24 | All | - | I/O ($\overline{CS}$), L49P_YY | I/O ($\overline{CS}$), L49P_YY |
| I/O ($\overline{WRITE}$), L49N_YY | 1 | A24 | All | - | I/O ($\overline{WRITE}$), L49N_YY | I/O ($\overline{WRITE}$), L49N_YY |
| I/O, L48P | 1 | B23 | - | - | I/O | I/O, L48P |
| I/O, L48N | 1 | A23 | - | - | - | I/O, L48N |
| I/O, L47P | 1 | B22 | XC2S400E | - | I/O, L47P_Y | I/O, L47P |
| I/O, L47N | 1 | A22 | XC2S400E | - | I/O, L47N_Y | I/O, L47N |
| I/O, L46P_YY | 1 | D21 | All | - | I/O, L46P_YY | I/O, L46P_YY |
| I/O, L46N_YY | 1 | C21 | All | - | I/O, L46N_YY | I/O, L46N_YY |
| I/O, VREF Bank 1, L45P_YY | 1 | B21 | All | All | I/O, VREF Bank 1, L45P_YY | I/O, VREF Bank 1, L45P_YY |
| I/O, L45N_YY | 1 | A21 | All | - | I/O, L45N_YY | I/O, L45N_YY |
| I/O, L44P | 1 | F20 | XC2S600E | - | - | I/O, L44P_Y |
| I/O, L44N | 1 | E20 | XC2S600E | - | I/O | I/O, L44N_Y |
| I/O, L43P_YY | 1 | D20 | All | - | I/O, L43P_YY | I/O, L43P_YY |
| I/O, L43N_YY | 1 | C20 | All | - | I/O, L43N_YY | I/O, L43N_YY |
| I/O, L42P_YY | 1 | B20 | All | - | I/O, L42P_YY | I/O, L42P_YY |
| I/O, L42N_YY | 1 | A20 | All | - | I/O, L42N_YY | I/O, L42N_YY |
| I/O, VREF Bank 1, L41P_YY | 1 | G19 | All | All | I/O, VREF Bank 1, L41P_YY | I/O, VREF Bank 1, L41P_YY |
| I/O, L41N_YY | 1 | F19 | All | - | I/O, L41N_YY | I/O, L41N_YY |
| I/O | 1 | E19 | - | - | - | I/O |
| I/O, L40P_YY | 1 | B19 | All | - | I/O, L40P_YY | I/O, L40P_YY |
| I/O, L40N_YY | 1 | A19 | All | - | I/O, L40N_YY | I/O, L40N_YY |
| I/O | 1 | H18 | - | - | I/O | I/O |
| I/O, L39P | 1 | G18 | XC2S600E | - | I/O, L39P | I/O, L39P_Y |