AMD Xilinx - XC2S150E-6FT256I Datasheet

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Details	
Product Status	Obsolete
Number of LABs/CLBs	864
Number of Logic Elements/Cells	3888
Total RAM Bits	49152
Number of I/O	182
Number of Gates	150000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s150e-6ft256i

Spartan-IIE FPGA Family: Introduction and Ordering Information

DS077-1 (v3.0) August 9, 2013

Product Specification

Introduction

The Spartan®-IIE Field-Programmable Gate Array family gives users high performance, abundant logic resources, and a rich feature set, all at an exceptionally low price. The seven-member family offers densities ranging from 50,000 to 600,000 system gates, as shown in Table 1. System performance is supported beyond 200 MHz.

Features include block RAM (to 288K bits), distributed RAM (to 221,184 bits), 19 selectable I/O standards, and four DLLs (Delay-Locked Loops). Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

The Spartan-IIE family is a superior alternative to mask-programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary (impossible with ASICs).

Features

- Second generation ASIC replacement technology
  - Densities as high as 15,552 logic cells with up to 600,000 system gates
  - Streamlined features based on Virtex®-E FPGA architecture
  - Unlimited in-system reprogrammability
  - Very low cost
  - Cost-effective 0.15 micron technology
- System level features
  - SelectRAM™ hierarchical memory:
    - 16 bits/LUT distributed RAM
    - Configurable 4K-bit true dual-port block RAM
    - Fast interfaces to external RAM
  - Fully 3.3V PCI compliant to 64 bits at 66 MHz and CardBus compliant
  - Low-power segmented routing architecture
  - Dedicated carry logic for high-speed arithmetic
  - Efficient multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with enable, set, reset
  - Four dedicated DLLs for advanced clock control
    - Eliminate clock distribution delay
    - Multiply, divide, or phase shift
  - Four primary low-skew global clock distribution nets
  - IEEE 1149.1 compatible boundary scan logic
- Versatile I/O and packaging
  - Pb-free package options
  - Low-cost packages available in all densities
  - Family footprint compatibility in common packages
  - 19 high-performance interface standards
    - LVTTL, LVCMOS, HSTL, SSTL, AGP, CTT, GTL
    - LVDS and LVPECL differential I/O
  - Up to 205 differential I/O pairs that can be input, output, or bidirectional
  - Hot swap I/O (CompactPCI friendly)
- Core logic powered at 1.8V and I/Os powered at 1.5V, 2.5V, or 3.3V
- Fully supported by powerful Xilinx® ISE® development system
  - Fully automatic mapping, placement, and routing
  - Integrated with design entry and verification tools
  - Extensive IP library including DSP functions and soft processors

Table 1: **Spartan-IIE FPGA Family Members**

Device	Logic Cells	Typical System Gate Range (Logic and RAM)	CLB Array (R x C)	Total CLBs	Maximum Available User I/O(1)	Maximum Differential I/O Pairs	Distributed RAM Bits	Block RAM Bits
XC2S50E	1,728	23,000 - 50,000	16 x 24	384	182	83	24,576	32K
XC2S100E	2,700	37,000 - 100,000	20 x 30	600	202	86	38,400	40K
XC2S150E	3,888	52,000 - 150,000	24 x 36	864	265	114	55,296	48K
XC2S200E	5,292	71,000 - 200,000	28 x 42	1,176	289	120	75,264	56K
XC2S300E	6,912	93,000 - 300,000	32 x 48	1,536	329	120	98,304	64K
XC2S400E	10,800	145,000 - 400,000	40 x 60	2,400	410	172	153,600	160K
XC2S600E	15,552	210,000 - 600,000	48 x 72	3,456	514	205	221,184	288K

Notes:

1. User I/O counts include the four global clock/user input pins. See details in Table 2, page 5

Optional pull-up and pull-down resistors and an optional weak-keeper circuit are attached to each user I/O pad. Prior to configuration all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but inputs may optionally be pulled up. The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins will float. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. After configuration, clamping diodes are connected to V_{CCO} for LVTTL, PCI, HSTL, SSTL, CTT, and AGP standards.

All Spartan-IIE FPGA IOBs support IEEE 1149.1-compatible boundary scan testing.

Input Path

A buffer in the IOB input path routes the input signal directly to internal logic and through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can used in close proximity to each other. See I/O Banking.

There are optional pull-up and pull-down resistors at each input for use after configuration.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. Each output buffer can source up to 24 mA and sink up to 48 mA. Drive strength and slew rate controls minimize bus transients. The default output driver is LVTTL with 12 mA drive strength and slow slew rate.

In most signaling standards, the output high voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See I/O Banking.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way helps eliminate bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signaling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks (see Figure 5). The pinout tables show the bank affiliation of each I/O (see Pinout Tables, page 53). Each bank has multiple V_{CCO} pins which must be connected to the same voltage. Voltage requirements are determined by the output standards in use.

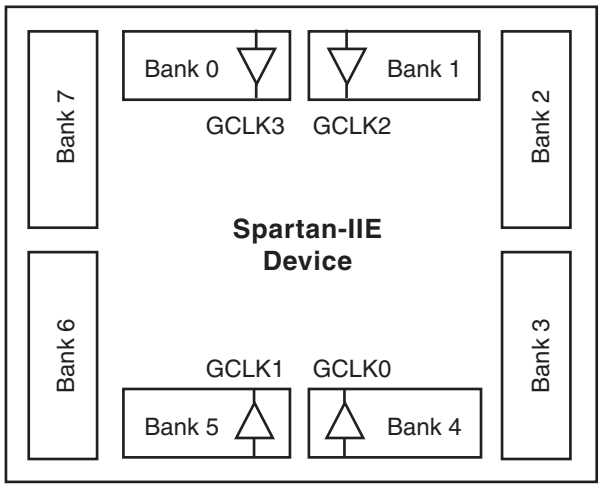


Figure 5: **Spartan-IIE I/O Banks**

In the TQ144 and PQ208 packages, the eight banks have V_{CCO} connected together. Thus, only one V_{CCO} level is allowed in these packages, although different V_{REF} values are allowed in each of the eight banks.

Within a bank, standards may be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 4. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO}. Note that V_{CCO}

Table 8: **Boundary-Scan Instructions *(Continued)***

Boundary-Scan Command	Binary Code[4:0]	Description
INTEST	00111	Enables boundary-scan INTEST operation
USERCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIGHZ	01010	Disables output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions

The public boundary-scan instructions are available prior to configuration, except for USER1 and USER2. After configuration, the public instructions remain available together with any USERCODE instructions installed during the configuration. While the SAMPLE/PRELOAD and BYPASS instructions are available during configuration, it is recommended that boundary-scan operations not be performed during this transitional period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

To facilitate internal scan chains, the User Register provides three outputs (Reset, Update, and Shift) that represent the corresponding states in the boundary-scan internal state machine.

Figure 14 is a diagram of the Spartan-IIE family boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

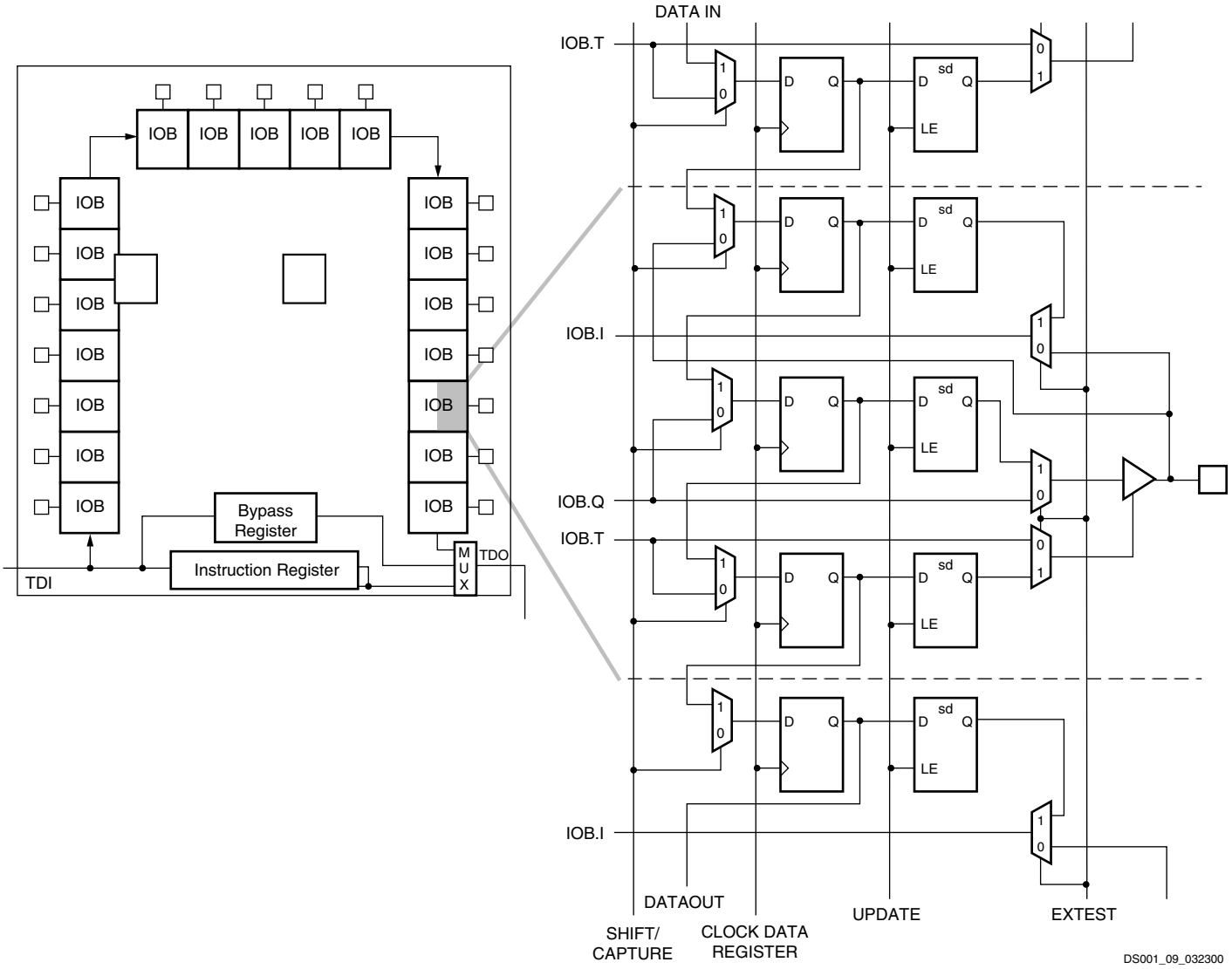


Figure 14: **Spartan-IIE Family Boundary Scan Logic**

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in IOB Output Delay Adjustments for Different Standards(1), page 40.

Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Propagation Delays						
T_{IOOP}	O input to pad	1.0	2.7	1.0	2.9	ns
T_{IOOLP}	O input to pad via transparent latch	1.2	3.1	1.2	3.4	ns
3-state Delays						
T_{IOTHZ}	T input to pad high impedance(1)	0.7	1.7	0.7	1.9	ns
T_{IOTON}	T input to valid data on pad	1.1	2.9	1.1	3.1	ns
$T_{IOTLPHZ}$	T input to pad high impedance via transparent latch(1)	0.8	2.0	0.8	2.2	ns
$T_{IOTLPON}$	T input to valid data on pad via transparent latch	1.2	3.2	1.2	3.4	ns
T_{GTS}	GTS to pad high impedance(1)	1.9	4.6	1.9	4.9	ns
Sequential Delays						
T_{IOCKP}	Clock CLK to pad	0.9	2.8	0.9	2.9	ns
T_{IOCKHZ}	Clock CLK to pad high impedance (synchronous)(1)	0.7	2.0	0.7	2.2	ns
T_{IOCKON}	Clock CLK to valid data on pad (synchronous)	1.1	3.2	1.1	3.4	ns
Setup/Hold Times with Respect to Clock CLK						
T_{IOOCK} / T_{IOCKO}	O input	1.0 / 0	-	1.1 / 0	-	ns
$T_{IOOCECK}$ / $T_{IOCKOCE}$	OCE input	0.7 / 0	-	0.7 / 0	-	ns
$T_{IOSRCKO}$ / $T_{IOCKOSR}$	SR input (OFF)	0.9 / 0	-	1.0 / 0	-	ns
T_{IOTCK} / T_{IOCKT}	3-state setup times, T input	0.6 / 0	-	0.7 / 0	-	ns
$T_{IOTCECK}$ / $T_{IOCKTCE}$	3-state setup times, TCE input	0.6 / 0	-	0.8 / 0	-	ns
$T_{IOSRCKT}$ / $T_{IOCKTSR}$	3-state setup times, SR input (TFF)	0.9 / 0	-	1.0 / 0	-	ns
Set/Reset Delays						
T_{IOSRP}	SR input to pad (asynchronous)	1.2	3.3	1.2	3.5	ns
T_{IOSRHZ}	SR input to pad high impedance (asynchronous)(1)	1.0	2.4	1.0	2.7	ns
T_{IOSRON}	SR input to valid data on pad (asynchronous)	1.4	3.7	1.4	3.9	ns
T_{IOGSRQ}	GSR to pad	3.8	8.5	3.8	9.7	ns

Notes:
1. Three-state turn-off delays should not be adjusted.

IOB Output Delay Adjustments for Different Standards(1)

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade		Units
			-7	-6	
Output Delay Adjustments (Adj)					
T_{OLVTTL_S2}	Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, C_{SL})	LVTTL, Slow, 2 mA	14.7	14.7	ns
T_{OLVTTL_S4}		4 mA	7.5	7.5	ns
T_{OLVTTL_S6}		6 mA	4.8	4.8	ns
T_{OLVTTL_S8}		8 mA	3.0	3.0	ns
T_{OLVTTL_S12}		12 mA	1.9	1.9	ns
T_{OLVTTL_S16}		16 mA	1.7	1.7	ns
T_{OLVTTL_S24}		24 mA	1.3	1.3	ns
T_{OLVTTL_F2}		LVTTL, Fast, 2 mA	13.1	13.1	ns
T_{OLVTTL_F4}		4 mA	5.3	5.3	ns
T_{OLVTTL_F6}		6 mA	3.1	3.1	ns
T_{OLVTTL_F8}		8 mA	1.0	1.0	ns
T_{OLVTTL_F12}		12 mA	0	0	ns
T_{OLVTTL_F16}		16 mA	–0.05	–0.05	ns
T_{OLVTTL_F24}		24 mA	–0.20	–0.20	ns
$T_{OLVCMOS2}$		LVCMOS2	0.09	0.09	ns
$T_{OLVCMOS18}$		LVCMOS18	0.7	0.7	ns
T_{OLVDS}		LVDS	–1.2	–1.2	ns
$T_{OLVPECL}$		LVPECL	–0.41	–0.41	ns
T_{OPCI33_3}		PCI, 33 MHz, 3.3V	2.3	2.3	ns
T_{OPCI66_3}		PCI, 66 MHz, 3.3V	–0.41	–0.41	ns
T_{OGTL}		GTL	0.49	0.49	ns
T_{OGTLP}		GTL+	0.8	0.8	ns
T_{OHSTL_I}		HSTL I	–0.51	–0.51	ns
T_{OHSTL_III}		HSTL III	–0.91	–0.91	ns
T_{OHSTL_IV}		HSTL IV	–1.01	–1.01	ns
T_{OSSTL2_I}		SSTL2 I	–0.51	–0.51	ns
T_{OSSLT2_II}		SSTL2 II	–0.91	–0.91	ns
T_{OSSTL3_I}		SSTL3 I	–0.51	–0.51	ns
T_{OSSTL3_II}		SSTL3 II	–1.01	–1.01	ns
T_{OCTT}		CTT	–0.61	–0.61	ns
T_{OAGP}		AGP	–0.91	–0.91	ns

Notes:

1. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see the tables Constants for Calculating T_{IOOP} and Delay Measurement Methodology, page 41.

Calculation of T_{IOOP} as a Function of Capacitance

T_{IOOP} is the propagation delay from the O Input of the IOB to the pad. The values for T_{IOOP} are based on the standard capacitive load (C_{SL}) for each I/O standard as listed in the table Constants for Calculating T_{IOOP}, below.

For other capacitive loads, use the formulas below to calculate an adjusted propagation delay, T_{IOOP1}.

$$T_{IOOP1} = T_{IOOP} + Adj + (C_{LOAD} - C_{SL}) * F_L$$

Where:

- Adj — is selected from IOB Output Delay Adjustments for Different Standards(1), page 40, according to the I/O standard used
- C_{LOAD} — is the capacitive load for the design
- F_L — is the capacitance scaling factor

Delay Measurement Methodology

Standard	V_L(1)	V_H(1)	Meas. Point	V_{REF} Typ(2)
LVTTL	0	3	1.4	-
LVCMOS2	0	2.5	1.125	-
PCI33_3	Per PCI Spec			-
PCI66_3	Per PCI Spec			-
GTL	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.80
GTL+	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.0
HSTL Class I	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL Class III	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL Class IV	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
SSTL3 I and II	V_{REF} – 1.0	V_{REF} + 1.0	V_{REF}	1.5
SSTL2 I and II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
CTT	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.5
AGP	V_{REF} – (0.2xV_{CCO})	V_{REF} + (0.2xV_{CCO})	V_{REF}	Per AGP Spec
LVDS	1.2 – 0.125	1.2 + 0.125	1.2	
LVPECL	1.6 – 0.3	1.6 + 0.3	1.6	

Notes:

1. Input waveform switches between V_L and V_H.
2. Measurements are made at V_{REF} Typ, Maximum, and Minimum. Worst-case values are reported.
3. I/O parameter measurements are made with the capacitance values shown in the following table, Constants for Calculating T_{IOOP}. Refer to Application Note XAPP179 for appropriate terminations.
4. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

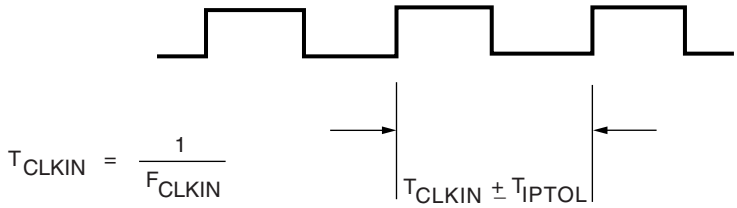
Constants for Calculating T_{IOOP}

Standard	C_{SL}(1) (pF)	F_L (ns/pF)
LVTTL Fast Slew Rate, 2 mA drive	35	0.41
LVTTL Fast Slew Rate, 4 mA drive	35	0.20
LVTTL Fast Slew Rate, 6 mA drive	35	0.13
LVTTL Fast Slew Rate, 8 mA drive	35	0.079
LVTTL Fast Slew Rate, 12 mA drive	35	0.044
LVTTL Fast Slew Rate, 16 mA drive	35	0.043
LVTTL Fast Slew Rate, 24 mA drive	35	0.033
LVTTL Slow Slew Rate, 2 mA drive	35	0.41
LVTTL Slow Slew Rate, 4 mA drive	35	0.20
LVTTL Slow Slew Rate, 6 mA drive	35	0.100
LVTTL Slow Slew Rate, 8 mA drive	35	0.086
LVTTL Slow Slew Rate, 12 mA drive	35	0.058
LVTTL Slow Slew Rate, 16 mA drive	35	0.050
LVTTL Slow Slew Rate, 24 mA drive	35	0.048
LVCMOS2	35	0.041
LVCMOS18	35	0.050
PCI 33 MHz 3.3V	10	0.050
PCI 66 MHz 3.3V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

Notes:

1. I/O parameter measurements are made with the capacitance values shown above. Refer to Application Note XAPP179 for appropriate terminations.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Period Tolerance: the allowed input clock period change in nanoseconds.



Output Jitter: the difference between an ideal reference clock edge and the actual design.

Phase Offset and Maximum Phase Difference

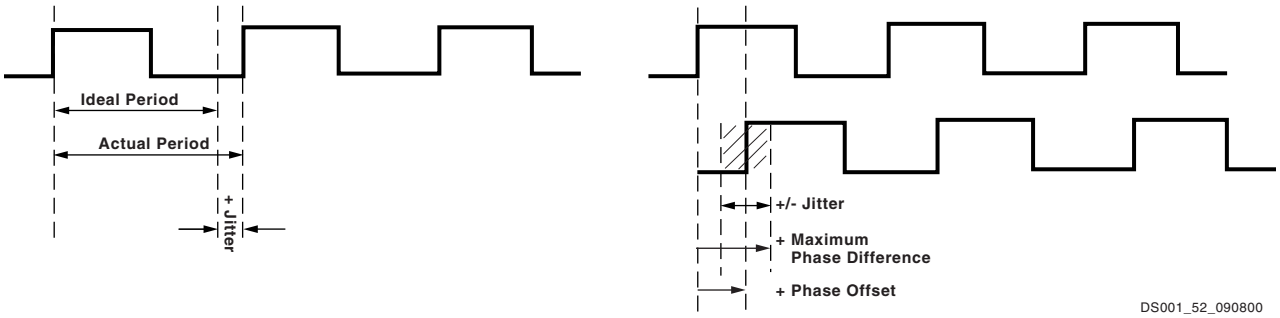


Figure 22: **Period Tolerance and Clock Jitter**

Package Thermal Characteristics

Table 14 provides the thermal characteristics for the various Spartan-II FPGA package offerings. This information is also available using the Thermal Query tool on xilinx.com (www.xilinx.com/cgi-bin/thermal/thermal.pl).

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board (θ_{JB}) value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The "Still Air (0 LFM)" column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 14: **Spartan-IIE Package Thermal Characteristics**

Package	Device	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
TQ144 TQG144	XC2S50E	5.8	N/A	32.3	25.1	21.5	20.1	°C/Watt
	XC2S100E	5.3	N/A	31.4	24.4	20.8	19.6	°C/Watt
PQ208 PQG208	XC2S50E	7.1	N/A	35.1	25.9	22.9	21.2	°C/Watt
	XC2S100E	6.1	N/A	34.2	25.2	22.3	20.7	°C/Watt
	XC2S150E	6.0	N/A	34.1	25.2	22.2	20.6	°C/Watt
	XC2S200E	4.6	N/A	32.4	23.9	21.2	19.6	°C/Watt
	XC2S300E	4.0	N/A	31.6	23.3	20.6	19.1	°C/Watt
FT256 FTG256	XC2S50E	7.3	17.8	27.4	21.6	20.4	20.0	°C/Watt
	XC2S100E	5.8	15.1	25.0	19.5	18.2	17.8	°C/Watt
	XC2S150E	5.7	14.8	24.8	19.3	18.0	17.6	°C/Watt
	XC2S200E	3.9	11.4	21.9	16.6	15.2	14.7	°C/Watt
	XC2S300E	3.2	10.1	20.8	15.6	14.2	13.7	°C/Watt
	XC2S400E	2.5	8.8	19.7	14.5	13.2	12.6	°C/Watt
FG456 FGG456	XC2S100E	8.4	14.9	24.3	19.2	18.1	17.4	°C/Watt
	XC2S150E	8.2	14.6	24.1	19.0	17.9	17.1	°C/Watt
	XC2S200E	6.3	11.6	21.0	16.1	15.0	14.3	°C/Watt
	XC2S300E	5.6	10.4	19.9	15.1	13.9	13.2	°C/Watt
	XC2S400E	3.6	6.5	17.7	11.7	10.5	10.0	°C/Watt
	XC2S600E	2.7	5.0	17.3	11.2	10.0	9.5	°C/Watt
FG676 FGG676	XC2S400E	4.1	7.9	15.6	11.1	9.8	9.2	°C/Watt
	XC2S600E	3.4	6.9	14.5	9.9	8.6	7.9	°C/Watt

Pinout Tables

The following device-specific pinout tables include all packages available for each Spartan-IIE device. They follow the pad locations around the die. In the TQ144 package, all VCCO pins must be connected to the same voltage.

TQ144 Pinouts (XC2S50E and XC2S100E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
GND	-	P1	-	-
TMS	-	P2	-	-
I/O	7	P3	-	-
I/O	7	P4	-	-
I/O, VREF Bank 7	7	P5	-	All
I/O	7	P6	-	-
I/O, L27P	7	P7	XC2S50E	XC2S100E
I/O, L27N	7	P8	XC2S50E	-
GND	-	P9	-	-
I/O, L26P_YY	7	P10	All	-
I/O, L26N_YY	7	P11	All	-
I/O, VREF Bank 7, L25P	7	P12	XC2S50E	All
I/O, L25N	7	P13	XC2S50E	-
I/O	7	P14	-	-
I/O (IRDY)	7	P15	-	-
GND	-	P16	-	-
VCCO	-	P17	-	-
I/O (TRDY)	6	P18	-	-
VCCINT	-	P19	-	-
I/O	6	P20	-	-
I/O, L24P	6	P21	XC2S50E	-
I/O, VREF Bank 6, L24N	6	P22	XC2S50E	All
I/O, L23P_YY	6	P23	All	-
I/O, L23N_YY	6	P24	All	-
GND	-	P25	-	-
I/O, L22P	6	P26	XC2S50E	-

TQ144 Pinouts (XC2S50E and XC2S100E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L22N	6	P27	XC2S50E	XC2S100E
I/O	6	P28	-	-
I/O, VREF Bank 6	6	P29	-	All
I/O	6	P30	-	-
I/O, L21P_YY	6	P31	All	-
I/O, L21N_YY	6	P32	All	-
M1	-	P33	-	-
GND	-	P34	-	-
M0	-	P35	-	-
VCCO	-	P36	-	-
M2	-	P37	-	-
I/O, L20N_YY	5	P38	All	-
I/O, L20P_YY	5	P39	All	-
I/O	5	P40	-	-
I/O, VREF Bank 5	5	P41	-	All
I/O	5	P42	-	-
I/O, L19N_YY	5	P43	All	XC2S100E
I/O, L19P_YY	5	P44	All	-
GND	-	P45	-	-
VCCINT	-	P46	-	-
I/O, L18N_YY	5	P47	All	-
I/O, L18P_YY	5	P48	All	-
I/O, VREF Bank 5	5	P49	-	All
I/O (DLL), L17N	5	P50	-	-
VCCINT	-	P51	-	-
GCK1, I	5	P52	-	-
VCCO	5	P53	-	-
GND	-	P54	-	-
GCK0, I	4	P55	-	-

TQ144 Pinouts (XC2S50E and XC2S100E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O (DLL), L17P	4	P56	-	-
I/O	4	P57	-	-
I/O, VREF Bank 4	4	P58	-	All
I/O, L16N_YY	4	P59	All	-
I/O, L16P_YY	4	P60	All	-
VCCINT	-	P61	-	-
GND	-	P62	-	-
I/O, L15N_YY	4	P63	All	-
I/O, L15P_YY	4	P64	All	XC2S100E
I/O	4	P65	-	-
I/O, VREF Bank 4	4	P66	-	All
I/O	4	P67	-	-
I/O, L14N_YY	4	P68	All	-
I/O, L14P_YY	4	P69	All	-
GND	-	P70	-	-
DONE	3	P71	-	-
VCCO	-	P72	-	-
$\overline{\text{PROGRAM}}$	-	P73	-	-
I/O ($\overline{\text{INIT}}$), L13N_YY	3	P74	All	-
I/O (D7), L13P_YY	3	P75	All	-
I/O	3	P76	-	-
I/O, VREF Bank 3	3	P77	-	All
I/O	3	P78	-	-
I/O, L12N	3	P79	XC2S50E	XC2S100E
I/O (D6), L12P	3	P80	XC2S50E	-
GND	-	P81	-	-
I/O (D5), L11N_YY	3	P82	All	-
I/O, L11P_YY	3	P83	All	-
I/O	3	P84	-	-

TQ144 Pinouts (XC2S50E and XC2S100E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 3, L10N	3	P85	XC2S50E	All
I/O (D4), L10P	3	P86	XC2S50E	-
I/O	3	P87	-	-
VCCINT	-	P88	-	-
I/O (TRDY)	3	P89	-	-
VCCO	-	P90	-	-
GND	-	P91	-	-
I/O (IRDY)	2	P92	-	-
I/O	2	P93	-	-
I/O (D3), L9N	2	P94	XC2S50E	-
I/O, VREF Bank 2, L9P	2	P95	XC2S50E	All
I/O	2	P96	-	-
I/O, L8N_YY	2	P97	All	-
I/O (D2), L8P_YY	2	P98	All	-
GND	-	P99	-	-
I/O (D1), L7N	2	P100	XC2S50E	-
I/O, L7P	2	P101	XC2S50E	XC2S100E
I/O	2	P102	-	-
I/O, VREF Bank 2	2	P103	-	All
I/O	2	P104	-	-
I/O (DIN, D0), L6N_YY	2	P105	All	-
I/O (DOUT, BUSY), L6P_YY	2	P106	All	-
CCLK	2	P107	-	-
VCCO	-	P108	-	-
TDO	2	P109	-	-
GND	-	P110	-	-
TDI	-	P111	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 6, L39P	6	P45	XC2S100E, 150E	All
I/O, L39N	6	P46	XC2S100E, 150E	-
I/O	6	P47	-	XC2S200E, 300E
I/O, L38P_YY	6	P48	All	-
I/O, L38N_YY	6	P49	All	-
M1	-	P50	-	-
GND	-	P51	-	-
M0	-	P52	-	-
VCCO	-	P53	-	-
M2	-	P54	-	-
I/O, L37N_YY	5	P55	All	-
I/O, L37P_YY	5	P56	All	-
I/O	5	P57	-	XC2S200E, 300E
I/O	5	P58	-	-
I/O, VREF Bank 5, L36N_YY	5	P59	All	All
I/O, L36P_YY	5	P60	All	-
I/O, L35N	5	P61	XC2S50E, 100E, 300E	-
I/O, L35P	5	P62	XC2S50E, 100E, 300E	-
I/O, L34N	5	P63	XC2S50E, 100E, 200E, 300E	XC2S100E, 150E, 200E, 300E
I/O, L34P	5	P64	XC2S50E, 100E, 200E, 300E	-
GND	-	P65	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
VCCO	-	P66	-	-
VCCINT	-	P67	-	-
I/O, L33N	5	P68	XC2S50E, 100E, 200E, 300E	-
I/O, L33P	5	P69	XC2S50E, 100E, 200E, 300E	-
I/O	5	P70	-	-
I/O, L32N	5	P71	XC2S100E, 150E	-
GND	-	P72	-	-
I/O, VREF Bank 5, L32P	5	P73	XC2S100E, 150E	All
I/O	5	P74	-	-
I/O (DLL), L31N	5	P75	-	-
VCCINT	-	P76	-	-
GCK1, I	5	P77	-	-
VCCO	-	P78	-	-
GND	-	P79	-	-
GCK0, I	4	P80	-	-
I/O (DLL), L31P	4	P81	-	-
I/O	4	P82	-	-
I/O, L30N	4	P83	XC2S50E, 200E, 300E	-
I/O, VREF Bank 4, L30P	4	P84	XC2S50E, 200E, 300E	All
GND	-	P85	-	-
I/O, L29N	4	P86	XC2S50E, 200E, 300E	-
I/O, L29P	4	P87	XC2S50E, 200E, 300E	-
I/O, L28N	4	P88	XC2S50E, 100E, 200E, 300E	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L28P	4	P89	XC2S50E, 100E, 200E, 300E	-
VCCINT	-	P90	-	-
VCCO	-	P91	-	-
GND	-	P92	-	-
I/O, L27N	4	P93	XC2S50E, 100E, 200E, 300E	-
I/O, L27P	4	P94	XC2S50E, 100E, 200E, 300E	XC2S100E, 150E, 200E, 300E
I/O	4	P95	-	-
I/O	4	P96	-	-
I/O, L26N_YY	4	P97	All	-
I/O, VREF Bank 4, L26P_YY	4	P98	All	All
I/O	4	P99	-	-
I/O	4	P100	-	XC2S200E, 300E
I/O, L25N_YY	4	P101	All	-
I/O, L25P_YY	4	P102	All	-
GND	-	P103	-	-
DONE	3	P104	-	-
VCCO	-	P105	-	-
$\overline{\text{PROGRAM}}$	-	P106	-	-
I/O ($\overline{\text{INIT}}$), L24N_YY	3	P107	All	-
I/O (D7), L24P_YY	3	P108	All	-
I/O	3	P109	-	XC2S200E, 300E
I/O	3	P110	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 3, L23N	3	P111	XC2S50E, 150E, 200E, 300E	All
I/O, L23P	3	P112	XC2S50E, 150E, 200E, 300E	-
I/O	3	P113	-	-
I/O	3	P114	-	-
I/O, L22N	3	P115	XC2S50E, 300E	XC2S100E, 150E, 200E, 300E
I/O (D6), L22P	3	P116	XC2S50E, 300E	-
GND	-	P117	-	-
VCCO	-	P118	-	-
VCCINT	-	P119	-	-
I/O (D5), L21N_YY	3	P120	All	-
I/O, L21P_YY	3	P121	All	-
I/O, L20N_YY	3	P122	All	-
I/O, L20P_YY	3	P123	All	-
GND	-	P124	-	-
I/O, VREF Bank 3, L19N	3	P125	XC2S50E, 300E	All
I/O (D4), L19P	3	P126	XC2S50E, 300E	-
I/O	3	P127	-	-
VCCINT	-	P128	-	-
I/O (TRDY)	3	P129	-	-
VCCO	-	P130	-	-
GND	-	P131	-	-
I/O (IRDY), L18N_YY	2	P132	All	-
I/O, L18P_YY	2	P133	All	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
TMS	-	B1	-	-
I/O	7	D3	-	-
I/O, L83P	7	C2	XC2S100E, 150E	-
I/O, L83N	7	C1	XC2S100E, 150E	XC2S200E, 300E, 400E
I/O, L82P_YY	7	D2	All	-
I/O, L82N_YY	7	D1	All	-
I/O, VREF Bank 7, L81P	7	E3	XC2S50E, 150E, 200E, 300E, 400E	All
I/O, L81N	7	E4	XC2S50E, 150E, 200E, 300E, 400E	-
I/O, L80P	7	E2	XC2S200E, 400E	-
I/O, L80N	7	E1	XC2S200E, 400E	-
I/O, L79P	7	F4	XC2S50E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L79N	7	F3	XC2S50E, 300E, 400E	-
I/O, L78P_YY	7	F2	All	-
I/O, L78N_YY	7	F1	All	-
I/O, L77P	7	F5	XC2S100E, 150E	-
I/O, L77N	7	G5	XC2S100E, 150E	-
I/O, L76P_YY	7	G3	All	-
I/O, L76N_YY	7	G4	All	-
I/O, VREF Bank 7, L75P	7	G2	XC2S50E, 300E, 400E	All
I/O, L75N	7	G1	XC2S50E, 300E, 400E	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L74P	7	H4	XC2S100E, 150E, 200E	-
I/O, L74N	7	H3	XC2S100E, 150E, 200E	XC2S400E
I/O, L73P_YY	7	H2	All	-
I/O (IRDY), L73N_YY	7	H1	All	-
I/O (TRDY)	6	J4	-	-
I/O, L72P	6	J2	XC2S100E, 150E, 200E, 400E	XC2S400E
I/O, L72N	6	J3	XC2S100E, 150E, 200E, 400E	-
I/O, L71P	6	J1	XC2S50E, 300E, 400E	-
I/O, VREF Bank 6, L71N	6	K1	XC2S50E, 300E, 400E	All
I/O, L70P_YY	6	K2	All	-
I/O, L70N_YY	6	K3	All	-
I/O, L69P	6	L1	XC2S100E, 150E, 400E	-
I/O, L69N	6	L2	XC2S100E, 150E, 400E	-
I/O, L68P_YY	6	K4	All	-
I/O, L68N_YY	6	K5	All	-
I/O, L67P	6	L3	XC2S50E, 300E, 400E	-
I/O, L67N	6	M2	XC2S50E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L66P	6	M1	XC2S150E, 200E, 400E	-
I/O, L66N	6	N1	XC2S150E, 200E, 400E	-

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
TMS	-	E4	-	-	TMS	TMS	TMS	TMS	TMS	TMS
I/O	7	D3	XC2S150E	-	I/O	I/O, L113P_Y	I/O	I/O	I/O	I/O
I/O	7	C2	-	-	-	-	-	I/O	I/O	I/O
I/O	7	C1	XC2S150E	-	-	I/O, L113N_Y	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	D2	XC2S150E, 200E, 300E, 400E	-	-	I/O, L112P_Y	I/O, L119P_Y	I/O, L119P_Y	I/O, L119P_Y	I/O, L119P
I/O, L#N_Y	7	D1	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L112N_Y	I/O, L119N_Y	I/O, L119N_Y	I/O, L119N_Y	I/O, L119N
I/O, L#P_Y	7	E2	XC2S100E, 200E, 300E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L85P_Y	I/O, L111P	I/O, VREF Bank 7, L118P_Y	I/O, VREF Bank 7, L118P_Y	I/O, VREF Bank 7, L118P	I/O, VREF Bank 7, L118P_Y
I/O, L#N_Y	7	E3	XC2S100E, 200E, 300E, 600E	-	I/O, L85N_Y	I/O, L111N	I/O, L118N_Y	I/O, L118N_Y	I/O, L118N	I/O, L118N_Y
I/O	7	E1	-	-	-	-	-	I/O	I/O	I/O
I/O	7	F5	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	F4	XC2S100E, 200E, 300E, 600E	-	I/O, L84P_Y	I/O, L110P	I/O, L117P_Y	I/O, L117P_Y	I/O, L117P	I/O, L117P_Y
I/O, L#N_Y	7	F3	XC2S100E, 200E, 300E, 600E	-	I/O, L84N_Y	I/O, L110N	I/O, L117N_Y	I/O, L117N_Y	I/O, L117N	I/O, L117N_Y
I/O, VREF Bank 7, L#P_Y	7	F2	XC2S150E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 7, L83P	I/O, VREF Bank 7, L109P_Y	I/O, VREF Bank 7, L116P_Y	I/O, VREF Bank 7, L116P_Y	I/O, VREF Bank 7, L116P_Y	I/O, VREF Bank 7, L116P_Y
I/O, L#N_Y	7	F1	XC2S150E, 200E, 300E, 400E, 600E	-	I/O, L83N	I/O, L109N_Y	I/O, L116N_Y	I/O, L116N_Y	I/O, L116N_Y	I/O, L116N_Y
I/O	7	G5	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	G4	XC2S150E, 200E, 300E, 400E	-	-	I/O, L108P_Y	I/O, L115P_Y	I/O, L115P_Y	I/O, L115P_Y	I/O, L115P
I/O, L#N_Y	7	G3	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L108N_Y	I/O, L115N_Y	I/O, L115N_Y	I/O, L115N_Y	I/O, L115N
I/O, L#P_Y	7	G2	XC2S100E, 150E, 300E, 600E	XC2S600E	I/O, L82P_Y	I/O, L107P_Y	I/O, L114P	I/O, L114P_Y	I/O, L114P	I/O, VREF Bank 7, L114P_Y
I/O, L#N_Y	7	G1	XC2S100E, 150E, 300E, 600E	-	I/O, L82N_Y	I/O, L107N_Y	I/O, L114N	I/O, L114N_Y	I/O, L114N	I/O, L114N_Y

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O, L#N	3	V19	XC2S150E, 200E, 300E, 400E	-	-	I/O, L54N_Y	I/O, L58N_Y	I/O, L58N_Y	I/O, L58N_Y	I/O, L58N
I/O, L#P	3	V20	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L54P_Y	I/O, L58P_Y	I/O, L58P_Y	I/O, L58P_Y	I/O, L58P
I/O, L#N	3	V22	XC2S100E, 200E, 300E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L40N_Y	I/O, L53N	I/O, VREF Bank 3, L57N_Y	I/O, VREF Bank 3, L57N_Y	I/O, VREF Bank 3, L57N	I/O, VREF Bank 3, L57N_Y
I/O, L#P	3	U22	XC2S100E, 200E, 300E, 600E	-	I/O, L40P_Y	I/O, L53P	I/O, L57P_Y	I/O, L57P_Y	I/O, L57P	I/O, L57P_Y
I/O	3	U21	-	-	-	-	-	I/O	I/O	I/O
I/O	3	U20	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N	3	U18	XC2S100E, 200E, 300E, 600E	-	I/O, L39N_Y	I/O, L52N	I/O, L56N_Y	I/O, L56N_Y	I/O, L56N	I/O, L56N_Y
I/O, L#P	3	U19	XC2S100E, 200E, 300E, 600E	-	I/O, L39P_Y	I/O, L52P	I/O, L56P_Y	I/O, L56P_Y	I/O, L56P	I/O, L56P_Y
I/O, VREF Bank 3, L#N	3	T21	XC2S150E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 3, L38N	I/O, VREF Bank 3, L51N_Y	I/O, VREF Bank 3, L55N_Y	I/O, VREF Bank 3, L55N_Y	I/O, VREF Bank 3, L55N_Y	I/O, VREF Bank 3, L55N_Y
I/O, L#P	3	T22	XC2S150E, 200E, 300E, 400E, 600E	-	I/O, L38P	I/O, L51P_Y	I/O, L55P_Y	I/O, L55P_Y	I/O, L55P_Y	I/O, L55P_Y
I/O	3	T20	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N	3	T18	XC2S150E, 200E, 300E, 400E	-	-	I/O, L50N_Y	I/O, L54N_Y	I/O, L54N_Y	I/O, L54N_Y	I/O, L54N
I/O, L#P	3	T19	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L50P_Y	I/O, L54P_Y	I/O, L54P_Y	I/O, L54P_Y	I/O, L54P
I/O, L#N	3	R21	XC2S100E, 150E, 300E, 600E	XC2S600E	I/O, L37N_Y	I/O, L49N_Y	I/O, L53N	I/O, L53N_Y	I/O, L53N	I/O, VREF Bank 3, L53N_Y
I/O, L#P	3	R22	XC2S100E, 150E, 300E, 600E	-	I/O, L37P_Y	I/O, L49P_Y	I/O, L53P	I/O, L53P_Y	I/O, L53P	I/O, L53P_Y
I/O	3	R20	-	-	-	-	-	I/O	I/O	I/O
I/O, VREF Bank 3, L#N	3	R18	XC2S300E, 400E, 600E	All	I/O, VREF Bank 3, L36N	I/O, VREF Bank 3, L48N	I/O, VREF Bank 3, L52N	I/O, VREF Bank 3, L52N_Y	I/O, VREF Bank 3, L52N_Y	I/O, VREF Bank 3, L52N_Y
I/O (D6), L#P	3	R19	XC2S300E, 400E, 600E	-	I/O (D6), L36P	I/O (D6), L48P	I/O (D6), L52P	I/O (D6), L52P_Y	I/O (D6), L52P_Y	I/O (D6), L52P_Y
I/O (D5), L#N_YY	3	P22	All	-	I/O (D5), L35N_YY	I/O (D5), L47N_YY	I/O (D5), L51N_YY	I/O (D5), L51N_YY	I/O (D5) L51N_YY	I/O (D5), L51N_YY
I/O, L#P_YY	3	P21	All	-	I/O, L35P_YY	I/O, L47P_YY	I/O, L51P_YY	I/O, L51P_YY	I/O, L51P_YY	I/O, L51P_YY

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O	3	P20	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#N	3	P18	XC2S150E, 200E, 300E, 400E	-	-	I/O, L46N_Y	I/O, L50N_Y	I/O, L50N_Y	I/O, L50N_Y	I/O, L50N
I/O, L#P	3	P19	XC2S100E, 150E, 200E, 300E, 400E	-	I/O, L34N_Y	I/O, L46P_Y	I/O, L50P_Y	I/O, L50P_Y	I/O, L50P_Y	I/O, L50P
I/O, L#N	3	N22	XC2S100E, 150E, 200E, 300E, 600E	-	I/O, L34P_Y	I/O, L45N_Y	I/O, L49N_Y	I/O, L49N_Y	I/O, L49N	I/O, L49N_Y
I/O, L#P	3	N21	XC2S150E, 200E, 300E, 600E	-	-	I/O, L45P_Y	I/O, L49P_Y	I/O, L49P_Y	I/O, L49P	I/O, L49P_Y
I/O	3	P17	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#N	3	N19	XC2S100E, 150E, 200E, 300E, 600E(1)	-	I/O, L33N_YY	I/O, L44N_YY	I/O, L48N_YY	I/O, L48N_YY	I/O, L48N	I/O, L48N_Y
I/O, L#P	3	N20	XC2S100E, 150E, 200E, 300E, 600E(1)	-	I/O, L33P_YY	I/O, L44P_YY	I/O, L48P_YY	I/O, L48P_YY	I/O, L48P	I/O, L48P_Y
I/O, VREF Bank 3, L#N	3	N18	XC2S300E, 400E, 600E	All	I/O, VREF Bank 3, L32N	I/O, VREF Bank 3, L43N	I/O, VREF Bank 3, L47N	I/O, VREF Bank 3, L47N_Y	I/O, VREF Bank 3, L47N_Y	I/O, VREF Bank 3, L47N_Y
I/O (D4), L#P	3	N17	XC2S300E, 400E, 600E	-	I/O (D4), L32P	I/O (D4), L43P	I/O (D4), L47P	I/O (D4), L47P_Y	I/O (D4), L47P_Y	I/O (D4), L47P_Y
I/O	3	M22	-	-	-	-	-	I/O	I/O	I/O
I/O, L#N	3	M20	XC2S300E, 400E	-	-	-	I/O, L46N	I/O, L46N_Y	I/O, L46N_Y	I/O, L46N
I/O, L#P	3	M21	XC2S100E, 150E, 300E, 400E	-	I/O, L31N_Y	I/O, L42N_Y	I/O, L46P	I/O, L46P_Y	I/O, L46P_Y	I/O, L46P
I/O, L#N	3	M18	XC2S100E, 150E, 200E, 300E, 600E	XC2S400E, 600E	I/O, L31P_Y	I/O, L42P_Y	I/O, L45N_Y	I/O, L45N_Y	I/O, VREF Bank 3, L45N	I/O, VREF Bank 3, L45N_Y
I/O, L#P	3	M19	XC2S200E, 300E, 600E	-	-	I/O	I/O, L45P_Y	I/O, L45P_Y	I/O, L45P	I/O, L45P_Y
I/O	3	M17	-	-	-	-	-	I/O	I/O	I/O
I/O (TRDY)	3	L22	-	-	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)
I/O (IRDY), L#N_YY	2	L21	All	-	I/O (IRDY), L30N_YY	I/O (IRDY), L41N_YY	I/O (IRDY), L44N_YY	I/O (IRDY), L44N_YY	I/O (IRDY), L44N_YY	I/O (IRDY), L44N_YY
I/O, L#P_YY	2	L20	All	-	I/O, L30P_YY	I/O, L41P_YY	I/O, L44P_YY	I/O, L44P_YY	I/O, L44P_YY	I/O, L44P_YY
I/O	2	L19	-	-	-	-	-	I/O	I/O	I/O
I/O, L#N	2	L18	XC2S200E, 300E, 600E	-	-	I/O	I/O, L43N_Y	I/O, L43N_Y	I/O, L43N	I/O, L43N_Y

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O, L#P	2	L17	XC2S100E, 150E, 200E, 300E, 600E	XC2S400E, 600E	I/O, L29N_Y	I/O, L40N_Y	I/O, L43P_Y	I/O, L43P_Y	I/O, VREF Bank 2, L43P	I/O, VREF Bank 2, L43P_Y
I/O, L#N	2	K22	XC2S100E, 150E, 300E, 400E	-	I/O, L29P_Y	I/O, L40P_Y	I/O, L42N	I/O, L42N_Y	I/O, L42N_Y	I/O, L42N
I/O, L#P	2	K21	XC2S300E, 400E	-	-	-	I/O, L42P	I/O, L42P_Y	I/O, L42P_Y	I/O, L42P
I/O	2	K20	-	-	-	-	-	I/O	I/O	I/O
I/O (D3)	2	K19	-	-	I/O (D3)	I/O (D3), L39N	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)
I/O, VREF Bank 2, L#N	2	K18	XC2S100E, 200E, 400E	All	I/O, VREF Bank 2, L28N_Y	I/O, VREF Bank 2, L39P	I/O, VREF Bank 2, L41N_Y	I/O, VREF Bank 2, L41N	I/O, VREF Bank 2, L41N_Y	I/O, VREF Bank 2, L41N
I/O, L#P	2	K17	XC2S100, 150E, 200E, 400E	-	I/O, L28P_Y	I/O, L38N_Y	I/O, L41P_Y	I/O, L41P	I/O, L41P_Y	I/O, L41P
I/O, L#N	2	J22	XC2S150E, 300E, 600E	-	I/O	I/O, L38P_Y	I/O, L40N	I/O, L40N_Y	I/O, L40N	I/O, L40N_Y
I/O, L#P	2	J21	XC2S300E, 600E	-	-	-	I/O, L40P	I/O, L40P_Y	I/O, L40P	I/O, L40P_Y
I/O, L#N	2	J20	XC2S150E, 200E, 300E, 600E	-	-	I/O, L37N_Y	I/O, L39N_Y	I/O, L39N_Y	I/O, L39N	I/O, L39N_Y
I/O, L#P	2	J19	XC2S100E, 150E, 200E, 300E, 600E	-	I/O, L27N_Y	I/O, L37P_Y	I/O, L39P_Y	I/O, L39P_Y	I/O, L39P	I/O, L39P_Y
I/O	2	H22	XC2S100E, 150E	-	I/O, L27P_Y	I/O, L36N_Y	I/O	I/O	I/O	I/O
I/O, L#N	2	J18	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L36P_Y	I/O, L38N_Y	I/O, L38N_Y	I/O, L38N_Y	I/O, L38N_Y
I/O, L#P	2	J17	XC2S200E, 300E, 400E, 600E	-	-	-	I/O, L38P_Y	I/O, L38P_Y	I/O, L38P_Y	I/O, L38P_Y
I/O, L#N	2	H21	XC2S150E, 200E, 300E, 400E, 600E	-	I/O	I/O, L35N_Y	I/O, L37N_Y	I/O, L37N_Y	I/O, L37N_Y	I/O, L37N_Y
I/O (D2), L#P	2	H20	XC2S150E, 200E, 300E, 400E, 600E	-	I/O (D2)	I/O (D2), L35P_Y	I/O (D2), L37P_Y	I/O (D2), L37P_Y	I/O (D2), L37P_Y	I/O (D2), L37P_Y
I/O (D1), L#N	2	H19	XC2S300E, 400E, 600E	-	I/O (D1), L26N	I/O (D1), L34N	I/O (D1), L36N	I/O (D1), L36N_Y	I/O (D1), L36N_Y	I/O (D1), L36N_Y
I/O, VREF Bank 2, L#P	2	H18	XC2S300E, 400E, 600E	All	I/O, VREF Bank 2, L26P	I/O, VREF Bank 2, L34P	I/O, VREF Bank 2, L36P	I/O, VREF Bank 2, L36P_Y	I/O, VREF Bank 2, L36P_Y	I/O, VREF Bank 2, L36P_Y
I/O	2	G22	-	-	-	-	-	I/O	I/O	I/O
I/O	2	F22	-	-	I/O	I/O	I/O	I/O	I/O	I/O

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O	4	AC18	-	-	I/O	I/O
I/O, VREF Bank 4, L114N	4	AB18	-	All	I/O, VREF Bank 4, L114N	I/O, VREF Bank 4, L114N
I/O, L114P	4	AA18	-	-	I/O, L114P	I/O, L114P
I/O, L113N	4	Y18	-	-	I/O, L113N	I/O, L113N
I/O, L113P	4	W18	-	-	I/O, L113P	I/O, L113P
I/O	4	AB19	-	-	I/O	I/O
I/O, L112N	4	AF19	XC2S600E	-	I/O	I/O, L112N_Y
I/O, L112P	4	AE19	XC2S600E	XC2S600E	-	I/O, VREF Bank 4, L112P_Y
I/O, L111N	4	AA19	XC2S600E	-	I/O, L111N	I/O, L111N_Y
I/O, L111P	4	Y19	XC2S600E	-	I/O, L111P	I/O, L111P_Y
I/O	4	AF20	-	-	-	I/O
I/O, L110N	4	AE20	XC2S600E	-	I/O, L110N	I/O, L110N_Y
I/O, L110P	4	AD20	XC2S600E	-	I/O, L110P	I/O, L110P_Y
I/O	4	AC20	-	-	I/O	I/O
I/O, L109N_YY	4	AB20	All	-	I/O, L109N_YY	I/O, L109N_YY
I/O, VREF Bank 4, L109P_YY	4	AA20	All	All	I/O, VREF Bank 4, L109P_YY	I/O, VREF Bank 4, L109P_YY
I/O	4	Y20	-	-	I/O	I/O
I/O, L108N	4	AF21	-	-	I/O, L108N	I/O, L108N
I/O, L108P	4	AE21	-	-	I/O, L108P	I/O, L108P
I/O, L107N	4	AD21	-	-	I/O, L107N	I/O, L107N
I/O, L107P	4	AC21	-	-	I/O, L107P	I/O, L107P
I/O	4	AC22	-	-	-	I/O
I/O, L106N_YY	4	AF22	All	-	I/O, L106N_YY	I/O, L106N_YY
I/O, VREF Bank 4, L106P_YY	4	AE22	All	All	I/O, VREF Bank 4, L106P_YY	I/O, VREF Bank 4, L106P_YY
I/O, L105N_YY	4	AB21	All	-	I/O, L105N_YY	I/O, L105N_YY
I/O, L105P_YY	4	AA21	All	-	I/O, L105P_YY	I/O, L105P_YY
I/O, L104N_YY	4	AF23	All	-	I/O, L104N_YY	I/O, L104N_YY
I/O, L104P_YY	4	AE23	All	-	I/O, L104P_YY	I/O, L104P_YY
I/O, L103N	4	AD23	XC2S600E	-	I/O	I/O, L103N_Y
I/O, L103P	4	AE24	XC2S600E	-	-	I/O, L103P_Y
I/O, L102N_YY	4	AF24	All	-	I/O, L102N_YY	I/O, L102N_YY
I/O, L102P_YY	4	AF25	All	-	I/O, L102P_YY	I/O, L102P_YY

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L2N_YY	0	E5	All	-	I/O, L2N_YY	I/O, L2N_YY
I/O, L1P_YY	0	B4	All	-	I/O, L1P_YY	I/O, L1P_YY
I/O, L1N_YY	0	C4	All	-	I/O, L1N_YY	I/O, L1N_YY
I/O, L0P	0	A3	XC2S600E	-	I/O	I/O, L0P_Y
I/O, L0N	0	B3	XC2S600E	-	-	I/O, L0N_Y
I/O	0	A4	-	-	I/O	I/O
TCK	-	A2	-	-	TCK	TCK

FG676 Differential Clock Pins

Clock	Bank	P Input		N Input	
		Pin	Name	Pin	Name
GCK0	4	AF14	GCK0, I	AE14	I/O (DLL), L126P
GCK1	5	AF13	GCK1, I	AE13	I/O (DLL), L126N
GCK2	1	A14	GCK2, I	B14	I/O (DLL), L23P
GCK3	0	A13	GCK3, I	B13	I/O (DLL), L23N

Additional FG676 Package Pins

VCCINT Pins						
H8	H19	J9	J18	K10	K11	K16
K17	L10	L17	T10	T17	U10	U11
U16	U17	V9	V18	W8	W19	-
VCCO Bank 0 Pins						
C5	C8	D11	J10	J11	K12	K13
VCCO Bank 1 Pins						
C19	C22	D16	J16	J17	K14	K15
VCCO Bank 2 Pins						
E24	H24	K18	L18	L23	M17	N17
VCCO Bank 3 Pins						
P17	R17	T18	T23	U18	W24	AB24
VCCO Bank 4 Pins						
U14	U15	V16	V17	AC16	AD19	AD22
VCCO Bank 5 Pins						
U12	U13	V10	V11	AC11	AD5	AD8
VCCO Bank 6 Pins						
P10	R10	T4	T9	U9	W3	AB3
VCCO Bank 7 Pins						
H3	K9	L4	L9	M10	N10	E3