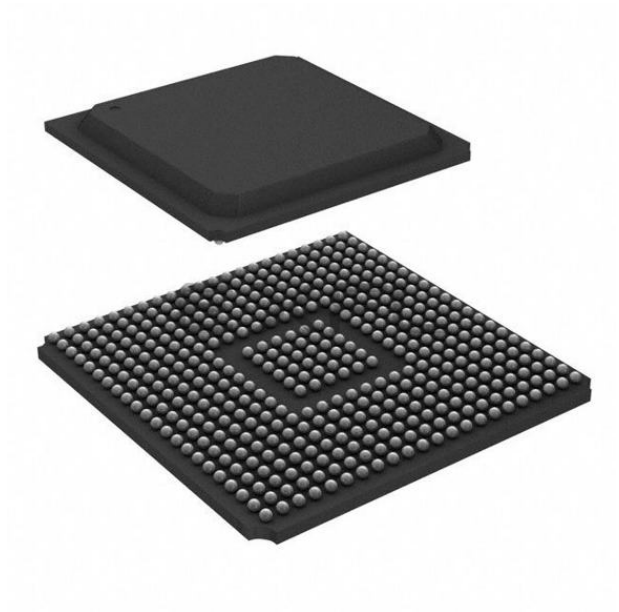
AMD Xilinx - XC2S200E-6FG456C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1176
Number of Logic Elements/Cells	5292
Total RAM Bits	57344
Number of I/O	289
Number of Gates	200000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s200e-6fg456c

Table 7 shows the depth and width aspect ratios for the block RAM.

Table 7: **Block RAM Port Aspect Ratios**

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

The Spartan-IIE FPGA block RAM also includes dedicated routing to provide an efficient interface with both CLBs and other block RAMs. See Xilinx Application Note XAPP173 for more information on block RAM.

Programmable Routing

It is the longest delay path that limits the speed of any design. Consequently, the Spartan-IIE FPGA routing architecture and its place-and-route software were defined jointly to minimize long-path delays and yield the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

The software automatically uses the best available routing based on user timing requirements. The details are provided here for reference.

Local Routing

The local routing resources, as shown in Figure 9, provide the following three types of connections:

- Interconnections among the LUTs, flip-flops, and General Routing Matrix (GRM), described below.
- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM

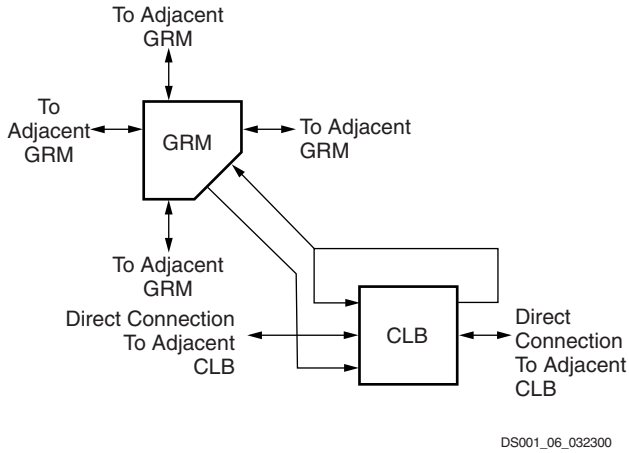


Figure 9: **Spartan-IIE Local Routing**

General Purpose Routing

Most Spartan-IIE FPGA signals are routed on the general purpose routing, and consequently, the majority of interconnect resources are associated with this level of the routing hierarchy. The general routing resources are located in horizontal and vertical routing channels associated with the rows and columns of CLBs. The general-purpose routing resources are listed below.

- Adjacent to each CLB is a General Routing Matrix (GRM). The GRM is the switch matrix through which horizontal and vertical routing resources connect, and is also the means by which the CLB gains access to the general purpose routing.
- 24 single-length lines route GRM signals to adjacent GRMs in each of the four directions.
- 96 buffered Hex lines route GRM signals to other GRMs six blocks away in each one of the four directions. Organized in a staggered pattern, Hex lines may be driven only at their endpoints. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source). One third of the Hex lines are bidirectional, while the remaining ones are unidirectional.
- 12 Longlines are buffered, bidirectional wires that distribute signals across the device quickly and efficiently. Vertical Longlines span the full height of the device, and horizontal ones span the full width of the device.

I/O Routing

Spartan-IIE devices have additional routing resources around their periphery that form an interface between the CLB array and the IOBs. This additional routing, called the VersaRing™ routing, facilitates pin-swapping and pin-locking, such that logic redesigns can adapt to existing PCB layouts. Time-to-market is reduced, since PCBs and other system components can be manufactured while the logic design is still in progress.

Table 8: **Boundary-Scan Instructions *(Continued)***

Boundary-Scan Command	Binary Code[4:0]	Description
INTEST	00111	Enables boundary-scan INTEST operation
USERCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIGHZ	01010	Disables output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions

The public boundary-scan instructions are available prior to configuration, except for USER1 and USER2. After configuration, the public instructions remain available together with any USERCODE instructions installed during the configuration. While the SAMPLE/PRELOAD and BYPASS instructions are available during configuration, it is recommended that boundary-scan operations not be performed during this transitional period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

To facilitate internal scan chains, the User Register provides three outputs (Reset, Update, and Shift) that represent the corresponding states in the boundary-scan internal state machine.

Figure 14 is a diagram of the Spartan-IIE family boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

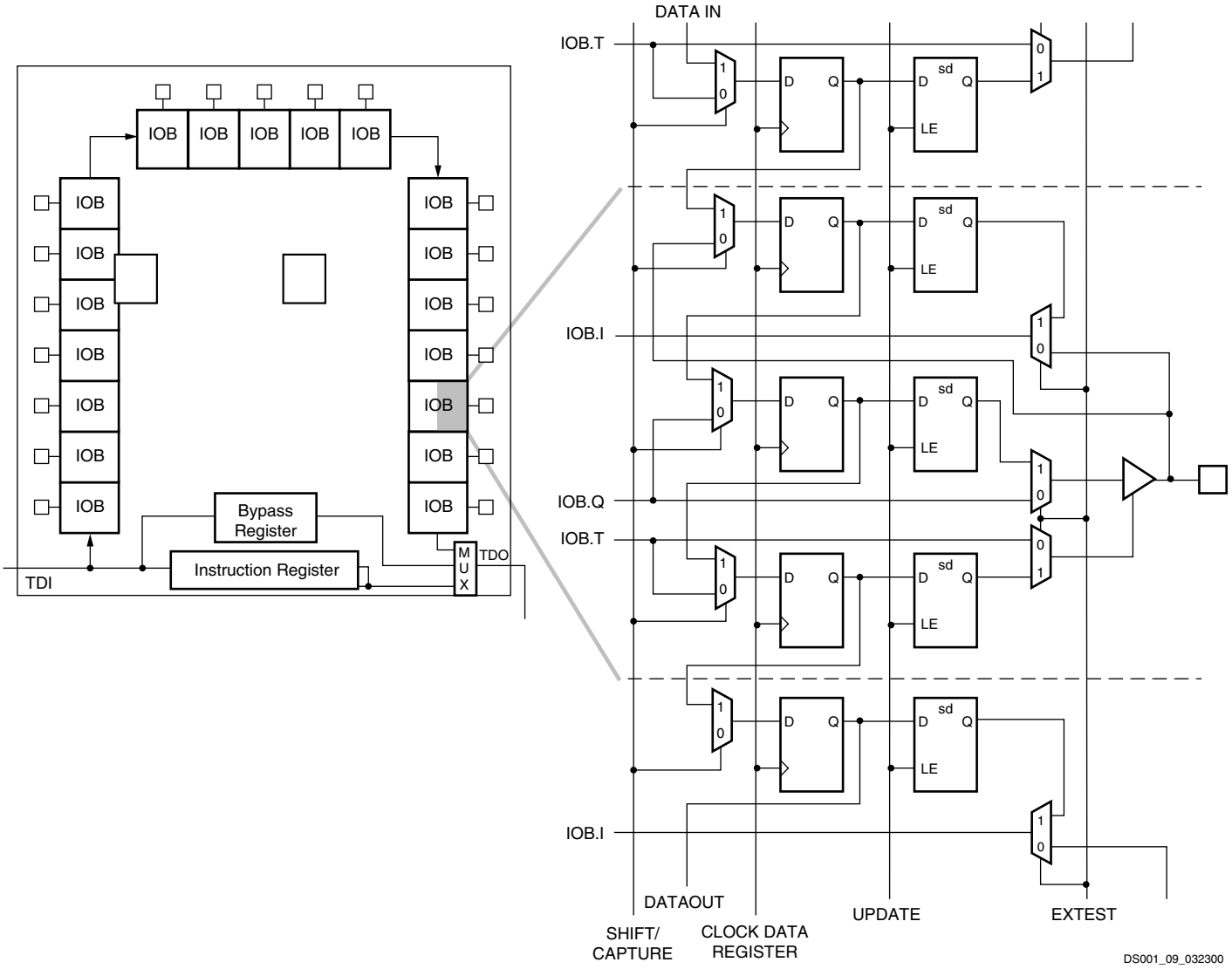


Figure 14: **Spartan-IIE Family Boundary Scan Logic**

During start-up, the device performs four operations:

1. The assertion of DONE. The failure of DONE to go High may indicate the unsuccessful loading of configuration data.
2. The release of the Global Three State (GTS). This activates all the I/Os to which signals are assigned. The remaining I/Os stay in a high-impedance state with internal weak pull-up resistors present.
3. The release of the Global Set Reset (GSR). This allows all flip-flops to change state.
4. The assertion of Global Write Enable (GWE). This allows all RAMs and flip-flops to change state.

By default, these operations are synchronized to CCLK. The entire start-up sequence lasts eight cycles, called C0-C7, after which the loaded design is fully functional. The four operations can be selected to switch on any CCLK cycle C1-C6 through settings in the Xilinx Development Software. The default timing for start-up is shown in the top half of Figure 17; heavy lines show default settings.

The default Start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The bottom half of Figure 17 shows another commonly used version of the start-up timing known as Sync-to-DONE. This version makes the GTS, GSR, and GWE events conditional upon the DONE pin going High. This timing is important for a daisy chain of multiple FPGAs in serial mode, since it ensures that all FPGAs go through start-up together, after all their DONE pins have gone High.

Sync-to-DONE timing is selected by setting the GTS, GSR, and GWE cycles to a value of DONE in the configuration options. This causes these signals to transition one clock cycle after DONE externally transitions High.

The sequence can also be paused at any stage until lock has been achieved on any or all DLLs.

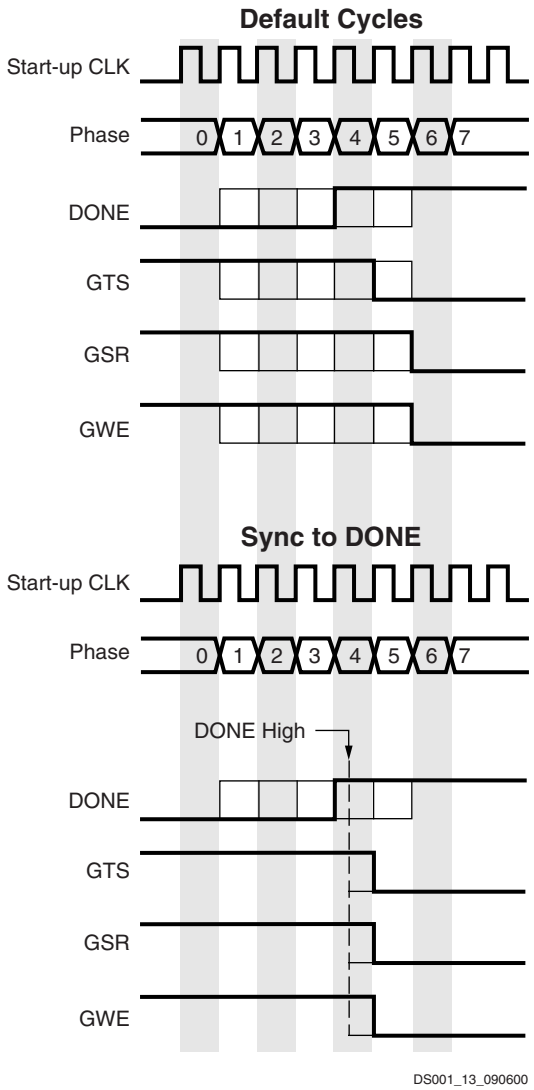


Figure 17: **Start-Up Waveforms**

Serial Modes

There are two serial configuration modes. In Master Serial mode, the FPGA controls the configuration process by driving CCLK as an output. In Slave Serial mode, the FPGA passively receives CCLK as an input from an external agent (e.g., a microprocessor, CPLD, or second FPGA in master mode) that is controlling the configuration process. In both modes, the FPGA is configured by loading one bit per CCLK cycle. The MSB of each configuration data byte is always written to the DIN pin first.

See Figure 18 for the sequence for loading data into the Spartan-IIE FPGA serially. This is an expansion of the "Load Configuration Data Frames" block in Figure 16, page 23. Note that $\overline{CS}$ and $\overline{WRITE}$ are not normally used during serial configuration. To ensure successful loading of the FPGA, do not toggle $\overline{WRITE}$ with $\overline{CS}$ Low during serial configuration.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
T_J	Junction temperature	Commercial	0	85	°C
		Industrial	–40	100	°C
V_{CCINT}	Supply voltage relative to GND(1)	Commercial	1.8 – 5%	1.8 + 5%	V
		Industrial	1.8 – 5%	1.8 + 5%	V
V_{CCO}	Supply voltage relative to GND(2)	Commercial	1.2	3.6	V
		Industrial	1.2	3.6	V
T_{IN}	Input signal transition time(3)		-	250	ns

Notes:
1. Functional operation is guaranteed down to a minimum V_{CCINT} of 1.62V (Nominal V_{CCINT} –10%). For every 50 mV reduction in V_{CCINT} below 1.71V (nominal V_{CCINT} –5%), all delay parameters increase by approximately 3%.
2. Minimum and maximum values for V_{CCO} vary according to the I/O standard selected.
3. Input and output measurement threshold is ~50% of V_{CCO}. See Delay Measurement Methodology, page 41 for specific details.

DC Characteristics Over Operating Conditions

Symbol	Description			Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data may be lost)			1.5	-	-	V
V_{DRIO}	Data retention V_{CCO} voltage (below which configuration data may be lost)			1.2	-	-	V
I_{CCINTQ}	Quiescent V_{CCINT} supply current(1)	XC2S50E	Commercial	-	10	200	mA
			Industrial	-	10	200	mA
		XC2S100E	Commercial	-	10	200	mA
			Industrial	-	10	200	mA
		XC2S150E	Commercial	-	10	300	mA
			Industrial	-	10	300	mA
		XC2S200E	Commercial	-	10	300	mA
			Industrial	-	10	300	mA
		XC2S300E	Commercial	-	12	300	mA
			Industrial	-	12	300	mA
		XC2S400E	Commercial	-	15	300	mA
			Industrial	-	15	300	mA
		XC2S600E	Commercial	-	15	400	mA
			Industrial	-	15	400	mA
I_{CCOQ}	Quiescent V_{CCO} supply current(1)			-	-	2	mA
I_{REF}	V_{REF} current per V_{REF} pin			-	-	20	µA
I_L	Input or output leakage current per pin			–10	-	+10	µA
C_{IN}	Input capacitance (sample tested)	TQ, PQ, FG, FT packages		-	-	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V (sample tested)(2)			-	-	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.6V (sample tested)(2)			-	-	0.25	mA

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not provide valid logic levels when input pins are connected to other circuits.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL I	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	8	–8
HSTL III	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	24	–8
HSTL IV	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	48	–8
SSTL3 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	–8
SSTL3 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	–16
SSTL2 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.61	V_{REF} + 0.61	7.6	–7.6
SSTL2 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	15.2	–15.2
CTT	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.4	V_{REF} + 0.4	8	–8
AGP	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	Note (2)	Note (2)

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested.
2. Tested according to the relevant specifications.

LVDS DC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		2.375	2.5	2.625	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	1.25	1.425	1.6	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	0.9	1.075	1.25	V
V_{ODIFF}	Differential output voltage (Q – $\overline{Q}$), Q = High or ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	250	350	450	mV
V_{OCM}	Output common-mode voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.125	1.25	1.375	V
V_{IDIFF}	Differential input voltage (Q – $\overline{Q}$), Q = High or ($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25 V	100	350	-	mV
V_{ICM}	Input common-mode voltage	Differential input voltage = ±350 mV	0.2	1.25	2.2	V

LVPECL DC Specifications

These values are valid at the output of the source termination pack shown under LVPECL, with a 100Ω differential load only. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. The following table summarizes the DC output specifications of LVPECL.

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential input voltage	0.3	-	0.3	-	0.3	-	V

IOB Input Switching Characteristics(1)

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in IOB Input Delay Adjustments for Different Standards, page 38.

Symbol	Description	Device	Speed Grade				Units
			-7		-6		
			Min	Max	Min	Max	
Propagation Delays							
T_{IOPI}	Pad to I output, no delay	All	0.4	0.8	0.4	0.8	ns
T_{IOPID}	Pad to I output, with delay	All	0.5	1.0	0.5	1.0	ns
T_{IOPLI}	Pad to output IQ via transparent latch, no delay	All	0.7	1.5	0.7	1.6	ns
T_{IOPLID}	Pad to output IQ via transparent latch, with delay	XC2S50E	1.3	3.0	1.3	3.1	ns
		XC2S100E	1.3	3.0	1.3	3.1	ns
		XC2S150E	1.3	3.2	1.3	3.3	ns
		XC2S200E	1.3	3.2	1.3	3.3	ns
		XC2S300E	1.3	3.2	1.3	3.3	ns
		XC2S400E	1.4	3.2	1.4	3.4	ns
		XC2S600E	1.5	3.5	1.5	3.7	ns
Sequential Delays							
T_{IOCKIQ}	Clock CLK to output IQ	All	0.1	0.7	0.1	0.7	ns
Setup/Hold Times with Respect to Clock CLK							
T_{IOPICK} / T_{IOICKP}	Pad, no delay	All	1.4 / 0	-	1.5 / 0	-	ns
$T_{IOPICKD}$ / $T_{IOICKPD}$	Pad, with delay	XC2S50E	2.9 / 0	-	2.9 / 0	-	ns
		XC2S100E	2.9 / 0	-	2.9 / 0	-	ns
		XC2S150E	3.1 / 0	-	3.1 / 0	-	ns
		XC2S200E	3.1 / 0	-	3.1 / 0	-	ns
		XC2S300E	3.1 / 0	-	3.1 / 0	-	ns
		XC2S400E	3.2 / 0	-	3.2 / 0	-	ns
		XC2S600E	3.5 / 0	-	3.5 / 0	-	ns
$T_{IOICECK}$ / $T_{IOCKICE}$	ICE input	All	0.7 / 0.01	-	0.7 / 0.01	-	ns
Set/Reset Delays							
$T_{IOSRCKI}$	SR input (IFF, synchronous)	All	0.9	-	1.0	-	ns
T_{IOSRIQ}	SR input to IQ (asynchronous)	All	0.5	1.2	0.5	1.4	ns
T_{GSRQ}	GSR to output IQ	All	3.8	8.5	3.8	9.7	ns

Notes:
1. Input timing for LVTTL is measured at 1.4V. For other I/O standards, see the table Delay Measurement Methodology, page 41.

DLL Timing Parameters

Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Symbol	Description	F_{CLKIN}	Speed Grade				Units
			-7		-6		
			Min	Max	Min	Max	
$F_{CLKINHF}$	Input clock frequency (CLKDLLHF)	-	60	320	60	275	MHz
$F_{CLKINLF}$	Input clock frequency (CLKDLL)	-	25	160	25	135	MHz
T_{DLLPW}	Input clock pulse width	≥25 MHz	5.0	-	5.0	-	ns
		≥50 MHz	3.0	-	3.0	-	ns
		≥100 MHz	2.4	-	2.4	-	ns
		≥150 MHz	2.0	-	2.0	-	ns
		≥200 MHz	1.8	-	1.8	-	ns
		≥250 MHz	1.5	-	1.5	-	ns
		≥300 MHz	1.3	-	NA	-	

DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications were determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers. Figure 22, page 44, provides definitions for various parameters in the table below.

Symbol	Description	F_{CLKIN}	CLKDLLHF		CLKDLL		Units
			Min	Max	Min	Max	
T_{IPTOL}	Input clock period tolerance		-	1.0	-	1.0	ns
T_{IJITCC}	Input clock jitter tolerance (cycle-to-cycle)		-	±150	-	±300	ps
T_{LOCK}	Time required for DLL to acquire lock(1)	> 60 MHz	-	20	-	20	µs
		50-60 MHz	-	-	-	25	µs
		40-50 MHz	-	-	-	50	µs
		30-40 MHz	-	-	-	90	µs
		25-30 MHz	-	-	-	120	µs
T_{OJITCC}	Output jitter (cycle-to-cycle) for any DLL clock output(2)		-	±60	-	±60	ps
T_{PHIO}	Phase offset between CLKIN and CLKO(3)		-	±100	-	±100	ps
T_{PHOO}	Phase offset between clock outputs on the DLL(4)		-	±140	-	±140	ps
T_{PHIOM}	Phase difference between CLKIN and CLKO(5)		-	±160	-	±160	ps
T_{PHOOM}	Phase difference between clock outputs on the DLL(6)		-	±200	-	±200	ps

Notes:

1. Commercial operating conditions. Add 30% for Industrial operating conditions.
2. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
3. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* output jitter and input clock jitter.
4. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* output jitter and input clock jitter.
5. **Maximum Phase Difference between CLKIN and CLKO** is the sum of output jitter and phase offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
6. **Maximum Phase Difference between Clock Outputs on the DLL** is the sum of output jitter and phase offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).

CLB Distributed RAM Switching Characteristics

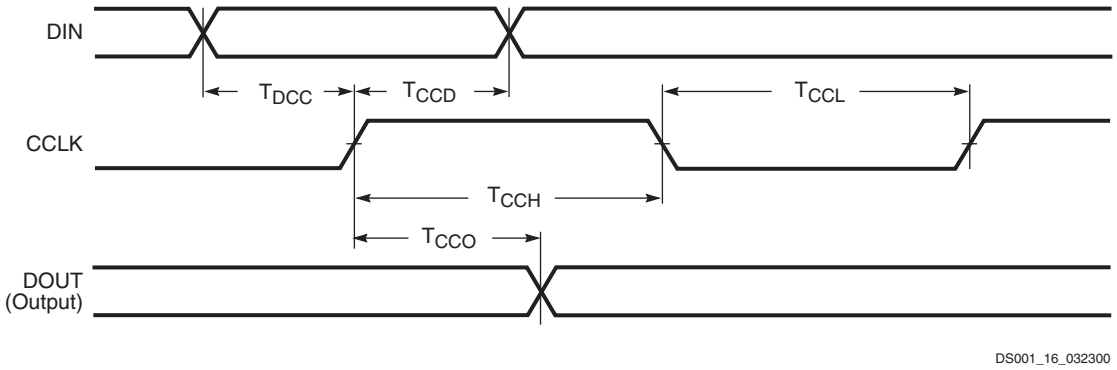
Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Sequential Delays						
$T_{SHCKO16}$	Clock CLK to X/Y outputs (WE active, 16 x 1 mode)	0.6	1.5	0.6	1.7	ns
$T_{SHCKO32}$	Clock CLK to X/Y outputs (WE active, 32 x 1 mode)	0.8	1.9	0.8	2.1	ns
Setup/Hold Times with Respect to Clock CLK						
T_{AS} / T_{AH}	F/G address inputs	0.42 / 0	-	0.5 / 0	-	ns
T_{DS} / T_{DH}	BX/BY data inputs (DIN)	0.53 / 0	-	0.6 / 0	-	ns
T_{WS} / T_{WH}	CE input (WS)	0.7 / 0	-	0.8 / 0	-	ns
Clock CLK						
T_{WPH}	Pulse width, High	2.1	-	2.4	-	ns
T_{WPL}	Pulse width, Low	2.1	-	2.4	-	ns
T_{WC}	Clock period to meet address write cycle time	4.2	-	4.8	-	ns

CLB Shift Register Switching Characteristics

Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Sequential Delays						
T_{REG}	Clock CLK to X/Y outputs	1.2	2.9	1.2	3.2	ns
Setup/Hold Times with Respect to Clock CLK						
T_{SHDICK}	BX/BY data inputs (DIN)	0.53 / 0	-	0.6 / 0	-	ns
T_{SHCECK}	CE input (WS)	0.7 / 0	-	0.8 / 0	-	ns
Clock CLK						
T_{SRPH}	Pulse width, High	2.1	-	2.4	-	ns
T_{SRPL}	Pulse width, Low	2.1	-	2.4	-	ns

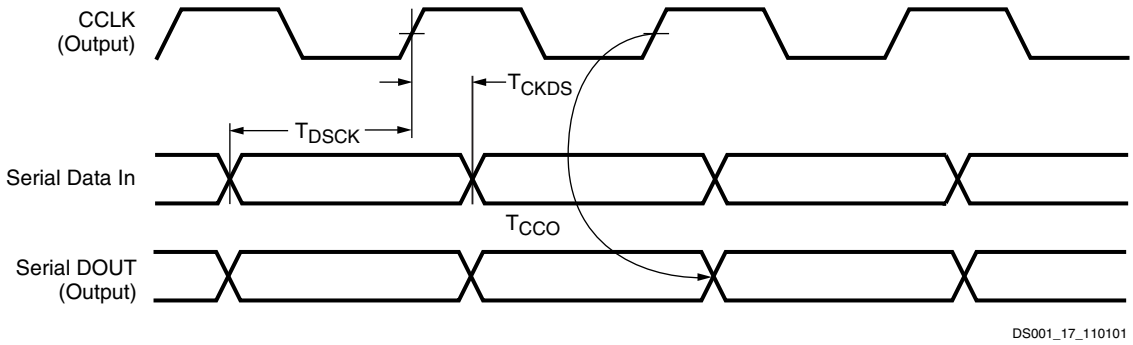
Block RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Sequential Delays						
T_{BCKO}	Clock CLK to DOUT output	0.6	3.1	0.6	3.5	ns
Setup/Hold Times with Respect to Clock CLK						
T_{BACK} / T_{BCKA}	ADDR inputs	1.0 / 0	-	1.1 / 0	-	ns
T_{BDCK}/ T_{BCKD}	DIN inputs	1.0 / 0	-	1.1 / 0	-	ns
T_{BECK}/ T_{BCKE}	EN inputs	2.2 / 0	-	2.5 / 0	-	ns
T_{BRCK}/ T_{BCKR}	RST input	2.1 / 0	-	2.3 / 0	-	ns
T_{BWCK}/ T_{BCKW}	WEN input	2.0 / 0	-	2.2 / 0	-	ns
Clock CLK						
T_{BPWH}	Pulse width, High	1.4	-	1.5	-	ns
T_{BPWL}	Pulse width, Low	1.4	-	1.5	-	ns
T_{BCCS}	CLKA -> CLKB setup time for different ports	2.7	-	3.0	-	ns



Symbol		Description	All Devices		Units
			Min	Max	
T_{DCC} / T_{CCD}	CCLK	DIN setup/hold	5 / 0	-	ns
T_{CCO}		DOUT	-	12	ns
T_{CCH}		High time	5	-	ns
T_{CCL}		Low time	5	-	ns
F_{CC}		Maximum frequency	-	66	MHz

Figure 24: **Slave Serial Mode Timing**



Symbol		Description	All Devices		Units
			Min	Max	
T_{DSCK} / T_{CKDS}	CCLK	DIN setup/hold	5 / 0	-	ns
T_{CCO}		DOUT	-	12	ns
F_{CC}		Frequency tolerance with respect to nominal	–30%	+45%	-

Figure 25: **Master Serial Mode Timing**

Pin Definitions *(Continued)*

Pad Name	Dedicated Pin	Direction	Description
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In Slave Parallel mode, D0-D7 are configuration data input pins. During readback, D0-D7 are output pins. These pins become user I/Os after configuration unless the Slave Parallel port is retained. In serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
$\overline{WRITE}$	No	Input	In Slave Parallel mode, the active-low Write Enable signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
$\overline{CS}$	No	Input	In Slave Parallel mode, the active-low Chip Select signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary Scan Test Access Port pins (IEEE 1149.1).
V_{CCINT}	Yes	Input	1.8V power supply pins for the internal core logic.
V_{CCO}	Yes	Input	Power supply pins for output drivers (1.5V, 1.8V, 2.5V, or 3.3V subject to banking rules in the Functional Description module.
V_{REF}	No	Input	Input threshold reference voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules in the Functional Description module.
GND	Yes	Input	Ground. All must be connected.
IRDY, TRDY	No	See PCI core documentation	These signals can only be accessed when using Xilinx PCI cores. If the cores are not used, these pins are available as user I/Os.
L#[P/N] (e.g., L0P)	No	Bidirectional	Differential I/O with synchronous output. P = positive, N = negative. The number (#) is used to associate the two pins of a differential pair. Becomes a general user I/O when not needed for differential signals.
L#[P/N]_Y (e.g., L0P_Y)	No	Bidirectional	Differential I/O with asynchronous or synchronous output (asynchronous output not compatible for all densities in a package). P = positive, N = negative. The number (#) is used to associate the two pins of a differential pair. Becomes a general user I/O when not needed for differential signals.
L#[P/N]_YY (e.g., L0P_YY)	No	Bidirectional	Differential I/O with asynchronous or synchronous output (compatible for all densities in a package). P = positive, N = negative. The number (#) is used to associate the two pins of a differential pair. Becomes a general user I/O when not needed for differential signals.
I/O	No	Bidirectional	These pins can be configured to be input and/or output after configuration is completed. Unused I/Os are disabled with a weak pull-down resistor. After power-on and before configuration is completed, these pins are either pulled up or left floating according to the Mode pin values. See the DC and Switching Characteristics module for power-on characteristics.

TQ144 Pinouts (XC2S50E and XC2S100E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O (DLL), L17P	4	P56	-	-
I/O	4	P57	-	-
I/O, VREF Bank 4	4	P58	-	All
I/O, L16N_YY	4	P59	All	-
I/O, L16P_YY	4	P60	All	-
VCCINT	-	P61	-	-
GND	-	P62	-	-
I/O, L15N_YY	4	P63	All	-
I/O, L15P_YY	4	P64	All	XC2S100E
I/O	4	P65	-	-
I/O, VREF Bank 4	4	P66	-	All
I/O	4	P67	-	-
I/O, L14N_YY	4	P68	All	-
I/O, L14P_YY	4	P69	All	-
GND	-	P70	-	-
DONE	3	P71	-	-
VCCO	-	P72	-	-
$\overline{\text{PROGRAM}}$	-	P73	-	-
I/O ($\overline{\text{INIT}}$), L13N_YY	3	P74	All	-
I/O (D7), L13P_YY	3	P75	All	-
I/O	3	P76	-	-
I/O, VREF Bank 3	3	P77	-	All
I/O	3	P78	-	-
I/O, L12N	3	P79	XC2S50E	XC2S100E
I/O (D6), L12P	3	P80	XC2S50E	-
GND	-	P81	-	-
I/O (D5), L11N_YY	3	P82	All	-
I/O, L11P_YY	3	P83	All	-
I/O	3	P84	-	-

TQ144 Pinouts (XC2S50E and XC2S100E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 3, L10N	3	P85	XC2S50E	All
I/O (D4), L10P	3	P86	XC2S50E	-
I/O	3	P87	-	-
VCCINT	-	P88	-	-
I/O (TRDY)	3	P89	-	-
VCCO	-	P90	-	-
GND	-	P91	-	-
I/O (IRDY)	2	P92	-	-
I/O	2	P93	-	-
I/O (D3), L9N	2	P94	XC2S50E	-
I/O, VREF Bank 2, L9P	2	P95	XC2S50E	All
I/O	2	P96	-	-
I/O, L8N_YY	2	P97	All	-
I/O (D2), L8P_YY	2	P98	All	-
GND	-	P99	-	-
I/O (D1), L7N	2	P100	XC2S50E	-
I/O, L7P	2	P101	XC2S50E	XC2S100E
I/O	2	P102	-	-
I/O, VREF Bank 2	2	P103	-	All
I/O	2	P104	-	-
I/O (DIN, D0), L6N_YY	2	P105	All	-
I/O (DOUT, BUSY), L6P_YY	2	P106	All	-
CCLK	2	P107	-	-
VCCO	-	P108	-	-
TDO	2	P109	-	-
GND	-	P110	-	-
TDI	-	P111	-	-

TQ144 Pinouts (XC2S50E and XC2S100E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O ($\overline{CS}$), L5P_YY	1	P112	All	-
I/O ($\overline{WRITE}$), L5N_YY	1	P113	All	-
I/O	1	P114	-	-
I/O, VREF Bank 1	1	P115	-	All
I/O	1	P116	-	-
I/O, L4P_YY	1	P117	All	XC2S100E
I/O, L4N_YY	1	P118	All	-
GND	-	P119	-	-
VCCINT	-	P120	-	-
I/O, L3P_YY	1	P121	All	-
I/O, L3N_YY	1	P122	All	-
I/O, VREF Bank 1	1	P123	-	All
I/O	1	P124	-	-
I/O (DLL), L2P	1	P125	-	-
GCK2, I	1	P126	-	-
GND	-	P127	-	-
VCCO	-	P128	-	-
GCK3, I	0	P129	-	-
VCCINT	-	P130	-	-
I/O (DLL), L2N	0	P131	-	-
I/O, VREF Bank 0	0	P132	-	All
I/O, L1P_YY	0	P133	All	-
I/O, L1N_YY	0	P134	All	-
VCCINT	-	P135	-	-
GND	-	P136	-	-
I/O, L0P_YY	0	P137	All	-
I/O, L0N_YY	0	P138	All	XC2S100E

TQ144 Pinouts (XC2S50E and XC2S100E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O	0	P139	-	-
I/O, VREF Bank 0	0	P140	-	All
I/O	0	P141	-	-
I/O	0	P142	-	-
TCK	-	P143	-	-
VCCO	-	P144	-	-

TQ144 Differential Clock Pins

Clock	Bank	P		N	
		Pin	Name	Pin	Name
GCK0	4	P55	GCK0, I	P56	I/O (DLL), L17P
GCK1	5	P52	GCK1, I	P50	I/O (DLL), L17N
GCK2	1	P126	GCK2, I	P125	I/O (DLL), L2P
GCK3	0	P129	GCK3, I	P131	I/O (DLL), L2N

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O (D5), L35N_YY	3	L13	All	-
I/O, L35P_YY	3	K14	All	-
I/O, L34N	3	K15	XC2S100E, 150E, 400E	-
I/O, L34P	3	K16	XC2S100E, 150E, 400E	-
I/O, L33N	3	L12	XC2S50E, 100E, 150E, 200E, 300E(1)	-
I/O, L33P	3	K12	XC2S50E, 100E, 150E, 200E, 300E(1)	-
I/O, VREF Bank 3, L32N	3	K13	XC2S50E, 300E, 400E	All
I/O (D4), L32P	3	J14	XC2S50E, 300E, 400E	-
I/O, L31N	3	J15	XC2S100E, 150E, 200E, 400E	-
I/O, L31P	3	J16	XC2S100E, 150E, 200E, 400E	XC2S400E
I/O (TRDY)	3	J13	-	-
I/O (IRDY), L30N_YY	2	H16	All	-
I/O, L30P_YY	2	G16	All	-
I/O, L29N	2	H14	XC2S100E, 150E, 200E, 400E	XC2S400E
I/O, L29P	2	H15	XC2S100E, 150E, 200E, 400E	-
I/O (D3), L28N	2	G15	XC2S50E, 300E, 400E	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 2, L28P	2	F16	XC2S50E, 300E, 400E	All
I/O, L27N	2	H13	XC2S50E, 100E, 150E, 200E, 300E(1)	-
I/O, L27P	2	G14	XC2S50E, 100E, 150E, 200E, 300E(2)	-
I/O, L26N	2	F15	XC2S100E, 150E, 400E	-
I/O, L26P	2	E16	XC2S100E, 150E, 400E	-
I/O, L25N_YY	2	G13	All	-
I/O (D2), L25P_YY	2	F14	All	-
I/O (D1), L24N	2	E15	XC2S50E, 300E, 400E	-
I/O, L24P	2	D16	XC2S50E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L23N	2	F13	XC2S150E, 200E, 400E	-
I/O, L23P	2	E14	XC2S150E, 200E, 400E	-
I/O, L22N	2	D15	XC2S50E, 150E, 200E, 300E, 400E	-
I/O, VREF Bank 2, L22P	2	C16	XC2S50E, 150E, 200E, 300E, 400E	All
I/O, L21N	2	G12	XC2S50E, 100E, 200E, 300E	-
I/O, L21P	2	F12	XC2S50E, 100E, 200E, 300E	-
I/O, L20N	2	E13	XC2S100E, 200E, 300E	-

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O, L#P_YY	7	L5	All	-	I/O, L75P_YY	I/O, L99P_YY	I/O, L105P_YY	I/O, L105P_YY	I/O, L105P_YY	I/O, L105P_YY
I/O (IRDY), L#N_YY	7	L6	All	-	I/O (IRDY), L75N_YY	I/O (IRDY), L99N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY
I/O (TRDY)	6	M1	-	-	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)
I/O	6	M2	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P_Y	6	M3	XC2S200E, 300E, 600E	-	-	I/O	I/O, L104P_Y	I/O, L104P_Y	I/O, L104P	I/O, L104P_Y
I/O, L#N_Y	6	M4	XC2S100E, 150E, 200E, 300E, 600E	XC2S400E, 600E	I/O, L74P_Y	I/O, L98P_Y	I/O, L104N_Y	I/O, L104N_Y	I/O, VREF Bank 6, L104N	I/O, VREF Bank 6, L104N_Y
I/O, L#P_Y	6	M5	XC2S100E, 150E, 300E, 400E	-	I/O, L74N_Y	I/O, L98N_Y	I/O, L103P	I/O, L103P_Y	I/O, L103P_Y	I/O, L103P
I/O, L#N_Y	6	M6	XC2S300E, 400E	-	-	-	I/O, L103N	I/O, L103N_Y	I/O, L103N_Y	I/O, L103N
I/O	6	N1	-	-	-	-	-	I/O	I/O	I/O
I/O	6	N2	-	-	I/O, L73P	I/O, L97P	I/O	I/O	I/O	I/O
I/O, VREF Bank 6, L#P	6	N3	XC2S200E, 400E	All	I/O, VREF Bank 6, L73N	I/O, VREF Bank 6, L97N	I/O, VREF Bank 6, L102P_Y	I/O, VREF Bank 6, L102P	I/O, VREF Bank 6, L102P_Y	I/O, VREF Bank 6, L102P
I/O, L#N	6	N4	XC2S100E, 150E, 200E, 400E	-	I/O, L72P_Y	I/O, L96P_Y	I/O, L102N_Y	I/O, L102N	I/O, L102N_Y	I/O, L102N
I/O, L#P_Y	6	N5	XC2S100E, 150E, 300E, 600E	-	I/O, L72N_Y	I/O, L96N_Y	I/O, L101P	I/O, L101P_Y	I/O, L101P	I/O, L101P_Y
I/O, L#N_Y	6	N6	XC2S300E, 600E	-	-	-	I/O, L101N	I/O, L101N_Y	I/O, L101N	I/O, L101N_Y
I/O, L#P_Y	6	P1	XC2S150E, 200E, 300E, 600E	-	-	I/O, L95P_Y	I/O, L100P_Y	I/O, L100P_Y	I/O, L100P	I/O, L100P_Y
I/O, L#N_Y	6	P2	XC2S100E, 150E, 200E, 300E, 600E	-	I/O, L71P_Y	I/O, L95N_Y	I/O, L100N_Y	I/O, L100N_Y	I/O, L100N	I/O, L100N_Y
I/O	6	R1	XC2S100E, 150E	-	I/O, L71N_Y	I/O, L94P_Y	I/O	I/O	I/O	I/O
I/O, L#P_Y	6	P3	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L94N_Y	I/O, L99P_Y	I/O, L99P_Y	I/O, L99P_Y	I/O, L99P_Y
I/O, L#N_Y	6	P4	XC2S200E, 300E, 400E, 600E	-	-	-	I/O, L99N_Y	I/O, L99N_Y	I/O, L99N_Y	I/O, L99N_Y
I/O, L#P_YY	6	P5	All	-	I/O, L70P_YY	I/O, L93P_YY	I/O, L98P_YY	I/O, L98P_YY	I/O, L98P_YY	I/O, L98P_YY
I/O, L#N_YY	6	P6	All	-	I/O, L70N_YY	I/O, L93N_YY	I/O, L98N_YY	I/O, L98N_YY	I/O, L98N_YY	I/O, L98N_YY

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O, VREF Bank 5, L#N_Y	5	V8	XC2S100E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 5, L58N_Y	I/O, VREF Bank 5, L77N	I/O, VREF Bank 5, L82N_Y	I/O, VREF Bank 5, L82N_Y	I/O, VREF Bank 5, L82N_Y	I/O, VREF Bank 5, L82N_Y
I/O, L#P_Y	5	W8	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L58P_Y	I/O, L77P	I/O, L82P_Y	I/O, L82P_Y	I/O, L82P_Y	I/O, L82P_Y
I/O, L#N_Y	5	AB9	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L57N_Y	I/O, L76N	I/O, L81N_Y	I/O, L81N_Y	I/O, L81N_Y	I/O, L81N_Y
I/O, L#P_Y	5	AA9	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L57P_Y	I/O, L76P	I/O, L81P_Y	I/O, L81P_Y	I/O, L81P_Y	I/O, L81P_Y
I/O	5	AB10	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#N_Y	5	W9	XC2S150E, 300E, 400E, 600E	-	-	I/O, L75N_Y	I/O, L80N	I/O, L80N_Y	I/O, L80N_Y	I/O, L80N_Y
I/O, L#P_Y	5	Y9	XC2S100E, 150E, 300E, 400E, 600E	-	I/O, L56N_Y	I/O, L75P_Y	I/O, L80P	I/O, L80P_Y	I/O, L80P_Y	I/O, L80P_Y
I/O, L#N_Y	5	V9	XC2S100E, 150E, 300E, 400E, 600E	-	I/O, L56P_Y	I/O, L74N_Y	I/O, L79N	I/O, L79N_Y	I/O, L79N_Y	I/O, L79N_Y
I/O, L#P_Y	5	U9	XC2S150E, 300E, 400E, 600E	-	-	I/O, L74P_Y	I/O, L79P	I/O, L79P_Y	I/O, L79P_Y	I/O, L79P_Y
I/O	5	AA10	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#N_Y	5	W10	XC2S200E, 300E, 400E, 600E	-	I/O, L55N	I/O, L73N	I/O, L78N_Y	I/O, L78N_Y	I/O, L78N_Y	I/O, L78N_Y
I/O, L#P_Y	5	Y10	XC2S200E, 300E, 400E, 600E	-	I/O, L55P	I/O, L73P	I/O, L78P_Y	I/O, L78P_Y	I/O, L78P_Y	I/O, L78P_Y
I/O, VREF Bank 5, L#N_Y	5	V10	XC2S200E, 300E, 400E, 600E	All	I/O, VREF Bank 5, L54N	I/O, VREF Bank 5, L72N	I/O, VREF Bank 5, L77N_Y	I/O, VREF Bank 5, L77N_Y	I/O, VREF Bank 5, L77N_Y	I/O, VREF Bank 5, L77N_Y
I/O, L#P_Y	5	U10	XC2S200E, 300E, 400E, 600E	-	I/O, L54P	I/O, L72P	I/O, L77P_Y	I/O, L77P_Y	I/O, L77P_Y	I/O, L77P_Y
I/O	5	U11	-	-	-	-	-	I/O	I/O	I/O
I/O	5	V11	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#N	5	W11	XC2S200E, 400E	-	I/O	I/O, L71N	I/O, L76N_Y	I/O, L76N	I/O, L76N_Y	I/O, L76N
I/O, L#P	5	Y11	XC2S200E, 400E	XC2S400E, 600E	-	I/O, L71P	I/O, L76P_Y	I/O, L76P	I/O, VREF Bank 5, L76P_Y	I/O, VREF Bank 5, L76P
I/O	5	AA11	-	-	-	-	-	I/O	I/O	I/O
I/O (DLL), L#N	5	AB11	-	-	I/O (DLL), L53N	I/O (DLL), L70N	I/O (DLL), L75N	I/O (DLL), L75N	I/O (DLL), L75N	I/O (DLL), L75N
GCK1, I	5	AB12	-	-	GCK1, I	GCK1, I	GCK1, I	GCK1, I	GCK1, I	GCK1, I

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
GCK0, I	4	AA12	-	-	GCK0, I	GCK0, I	GCK0, I	GCK0, I	GCK0, I	GCK0, I
I/O (DLL), L#P	4	Y12	-	-	I/O (DLL), L53P	I/O (DLL), L70P	I/O (DLL), L75P	I/O (DLL), L75P	I/O (DLL), L75P	I/O (DLL), L75P
I/O	4	W12	-	-	-	-	-	I/O	I/O	I/O
I/O, L#N	4	V12	XC2S150E, 300E, 600E	-	-	I/O, L69N_Y	I/O, L74N	I/O, L74N_Y	I/O, L74N	I/O, L74N_Y
I/O, L#P	4	U12	XC2S150E, 300E, 600E	XC2S400E, 600E	I/O, L52N	I/O, L69P_Y	I/O, L74P	I/O, L74P_Y	I/O, VREF Bank 4, L74P	I/O, VREF Bank 4, L74P_Y
I/O, L#N	4	AB13	XC2S300E, 600E	-	I/O, L52P	I/O	I/O, L73N	I/O, L73N_Y	I/O, L73N	I/O, L73N_Y
I/O, L#P	4	AA13	XC2S300E, 600E	-	-	-	I/O, L73P	I/O, L73P_Y	I/O, L73P	I/O, L73P_Y
I/O	4	Y13	-	-	-	-	-	I/O	I/O	I/O
I/O, L#N	4	W13	XC2S200E, 300E, 400E, 600E	-	I/O, L51N	I/O, L68N	I/O, L72N_Y	I/O, L72N_Y	I/O, L72N_Y	I/O, L72N_Y
I/O, VREF Bank 4, L#P	4	V13	XC2S200E, 300E, 400E, 600E	All	I/O, VREF Bank 4, L51P	I/O, VREF Bank 4, L68P	I/O, VREF Bank 4, L72P_Y	I/O, VREF Bank 4, L72P_Y	I/O, VREF Bank 4, L72P_Y	I/O, VREF Bank 4, L72P_Y
I/O	4	U13	-	-	I/O, L50N	I/O, L67N	I/O	I/O	I/O	I/O
I/O, L#N	4	AB14	-	-	I/O, L50P	I/O, L67P	I/O, L71N	I/O, L71N	I/O, L71N	I/O, L71N
I/O, L#P	4	AA14	-	-	-	-	I/O, L71P	I/O, L71P	I/O, L71P	I/O, L71P
I/O	4	AB15	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#N	4	Y14	XC2S100E, 150E, 200E	-	I/O, L49N_Y	I/O, L66N_Y	I/O, L70N_Y	I/O, L70N	I/O, L70N	I/O, L70N
I/O, L#P	4	W14	XC2S100E, 150E, 200E	-	I/O, L49P_Y	I/O, L66P_Y	I/O, L70P_Y	I/O, L70P	I/O, L70P	I/O, L70P
I/O, L#N	4	U14	XC2S150E, 200E	-	-	I/O, L65N_Y	I/O, L69N_Y	I/O, L69N	I/O, L69N	I/O, L69N
I/O, L#P	4	V14	XC2S150E, 200E	-	-	I/O, L65P_Y	I/O, L69P_Y	I/O, L69P	I/O, L69P	I/O, L69P
I/O, L#N	4	AA15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L48N_Y	I/O, L64N	I/O, L68N_Y	I/O, L68N_Y	I/O, L68N_Y	I/O, L68N_Y
I/O, L#P	4	Y15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L48P_Y	I/O, L64P	I/O, L68P_Y	I/O, L68P_Y	I/O, L68P_Y	I/O, L68P_Y
I/O, L#N	4	W15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L47N_Y	I/O, L63N	I/O, L67N_Y	I/O, L67N_Y	I/O, L67N_Y	I/O, L67N_Y
I/O, VREF Bank 4, L#P	4	V15	XC2S100E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 4, L47P_Y	I/O, VREF Bank 4, L63P	I/O, VREF Bank 4, L67P_Y	I/O, VREF Bank 4, L67P_Y	I/O, VREF Bank 4, L67P_Y	I/O, VREF Bank 4, L67P_Y
I/O	4	AB16	-	-	-	-	-	I/O	I/O	I/O
I/O	4	AB17	-	-	I/O	I/O	I/O	I/O	I/O	I/O

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O, L#P	2	L17	XC2S100E, 150E, 200E, 300E, 600E	XC2S400E, 600E	I/O, L29N_Y	I/O, L40N_Y	I/O, L43P_Y	I/O, L43P_Y	I/O, VREF Bank 2, L43P	I/O, VREF Bank 2, L43P_Y
I/O, L#N	2	K22	XC2S100E, 150E, 300E, 400E	-	I/O, L29P_Y	I/O, L40P_Y	I/O, L42N	I/O, L42N_Y	I/O, L42N_Y	I/O, L42N
I/O, L#P	2	K21	XC2S300E, 400E	-	-	-	I/O, L42P	I/O, L42P_Y	I/O, L42P_Y	I/O, L42P
I/O	2	K20	-	-	-	-	-	I/O	I/O	I/O
I/O (D3)	2	K19	-	-	I/O (D3)	I/O (D3), L39N	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)
I/O, VREF Bank 2, L#N	2	K18	XC2S100E, 200E, 400E	All	I/O, VREF Bank 2, L28N_Y	I/O, VREF Bank 2, L39P	I/O, VREF Bank 2, L41N_Y	I/O, VREF Bank 2, L41N	I/O, VREF Bank 2, L41N_Y	I/O, VREF Bank 2, L41N
I/O, L#P	2	K17	XC2S100, 150E, 200E, 400E	-	I/O, L28P_Y	I/O, L38N_Y	I/O, L41P_Y	I/O, L41P	I/O, L41P_Y	I/O, L41P
I/O, L#N	2	J22	XC2S150E, 300E, 600E	-	I/O	I/O, L38P_Y	I/O, L40N	I/O, L40N_Y	I/O, L40N	I/O, L40N_Y
I/O, L#P	2	J21	XC2S300E, 600E	-	-	-	I/O, L40P	I/O, L40P_Y	I/O, L40P	I/O, L40P_Y
I/O, L#N	2	J20	XC2S150E, 200E, 300E, 600E	-	-	I/O, L37N_Y	I/O, L39N_Y	I/O, L39N_Y	I/O, L39N	I/O, L39N_Y
I/O, L#P	2	J19	XC2S100E, 150E, 200E, 300E, 600E	-	I/O, L27N_Y	I/O, L37P_Y	I/O, L39P_Y	I/O, L39P_Y	I/O, L39P	I/O, L39P_Y
I/O	2	H22	XC2S100E, 150E	-	I/O, L27P_Y	I/O, L36N_Y	I/O	I/O	I/O	I/O
I/O, L#N	2	J18	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L36P_Y	I/O, L38N_Y	I/O, L38N_Y	I/O, L38N_Y	I/O, L38N_Y
I/O, L#P	2	J17	XC2S200E, 300E, 400E, 600E	-	-	-	I/O, L38P_Y	I/O, L38P_Y	I/O, L38P_Y	I/O, L38P_Y
I/O, L#N	2	H21	XC2S150E, 200E, 300E, 400E, 600E	-	I/O	I/O, L35N_Y	I/O, L37N_Y	I/O, L37N_Y	I/O, L37N_Y	I/O, L37N_Y
I/O (D2), L#P	2	H20	XC2S150E, 200E, 300E, 400E, 600E	-	I/O (D2)	I/O (D2), L35P_Y	I/O (D2), L37P_Y	I/O (D2), L37P_Y	I/O (D2), L37P_Y	I/O (D2), L37P_Y
I/O (D1), L#N	2	H19	XC2S300E, 400E, 600E	-	I/O (D1), L26N	I/O (D1), L34N	I/O (D1), L36N	I/O (D1), L36N_Y	I/O (D1), L36N_Y	I/O (D1), L36N_Y
I/O, VREF Bank 2, L#P	2	H18	XC2S300E, 400E, 600E	All	I/O, VREF Bank 2, L26P	I/O, VREF Bank 2, L34P	I/O, VREF Bank 2, L36P	I/O, VREF Bank 2, L36P_Y	I/O, VREF Bank 2, L36P_Y	I/O, VREF Bank 2, L36P_Y
I/O	2	G22	-	-	-	-	-	I/O	I/O	I/O
I/O	2	F22	-	-	I/O	I/O	I/O	I/O	I/O	I/O

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, VREF Bank 6, L176N	6	P9	XC2S600E	All	I/O, VREF Bank 6, L176N	I/O, VREF Bank 6, L176N_Y
I/O, L175P	6	R1	XC2S400E	-	I/O, L175P_Y	I/O, L175P
I/O, L175N	6	R2	XC2S400E	-	I/O, L175N_Y	I/O, L175N
I/O	6	R4	-	-	-	I/O
I/O, L174P_YY	6	R5	All	-	I/O, L174P_YY	I/O, L174P_YY
I/O, L174N_YY	6	R6	All	-	I/O, L174N_YY	I/O, L174N_YY
I/O	6	R7	-	-	-	I/O
I/O, L173P_YY	6	R8	All	-	I/O, L173P_YY	I/O, L173P_YY
I/O, VREF Bank 6, L173N_YY	6	R9	All	All	I/O, VREF Bank 6, L173N_YY	I/O, VREF Bank 6, L173N_YY
I/O, L172P	6	T1	XC2S600E	-	I/O, L172P	I/O, L172P_Y
I/O, L172N	6	T2	XC2S600E	-	I/O, L172N	I/O, L172N_Y
I/O	6	T3	-	-	-	I/O
I/O, L171P	6	T5	XC2S600E	-	I/O, L171P	I/O, L171P_Y
I/O, L171N	6	T6	XC2S600E	-	I/O, L171N	I/O, L171N_Y
I/O	6	U1	-	-	-	I/O
I/O, L170P	6	T7	XC2S600E	-	I/O, L170P	I/O, L170P_Y
I/O, L170N	6	T8	XC2S600E	-	I/O, L170N	I/O, L170N_Y
I/O, L169P	6	U2	XC2S400E	-	I/O, L169P_Y	I/O, L169P
I/O, L169N	6	U3	XC2S400E	-	I/O, L169N_Y	I/O, L169N
I/O	6	U7	-	-	-	I/O
I/O, L168P	6	U4	XC2S600E	-	-	I/O, L168P_Y
I/O, L168N	6	U5	XC2S600E	-	I/O	I/O, L168N_Y
I/O	6	U8	-	-	I/O	I/O
I/O, L167P_YY	6	V1	All	-	I/O, L167P_YY	I/O, L167P_YY
I/O, L167N_YY	6	V2	All	-	I/O, L167N_YY	I/O, L167N_YY
I/O	6	V3	-	-	I/O	I/O
I/O, VREF Bank 6, L166P_YY	6	V4	All	All	I/O, VREF Bank 6, L166P_YY	I/O, VREF Bank 6, L166P_YY
I/O, L166N_YY	6	V5	All	-	I/O, L166N_YY	I/O, L166N_YY
I/O, L165P_YY	6	V6	All	-	I/O, L165P_YY	I/O, L165P_YY
I/O, L165N_YY	6	V7	All	-	I/O, L165N_YY	I/O, L165N_YY
I/O	6	V8	-	-	-	I/O
I/O, L164P	6	W1	XC2S600E	-	I/O, L164P	I/O, L164P_Y

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
DONE	3	AE26	-	-	DONE	DONE
$\overline{\text{PROGRAM}}$	-	AC24	-	-	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$
I/O ($\overline{\text{INIT}}$), L101N_YY	3	AD25	All	-	I/O ($\overline{\text{INIT}}$), L101N_YY	I/O ($\overline{\text{INIT}}$), L101N_YY
I/O (D7), L101P_YY	3	AD26	All	-	I/O (D7), L101P_YY	I/O (D7), L101P_YY
I/O, L100N	3	AC25	-	-	-	I/O, L100N
I/O, L100P	3	AC26	-	-	-	I/O, L100P
I/O, L99N	3	AB22	XC2S600E	-	-	I/O, L99N_Y
I/O, L99P	3	AB23	XC2S600E	-	I/O	I/O, L99P_Y
I/O, L98N_YY	3	AB25	All	-	I/O, L98N_YY	I/O, L98N_YY
I/O, L98P_YY	3	AB26	All	-	I/O, L98P_YY	I/O, L98P_YY
I/O, L97N	3	AA23	-	-	I/O, L97N_Y	I/O, L97N
I/O, L97P	3	AA24	-	-	I/O, L97P_Y	I/O, L97P
I/O, VREF Bank 3, L96N	3	AA25	XC2S600E	All	I/O, VREF Bank 3, L96N	I/O, VREF Bank 3, L96N_Y
I/O, L96P	3	AA26	XC2S600E	-	I/O, L96P	I/O, L96P_Y
I/O, L95N	3	AA22	XC2S600E	-	-	I/O, L95N_Y
I/O, L95P	3	Y22	XC2S600E	-	I/O	I/O, L95P_Y
I/O, L94N	3	Y23	XC2S400E	-	I/O, L94N_Y	I/O, L94N
I/O, L94P	3	Y24	XC2S400E	-	I/O, L94P_Y	I/O, L94P
I/O, L93N	3	Y25	XC2S600E	-	I/O, L93N	I/O, L93N_Y
I/O, L93P	3	Y26	XC2S600E	-	I/O, L93P	I/O, L93P_Y
I/O, VREF Bank 3, L92N_YY	3	W21	All	All	I/O, VREF Bank 3, L92N_YY	I/O, VREF Bank 3, L92N_YY
I/O, L92P_YY	3	W22	All	-	I/O, L92P_YY	I/O, L92P_YY
I/O	3	Y21	-	-	-	I/O
I/O, L91N_YY	3	W25	All	-	I/O, L91N_YY	I/O, L91N_YY
I/O, L91P_YY	3	W26	All	-	I/O, L91P_YY	I/O, L91P_YY
I/O	3	W20	-	-	I/O	I/O
I/O, L90N	3	V19	XC2S400E	-	I/O, L90N_Y	I/O, L90N
I/O, L90P	3	V20	XC2S400E	-	I/O, L90P_Y	I/O, L90P
I/O, L89N	3	V21	XC2S600E	XC2S600E	-	I/O, VREF Bank 3, L89N_Y
I/O, L89P	3	V22	XC2S600E	-	I/O	I/O, L89P_Y
I/O	3	V23	-	-	I/O	I/O
I/O, L88N_YY	3	V24	All	-	I/O, L88N_YY	I/O, L88N_YY

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, VREF Bank 1, L25P	1	D14	XC2S600E	All	I/O, VREF Bank 1, L25P	I/O, VREF Bank 1, L25P_Y
I/O, L25N	1	C14	XC2S600E	-	I/O, L25N	I/O, L25N_Y
I/O	1	J13	-	-	-	I/O
I/O, L24P	1	C13	-	-	I/O, L24P	I/O, L24P
I/O, L24N	1	D13	-	-	I/O, L24N	I/O, L24N
I/O	1	H13	-	-	-	I/O
I/O (DLL), L23P	1	B14	-	-	I/O (DLL), L23P	I/O (DLL), L23P
GCK2, I	1	A14	-	-	GCK2, I	GCK2, I
GCK3, I	0	A13	-	-	GCK3, I	GCK3, I
I/O (DLL), L23N	0	B13	-	-	I/O (DLL), L23N	I/O (DLL), L23N
I/O	0	E13	-	-	-	I/O
I/O, L22P_YY	0	F13	All	-	I/O, L22P_YY	I/O, L22P_YY
I/O, L22N_YY	0	G13	All	-	I/O, L22N_YY	I/O, L22N_YY
I/O, L21P	0	A12	XC2S600E	-	-	I/O, L21P_Y
I/O, VREF Bank 0, L21N	0	B12	XC2S600E	All	I/O, VREF Bank 0	I/O, VREF Bank 0, L21N_Y
I/O, L20P	0	D12	XC2S600E	-	I/O, L20P	I/O, L20P_Y
I/O, L20N	0	E12	XC2S600E	-	I/O, L20N	I/O, L20N_Y
I/O	0	F12	-	-	-	I/O
I/O, L19P_YY	0	G12	All	-	I/O, L19P_YY	I/O, L19P_YY
I/O, L19N_YY	0	H12	All	-	I/O, L19N_YY	I/O, L19N_YY
I/O	0	J12	-	-	-	I/O
I/O, L18P_YY	0	A11	All	-	I/O, L18P_YY	I/O, L18P_YY
I/O, VREF Bank 0, L18N_YY	0	B11	All	All	I/O, VREF Bank 0, L18N_YY	I/O, VREF Bank 0, L18N_YY
I/O, L17P_YY	0	E11	All	-	I/O, L17P_YY	I/O, L17P_YY
I/O, L17N_YY	0	F11	All	-	I/O, L17N_YY	I/O, L17N_YY
I/O	0	C11	-	-	-	I/O
I/O, L16P	0	G11	-	-	I/O, L16P	I/O, L16P
I/O, L16N	0	H11	-	-	I/O, L16N	I/O, L16N
I/O	0	C10	-	-	-	I/O
I/O, L15P_YY	0	A10	All	-	I/O, L15P_YY	I/O, L15P_YY
I/O, L15N_YY	0	B10	All	-	I/O, L15N_YY	I/O, L15N_YY
I/O, L14P_YY	0	D10	All	-	I/O, L14P_YY	I/O, L14P_YY