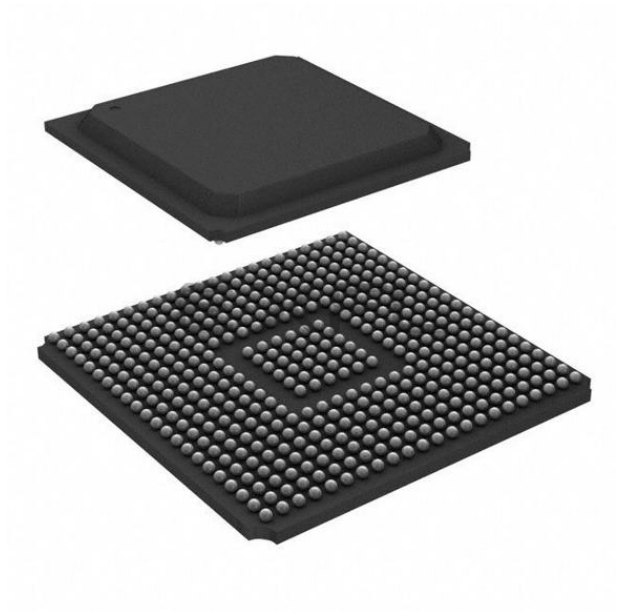
AMD Xilinx - XC2S200E-6FGG456C Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1176
Number of Logic Elements/Cells	5292
Total RAM Bits	57344
Number of I/O	289
Number of Gates	200000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s200e-6fgg456c

edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

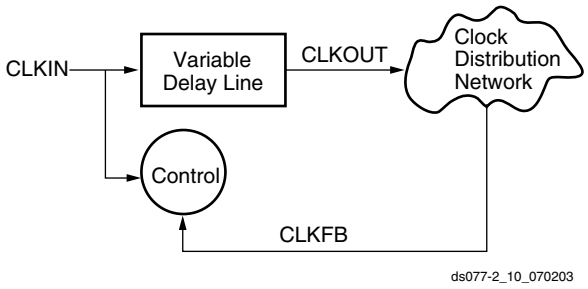


Figure 12: **Delay-Locked Loop Block Diagram**

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16. The phase-shifted output have optional duty-cycle correction (Figure 13).

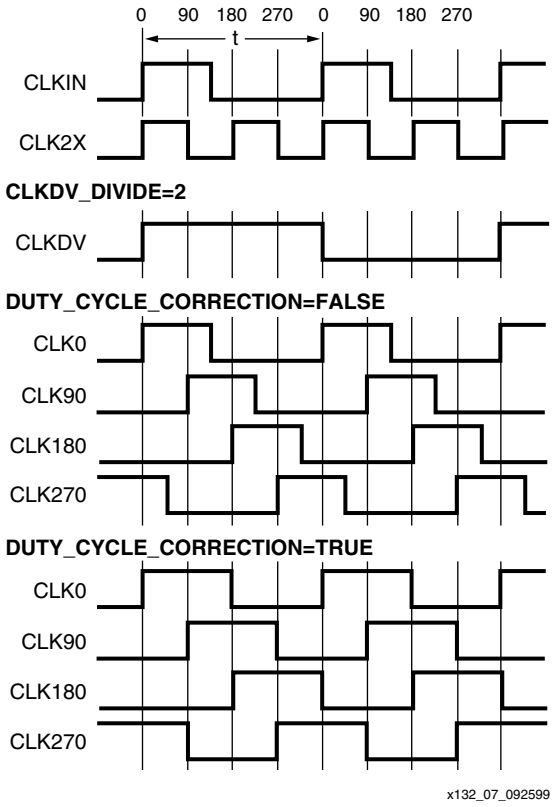


Figure 13: **DLL Output Characteristics**

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to deskew a board level clock among multiple Spartan-IIE devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock. If the DLL uses external feedback, apply a reset after startup to ensure consistent locking to the external signal. See Xilinx Application Note XAPP174 for more information on DLLs.

Boundary Scan

Spartan-IIE devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, and HIGHZ instructions. The TAP also supports two USERCODE instructions, internal scan chains, and configuration/readback of the device.

The TAP uses dedicated package pins that always operate using LVTTL. For TDO to operate using LVTTL, the V_{CCO} for Bank 2 must be 3.3V. Otherwise, TDO switches rail-to-rail between ground and V_{CCO}. The boundary-scan input pins (TDI, TMS, TCK) do not have a V_{CCO} requirement and operate with either 2.5V or 3.3V input signaling levels. TDI, TMS, and TCK hava a default internal weak pull-up resistor, and TDO has no default resistor. Bitstream options allow setting any of the four TAP pins to have an internal pull-up, pull-down, or neither.

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including unbonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections.

Table 8 lists the boundary-scan instructions supported in Spartan-IIE FPGAs. Internal signals can be captured during EXTEST by connecting them to unbonded or unused IOBs. They may also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Table 8: **Boundary-Scan Instructions**

Boundary-Scan Command	Binary Code[4:0]	Description
EXTEST	00000	Enables boundary-scan EXTEST operation
SAMPLE/ PRELOAD	00001	Enables boundary-scan SAMPLE/PRELOAD operation
USER1	00010	Access user-defined register 1
USER2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for Readback
CFG_IN	00101	Access the configuration bus for Configuration

Table 8: **Boundary-Scan Instructions *(Continued)***

Boundary-Scan Command	Binary Code[4:0]	Description
INTEST	00111	Enables boundary-scan INTEST operation
USERCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIGHZ	01010	Disables output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions

The public boundary-scan instructions are available prior to configuration, except for USER1 and USER2. After configuration, the public instructions remain available together with any USERCODE instructions installed during the configuration. While the SAMPLE/PRELOAD and BYPASS instructions are available during configuration, it is recommended that boundary-scan operations not be performed during this transitional period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

To facilitate internal scan chains, the User Register provides three outputs (Reset, Update, and Shift) that represent the corresponding states in the boundary-scan internal state machine.

Figure 14 is a diagram of the Spartan-IIE family boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

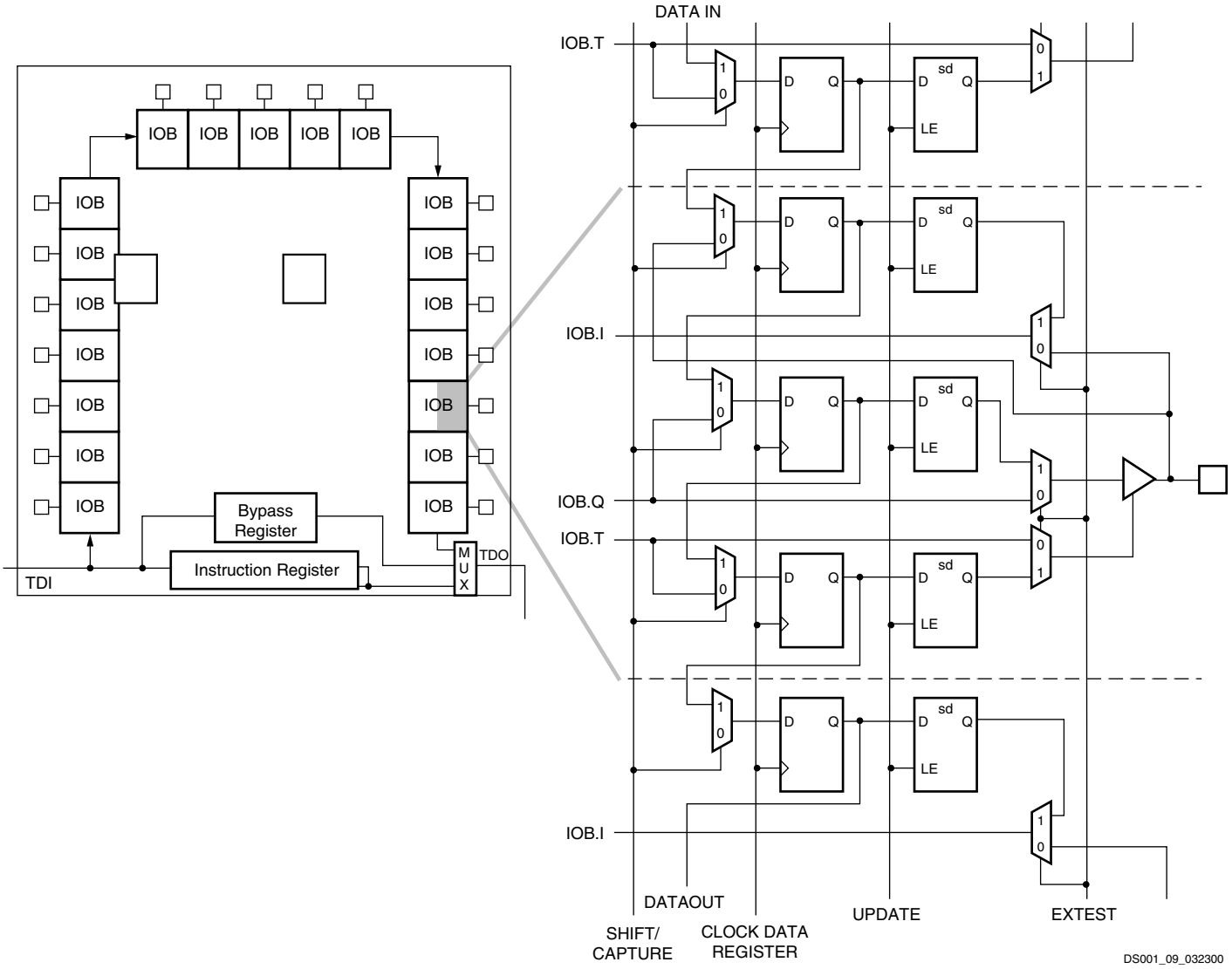


Figure 14: **Spartan-IIE Family Boundary Scan Logic**

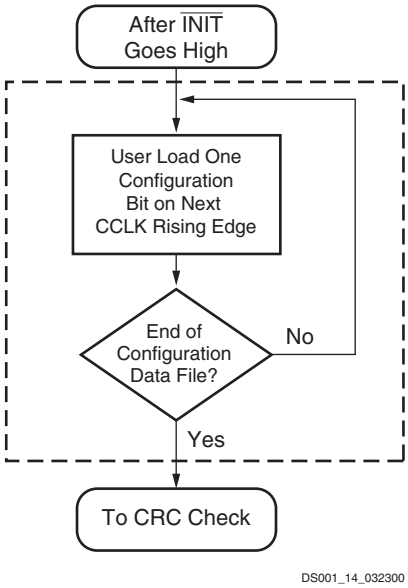


Figure 18: **Loading Serial Mode Configuration Data**

Slave Serial Mode

In Slave Serial mode, the FPGA's CCLK pin is driven by an external source, allowing the FPGA to be configured from other logic devices such as microprocessors or in a daisy-chain configuration. Figure 19 shows connections for a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-IIE device in slave serial mode should be connected as shown for the third device from the left. Slave Serial mode is selected by a <11x> on the mode pins (M0, M1, M2). The weak pull-ups on the mode pins make slave serial the default mode if the pins are left unconnected.

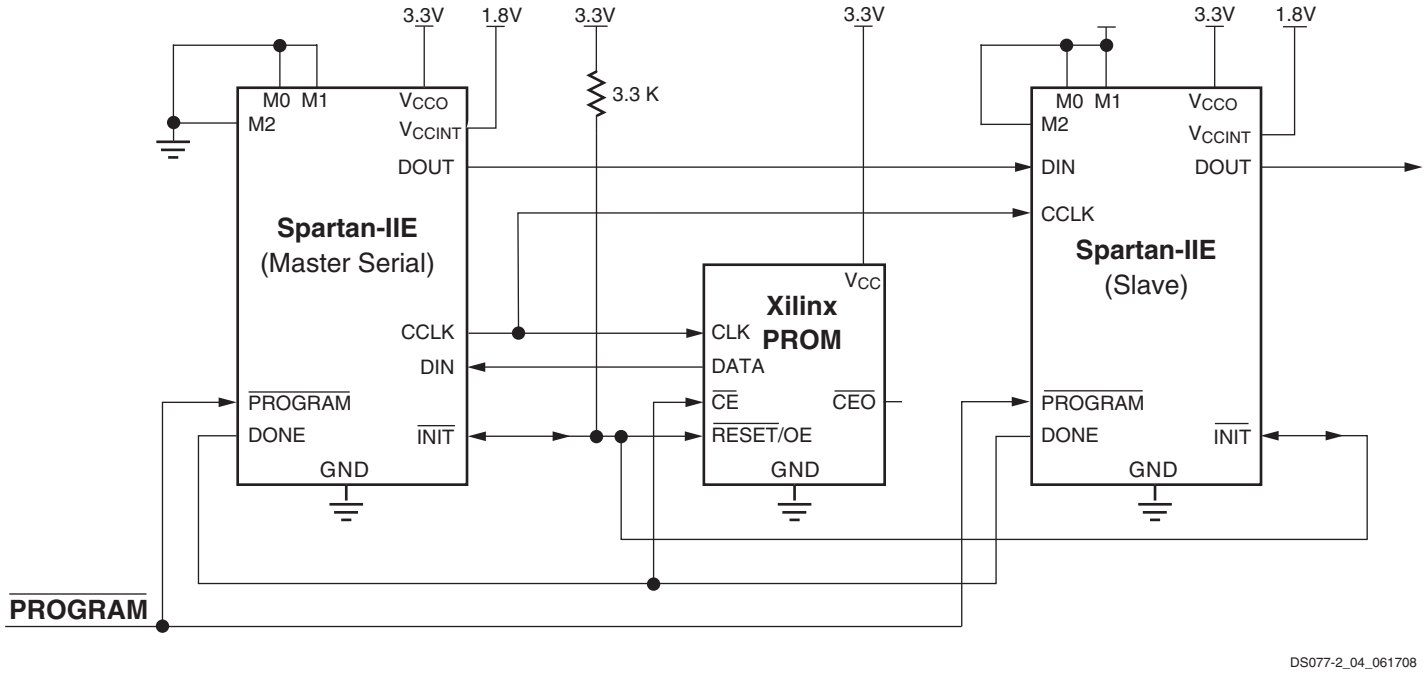
The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

Timing for Slave Serial mode is shown in Figure 24, page 49.

Daisy Chain

Multiple FPGAs in Slave Serial mode can be daisy-chained for configuration from a single source. After an FPGA is configured, data for the next device is sent to the DOUT pin. Data on the DOUT pin changes on the rising edge of CCLK. Note that DOUT changes on the falling edge of CCLK for some Xilinx families but mixed daisy chains are allowed. Configuration must be delayed until $\overline{\text{INIT}}$ pins of all daisy-chained FPGAs are High. For more information, see Start-up, page 23.

The maximum amount of data that can be sent to the DOUT pin for a serial daisy chain is 2^{20}-1 (1,048,575) 32-bit words, or 33,554,400 bits, which is approximately 8 XC2S600E bitstreams. The configuration bitstream of downstream devices is limited to this size.



Notes:
1. If the DriveDone configuration option is not active for any of the FPGAs, pull up DONE with a 330Ω resistor.

Figure 19: **Master/Slave Serial Configuration Circuit Diagram**

Revision History

Date	Version	Description
11/15/2001	1.0	Initial Xilinx release.
11/18/2002	2.0	Added XC2S400E and XC2S600E. Removed Preliminary designation. Clarified details of I/O standards, boundary scan, and configuration.
07/09/2003	2.1	Added hot swap description (see Hot Swap, Hot Insertion, Hot Socketing Support). Added Table 9 containing JTAG IDCODE values. Clarified configuration PROM support.
06/18/2008	2.3	Added note that TDI, TMS, and TCK have a default pull-up resistor. Add note on maximum daisy-chain limit. Updated Figure 19 since Mode pins can be pulled up to either 2.5V or 3.3V. Updated all modules for continuous page, figure, and table numbering. Updated links. Synchronized all modules to v2.3.
08/09/2013	3.0	This product is obsolete/discontinued per XCN12026.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
T_J	Junction temperature	Commercial	0	85	°C
		Industrial	–40	100	°C
V_{CCINT}	Supply voltage relative to GND(1)	Commercial	1.8 – 5%	1.8 + 5%	V
		Industrial	1.8 – 5%	1.8 + 5%	V
V_{CCO}	Supply voltage relative to GND(2)	Commercial	1.2	3.6	V
		Industrial	1.2	3.6	V
T_{IN}	Input signal transition time(3)		-	250	ns

Notes:
1. Functional operation is guaranteed down to a minimum V_{CCINT} of 1.62V (Nominal V_{CCINT} –10%). For every 50 mV reduction in V_{CCINT} below 1.71V (nominal V_{CCINT} –5%), all delay parameters increase by approximately 3%.
2. Minimum and maximum values for V_{CCO} vary according to the I/O standard selected.
3. Input and output measurement threshold is ~50% of V_{CCO}. See Delay Measurement Methodology, page 41 for specific details.

DC Characteristics Over Operating Conditions

Symbol	Description			Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data may be lost)			1.5	-	-	V
V_{DRIO}	Data retention V_{CCO} voltage (below which configuration data may be lost)			1.2	-	-	V
I_{CCINTQ}	Quiescent V_{CCINT} supply current(1)	XC2S50E	Commercial	-	10	200	mA
			Industrial	-	10	200	mA
		XC2S100E	Commercial	-	10	200	mA
			Industrial	-	10	200	mA
		XC2S150E	Commercial	-	10	300	mA
			Industrial	-	10	300	mA
		XC2S200E	Commercial	-	10	300	mA
			Industrial	-	10	300	mA
		XC2S300E	Commercial	-	12	300	mA
			Industrial	-	12	300	mA
		XC2S400E	Commercial	-	15	300	mA
			Industrial	-	15	300	mA
		XC2S600E	Commercial	-	15	400	mA
			Industrial	-	15	400	mA
I_{CCOQ}	Quiescent V_{CCO} supply current(1)			-	-	2	mA
I_{REF}	V_{REF} current per V_{REF} pin			-	-	20	µA
I_L	Input or output leakage current per pin			–10	-	+10	µA
C_{IN}	Input capacitance (sample tested)	TQ, PQ, FG, FT packages		-	-	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V (sample tested)(2)			-	-	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.6V (sample tested)(2)			-	-	0.25	mA

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not provide valid logic levels when input pins are connected to other circuits.

IOB Input Switching Characteristics(1)

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in IOB Input Delay Adjustments for Different Standards, page 38.

Symbol	Description	Device	Speed Grade				Units
			-7		-6		
			Min	Max	Min	Max	
Propagation Delays							
T_{IOPI}	Pad to I output, no delay	All	0.4	0.8	0.4	0.8	ns
T_{IOPID}	Pad to I output, with delay	All	0.5	1.0	0.5	1.0	ns
T_{IOPLI}	Pad to output IQ via transparent latch, no delay	All	0.7	1.5	0.7	1.6	ns
T_{IOPLID}	Pad to output IQ via transparent latch, with delay	XC2S50E	1.3	3.0	1.3	3.1	ns
		XC2S100E	1.3	3.0	1.3	3.1	ns
		XC2S150E	1.3	3.2	1.3	3.3	ns
		XC2S200E	1.3	3.2	1.3	3.3	ns
		XC2S300E	1.3	3.2	1.3	3.3	ns
		XC2S400E	1.4	3.2	1.4	3.4	ns
		XC2S600E	1.5	3.5	1.5	3.7	ns
Sequential Delays							
T_{IOCKIQ}	Clock CLK to output IQ	All	0.1	0.7	0.1	0.7	ns
Setup/Hold Times with Respect to Clock CLK							
T_{IOPICK} / T_{IOICKP}	Pad, no delay	All	1.4 / 0	-	1.5 / 0	-	ns
$T_{IOPICKD}$ / $T_{IOICKPD}$	Pad, with delay	XC2S50E	2.9 / 0	-	2.9 / 0	-	ns
		XC2S100E	2.9 / 0	-	2.9 / 0	-	ns
		XC2S150E	3.1 / 0	-	3.1 / 0	-	ns
		XC2S200E	3.1 / 0	-	3.1 / 0	-	ns
		XC2S300E	3.1 / 0	-	3.1 / 0	-	ns
		XC2S400E	3.2 / 0	-	3.2 / 0	-	ns
		XC2S600E	3.5 / 0	-	3.5 / 0	-	ns
$T_{IOICECK}$ / $T_{IOCKICE}$	ICE input	All	0.7 / 0.01	-	0.7 / 0.01	-	ns
Set/Reset Delays							
$T_{IOSRCKI}$	SR input (IFF, synchronous)	All	0.9	-	1.0	-	ns
T_{IOSRIQ}	SR input to IQ (asynchronous)	All	0.5	1.2	0.5	1.4	ns
T_{GSRQ}	GSR to output IQ	All	3.8	8.5	3.8	9.7	ns

Notes:
1. Input timing for LVTTL is measured at 1.4V. For other I/O standards, see the table Delay Measurement Methodology, page 41.

Clock Distribution Switching Characteristics

T_{GPIO} is specified for LVTTL levels. For other standards, adjust T_{GPIO} with the values shown in I/O Standard Global Clock Input Adjustments.

Symbol	Description	Speed Grade		Units
		-7	-6	
		Max	Max	
GCLK IOB and Buffer				
T_{GPIO}	Global clock pad to output	0.7	0.7	ns
T_{GIO}	Global clock buffer I input to O output	0.45	0.5	ns

I/O Standard Global Clock Input Adjustments

Delays associated with a global clock input pad are specified for LVTTL levels. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade		Units
			-7	-6	
Data Input Delay Adjustments					
$T_{GPLVTTL}$	Standard-specific global clock input delay adjustments	LVTTL	0	0	ns
$T_{GPLVCMOS2}$		LVCMOS2	0	0	ns
$T_{GPLVCMOS18}$		LVCMOS18	0.2	0.2	ns
$T_{GPLVCDS}$		LVDS	0.38	0.38	ns
$T_{GPLVPECL}$		LVCPECL	0.38	0.38	ns
$T_{GPPCI33\_3}$		PCI, 33 MHz, 3.3V	0.08	0.08	ns
$T_{GPPCI66\_3}$		PCI, 66 MHz, 3.3V	–0.11	–0.11	ns
T_{GPGTL}		GTL	0.37	0.37	ns
T_{GPGTLP}		GTL+	0.37	0.37	ns
T_{GPHSTL}		HSTL	0.27	0.27	ns
$T_{GPSSTL2}$		SSTL2	0.27	0.27	ns
$T_{GPSSTL3}$		SSTL3	0.27	0.27	ns
T_{GPCTT}		CTT	0.33	0.33	ns
T_{GPAGP}		AGP	0.27	0.27	ns

Notes:
1. Input timing for GPLVTTL is measured at 1.4V. For other I/O standards, see the table Delay Measurement Methodology, page 41.

DLL Timing Parameters

Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Symbol	Description	F_{CLKIN}	Speed Grade				Units
			-7		-6		
			Min	Max	Min	Max	
$F_{CLKINHF}$	Input clock frequency (CLKDLLHF)	-	60	320	60	275	MHz
$F_{CLKINLF}$	Input clock frequency (CLKDLL)	-	25	160	25	135	MHz
T_{DLLPW}	Input clock pulse width	≥25 MHz	5.0	-	5.0	-	ns
		≥50 MHz	3.0	-	3.0	-	ns
		≥100 MHz	2.4	-	2.4	-	ns
		≥150 MHz	2.0	-	2.0	-	ns
		≥200 MHz	1.8	-	1.8	-	ns
		≥250 MHz	1.5	-	1.5	-	ns
		≥300 MHz	1.3	-	NA	-	

DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications were determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers. Figure 22, page 44, provides definitions for various parameters in the table below.

Symbol	Description	F_{CLKIN}	CLKDLLHF		CLKDLL		Units
			Min	Max	Min	Max	
T_{IPTOL}	Input clock period tolerance		-	1.0	-	1.0	ns
T_{IJITCC}	Input clock jitter tolerance (cycle-to-cycle)		-	±150	-	±300	ps
T_{LOCK}	Time required for DLL to acquire lock(1)	> 60 MHz	-	20	-	20	µs
		50-60 MHz	-	-	-	25	µs
		40-50 MHz	-	-	-	50	µs
		30-40 MHz	-	-	-	90	µs
		25-30 MHz	-	-	-	120	µs
T_{OJITCC}	Output jitter (cycle-to-cycle) for any DLL clock output(2)		-	±60	-	±60	ps
T_{PHIO}	Phase offset between CLKIN and CLKO(3)		-	±100	-	±100	ps
T_{PHOO}	Phase offset between clock outputs on the DLL(4)		-	±140	-	±140	ps
T_{PHIOM}	Phase difference between CLKIN and CLKO(5)		-	±160	-	±160	ps
T_{PHOOM}	Phase difference between clock outputs on the DLL(6)		-	±200	-	±200	ps

Notes:

1. Commercial operating conditions. Add 30% for Industrial operating conditions.
2. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
3. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* output jitter and input clock jitter.
4. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* output jitter and input clock jitter.
5. **Maximum Phase Difference between CLKIN and CLKO** is the sum of output jitter and phase offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
6. **Maximum Phase Difference between Clock Outputs on the DLL** is the sum of output jitter and phase offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Combinatorial Delays						
T_{ILO}	4-input function: F/G inputs to X/Y outputs	0.18	0.42	0.18	0.47	ns
T_{IF5}	5-input function: F/G inputs to F5 output	0.3	0.8	0.3	0.9	ns
T_{IF5X}	5-input function: F/G inputs to X output	0.3	0.8	0.3	0.9	ns
T_{IF6Y}	6-input function: F/G inputs to Y output via F6 MUX	0.3	0.9	0.3	1.0	ns
T_{F5INY}	6-input function: F5IN input to Y output	0.04	0.2	0.04	0.22	ns
T_{IFNCTL}	Incremental delay routing through transparent latch to XQ/YQ outputs	-	0.7	-	0.8	ns
T_{BYYB}	BY input to YB output	0.18	0.46	0.18	0.51	ns
Sequential Delays						
T_{CKO}	FF clock CLK to XQ/YQ outputs	0.3	0.9	0.3	1.0	ns
T_{CKLO}	Latch clock CLK to XQ/YQ outputs	0.3	0.9	0.3	1.0	ns
Setup/Hold Times with Respect to Clock CLK						
T_{ICK} / T_{CKI}	4-input function: F/G inputs	1.0 / 0	-	1.1 / 0	-	ns
T_{IF5CK} / T_{CKIF5}	5-input function: F/G inputs	1.4 / 0	-	1.5 / 0	-	ns
T_{F5INCK} / T_{CKF5IN}	6-input function: F5IN input	0.8 / 0	-	0.8 / 0	-	ns
T_{IF6CK} / T_{CKIF6}	6-input function: F/G inputs via F6 MUX	1.5 / 0	-	1.6 / 0	-	ns
T_{DICK} / T_{CKDI}	BX/BY inputs	0.7 / 0	-	0.8 / 0	-	ns
T_{CECK} / T_{CKCE}	CE input	0.7 / 0	-	0.7 / 0	-	ns
T_{RCK} / T_{CKR}	SR/BY inputs (synchronous)	0.52 / 0	-	0.6 / 0	-	ns
Clock CLK						
T_{CH}	Pulse width, High	1.3	-	1.4	-	ns
T_{CL}	Pulse width, Low	1.3	-	1.4	-	ns
Set/Reset						
T_{RPW}	Pulse width, SR/BY inputs	2.1	-	2.4	-	ns
T_{RQ}	Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	0.3	0.9	0.3	1.0	ns
F_{TOG}	Toggle frequency (for export control)	-	400	-	357	MHz

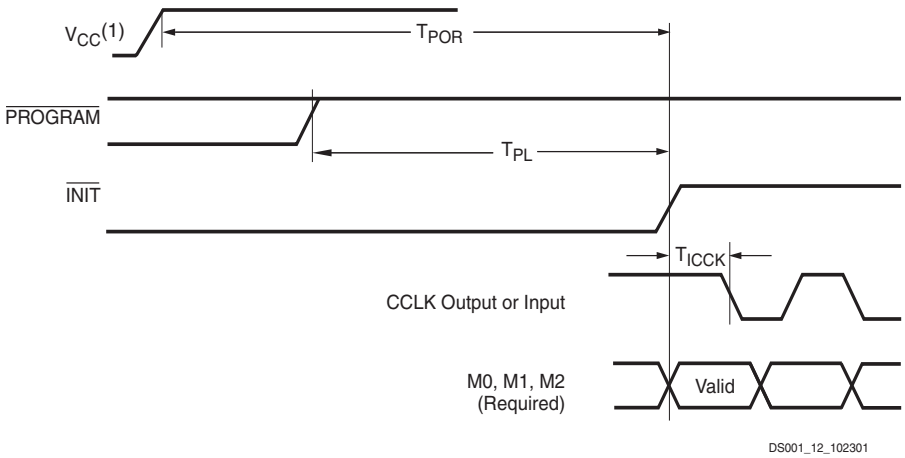
TBUF Switching Characteristics

Symbol	Description	Speed Grade		Units
		-7	-6	
		Max	Max	
T_{IO}	IN input to OUT output	0	0	ns
T_{OFF}	TRI input to OUT output high impedance	0.1	0.11	ns
T_{ON}	TRI input to valid data on OUT output	0.1	0.11	ns

JTAG Test Access Port Switching Characteristics

Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Setup/Hold Times with Respect to TCK						
T_{TAPTCK} / T_{TCKTAP}	TMS and TDI setup times and hold times	4.0 / 2.0	-	4.0 / 2.0	-	ns
Sequential Delays						
T_{TCKTDO}	Output delay from clock TCK to output TDO	-	11.0	-	11.0	ns
FTCK	TCK clock frequency	-	33	-	33	MHz

Configuration Switching Characteristics



Symbol	Description	All Devices		Units
		Min	Max	
T_{POR}	Power-on reset	-	2	ms
T_{PL}	Program latency	-	100	µs
T_{ICCK}	CCLK output delay (Master serial mode only)	0.5	4	µs
$T_{PROGRAM}$	Program pulse width	300	-	ns

Notes:
1. Before configuration can begin, V_{CCINT} and V_{CCO} Bank 2 must reach the recommended operating voltage.

Figure 23: **Configuration Timing on Power-Up**

Revision History

Date	Version	Description
11/15/2001	1.0	Initial Xilinx release.
06/28/2002	1.1	Added -7 speed grade and extended DLL specs to Industrial.
11/18/2002	2.0	Added XC2S400E and XC2S600E. Added minimum specifications. Added reference to XAPP450 for Power-On Requirements. Removed Preliminary designation.
07/09/2003	2.1	Added I_{CCINTQ} typical values. Reduced ICCPO power-on current requirements. Relaxed TCCPO power-on ramp requirements. Added IHSPO to describe current in hot-swap applications. Updated TPSFD / TPHFD description to indicate use of delay element.
06/18/2008	2.3	Updated I/O measurement thresholds. Updated all modules for continuous page, figure, and table numbering. Updated links. Synchronized all modules to v2.3.
08/09/2013	3.0	This product is obsolete/discontinued per XCN12026.

Pin Definitions *(Continued)*

Pad Name	Dedicated Pin	Direction	Description
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In Slave Parallel mode, D0-D7 are configuration data input pins. During readback, D0-D7 are output pins. These pins become user I/Os after configuration unless the Slave Parallel port is retained. In serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
$\overline{WRITE}$	No	Input	In Slave Parallel mode, the active-low Write Enable signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
$\overline{CS}$	No	Input	In Slave Parallel mode, the active-low Chip Select signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary Scan Test Access Port pins (IEEE 1149.1).
V_{CCINT}	Yes	Input	1.8V power supply pins for the internal core logic.
V_{CCO}	Yes	Input	Power supply pins for output drivers (1.5V, 1.8V, 2.5V, or 3.3V subject to banking rules in the Functional Description module.
V_{REF}	No	Input	Input threshold reference voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules in the Functional Description module.
GND	Yes	Input	Ground. All must be connected.
IRDY, TRDY	No	See PCI core documentation	These signals can only be accessed when using Xilinx PCI cores. If the cores are not used, these pins are available as user I/Os.
L#[P/N] (e.g., L0P)	No	Bidirectional	Differential I/O with synchronous output. P = positive, N = negative. The number (#) is used to associate the two pins of a differential pair. Becomes a general user I/O when not needed for differential signals.
L#[P/N]_Y (e.g., L0P_Y)	No	Bidirectional	Differential I/O with asynchronous or synchronous output (asynchronous output not compatible for all densities in a package). P = positive, N = negative. The number (#) is used to associate the two pins of a differential pair. Becomes a general user I/O when not needed for differential signals.
L#[P/N]_YY (e.g., L0P_YY)	No	Bidirectional	Differential I/O with asynchronous or synchronous output (compatible for all densities in a package). P = positive, N = negative. The number (#) is used to associate the two pins of a differential pair. Becomes a general user I/O when not needed for differential signals.
I/O	No	Bidirectional	These pins can be configured to be input and/or output after configuration is completed. Unused I/Os are disabled with a weak pull-down resistor. After power-on and before configuration is completed, these pins are either pulled up or left floating according to the Mode pin values. See the DC and Switching Characteristics module for power-on characteristics.

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L51P	4	N9	XC2S50E, 150E, 200E, 400E	-
I/O, L50N	4	T10	XC2S50E, 200E, 300E, 400E	-
I/O, VREF Bank 4, L50P	4	R10	XC2S50E, 200E, 300E, 400E	All
I/O, L49N	4	P10	XC2S50E, 200E, 300E, 400E	-
I/O, L49P	4	R11	XC2S50E, 200E, 300E, 400E	-
I/O	4	T11	-	-
I/O, L48N	4	N10	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L48P	4	M10	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L47N	4	P11	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L47P	4	R12	XC2S50E, 100E, 200E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L46N	4	T12	XC2S50E, 100E, 150E, 300E	-
I/O, L46P	4	T13	XC2S50E, 100E, 150E, 300E	-
I/O, L45N_YY	4	N11	All	-
I/O, VREF Bank 4, L45P_YY	4	M11	All	All
I/O, L44N_YY	4	P12	All	-
I/O, L44P_YY	4	N12	All	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L43N	4	R13	XC2S50E, 150E	XC2S200E, 300E, 400E
I/O, L43P	4	P13	XC2S50E, 150E	-
I/O, L42N_YY	4	T14	All	-
I/O, L42P_YY	4	R14	All	-
DONE	3	T15	-	-
$\overline{\text{PROGRAM}}$	-	R16	-	-
I/O ($\overline{\text{INIT}}$), L41N_YY	3	P15	All	-
I/O (D7), L41P_YY	3	P16	All	-
I/O, L40N	3	N15	XC2S100E, 150E, 400E	-
I/O, L40P	3	N16	XC2S100E, 150E, 400E	XC2S200E, 300E, 400E
I/O, L39N	3	N14	XC2S50E, 100E, 150E, 200E, 300E(1)	-
I/O, L39P	3	M14	XC2S50E, 100E, 150E, 200E, 300E(1)	-
I/O, VREF Bank 3, L38N	3	M15	XC2S50E, 150E, 200E, 300E, 400E	All
I/O, L38P	3	M16	XC2S50E, 150E, 200E, 300E, 400E	-
I/O(2)	3	M13	-	-
I/O(2)	3	L14	-	-
I/O, L36N	3	L15	XC2S50E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O (D6), L36P	3	L16	XC2S50E, 300E, 400E	-

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
TMS	-	E4	-	-	TMS	TMS	TMS	TMS	TMS	TMS
I/O	7	D3	XC2S150E	-	I/O	I/O, L113P_Y	I/O	I/O	I/O	I/O
I/O	7	C2	-	-	-	-	-	I/O	I/O	I/O
I/O	7	C1	XC2S150E	-	-	I/O, L113N_Y	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	D2	XC2S150E, 200E, 300E, 400E	-	-	I/O, L112P_Y	I/O, L119P_Y	I/O, L119P_Y	I/O, L119P_Y	I/O, L119P
I/O, L#N_Y	7	D1	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L112N_Y	I/O, L119N_Y	I/O, L119N_Y	I/O, L119N_Y	I/O, L119N
I/O, L#P_Y	7	E2	XC2S100E, 200E, 300E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L85P_Y	I/O, L111P	I/O, VREF Bank 7, L118P_Y	I/O, VREF Bank 7, L118P_Y	I/O, VREF Bank 7, L118P	I/O, VREF Bank 7, L118P_Y
I/O, L#N_Y	7	E3	XC2S100E, 200E, 300E, 600E	-	I/O, L85N_Y	I/O, L111N	I/O, L118N_Y	I/O, L118N_Y	I/O, L118N	I/O, L118N_Y
I/O	7	E1	-	-	-	-	-	I/O	I/O	I/O
I/O	7	F5	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	F4	XC2S100E, 200E, 300E, 600E	-	I/O, L84P_Y	I/O, L110P	I/O, L117P_Y	I/O, L117P_Y	I/O, L117P	I/O, L117P_Y
I/O, L#N_Y	7	F3	XC2S100E, 200E, 300E, 600E	-	I/O, L84N_Y	I/O, L110N	I/O, L117N_Y	I/O, L117N_Y	I/O, L117N	I/O, L117N_Y
I/O, VREF Bank 7, L#P_Y	7	F2	XC2S150E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 7, L83P	I/O, VREF Bank 7, L109P_Y	I/O, VREF Bank 7, L116P_Y	I/O, VREF Bank 7, L116P_Y	I/O, VREF Bank 7, L116P_Y	I/O, VREF Bank 7, L116P_Y
I/O, L#N_Y	7	F1	XC2S150E, 200E, 300E, 400E, 600E	-	I/O, L83N	I/O, L109N_Y	I/O, L116N_Y	I/O, L116N_Y	I/O, L116N_Y	I/O, L116N_Y
I/O	7	G5	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	G4	XC2S150E, 200E, 300E, 400E	-	-	I/O, L108P_Y	I/O, L115P_Y	I/O, L115P_Y	I/O, L115P_Y	I/O, L115P
I/O, L#N_Y	7	G3	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L108N_Y	I/O, L115N_Y	I/O, L115N_Y	I/O, L115N_Y	I/O, L115N
I/O, L#P_Y	7	G2	XC2S100E, 150E, 300E, 600E	XC2S600E	I/O, L82P_Y	I/O, L107P_Y	I/O, L114P	I/O, L114P_Y	I/O, L114P	I/O, VREF Bank 7, L114P_Y
I/O, L#N_Y	7	G1	XC2S100E, 150E, 300E, 600E	-	I/O, L82N_Y	I/O, L107N_Y	I/O, L114N	I/O, L114N_Y	I/O, L114N	I/O, L114N_Y

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
M0	-	AA1	-	-	M0	M0	M0	M0	M0	M0
M2	-	AB2	-	-	M2	M2	M2	M2	M2	M2
I/O, L#N_Y	5	AA3	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L84N_Y	I/O, L89N_Y	I/O, L89N_Y	I/O, L89N_Y	I/O, L89N_Y
I/O, L#P_Y	5	AB3	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L84P_Y	I/O, L89P_Y	I/O, L89P_Y	I/O, L89P_Y	I/O, L89P_Y
I/O	5	AB4	-	-	-	-	-	I/O	I/O	I/O
I/O	5	AA5	XC2S100E, 150E	-	I/O, L63N_Y	I/O, L83N_Y	I/O	I/O	I/O	I/O
I/O, L#N_Y	5	W5	XC2S100E, 150E, 200E, 300E, 400E, 600E	-	I/O, L63P_Y	I/O, L83P_Y	I/O, L88N_Y	I/O, L88N_Y	I/O, L88N_Y	I/O, L88N_Y
I/O, L#P_Y	5	Y5	XC2S200E, 300E, 400E, 600E	-	I/O	I/O	I/O, L88P_Y	I/O, L88P_Y	I/O, L88P_Y	I/O, L88P_Y
I/O, L#N_Y	5	AB5	XC2S100E, 200E, 300E, 400E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L62N_Y	I/O, L82N	I/O, VREF Bank 5, L87N_Y	I/O, VREF Bank 5, L87N_Y	I/O, VREF Bank 5, L87N_Y	I/O, VREF Bank 5, L87N_Y
I/O, L#P_Y	5	AB6	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L62P_Y	I/O, L82P	I/O, L87P_Y	I/O, L87P_Y	I/O, L87P_Y	I/O, L87P_Y
I/O	5	Y6	-	-	-	-	-	I/O	I/O	I/O
I/O	5	AA6	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N_YY	5	V6	All	-	I/O, L61N_YY	I/O, L81N_YY	I/O, L86N_YY	I/O, L86N_YY	I/O, L86N_YY	I/O, L86N_YY
I/O, L#P_YY	5	W6	All	-	I/O, L61P_YY	I/O, L81P_YY	I/O, L86P_YY	I/O, L86P_YY	I/O, L86P_YY	I/O, L86P_YY
I/O, VREF Bank 5, L#N_YY	5	AB7	All	All	I/O, VREF Bank 5, L60N_YY	I/O, VREF Bank 5, L80N_YY	I/O, VREF Bank 5, L85N_YY	I/O, VREF Bank 5, L85N_YY	I/O, VREF Bank 5, L85N_YY	I/O, VREF Bank 5, L85N_YY
I/O, L#P_YY	5	AA7	All	-	I/O, L60P_YY	I/O, L80P_YY	I/O, L85P_YY	I/O, L85P_YY	I/O, L85P_YY	I/O, L85P_YY
I/O	5	Y7	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N_Y	5	V7	XC2S300E, 600E	-	-	I/O, L79N	I/O, L84N	I/O, L84N_Y	I/O, L84N	I/O, L84N_Y
I/O, L#P_Y	5	W7	XC2S300E, 600E	-	I/O	I/O, L79P	I/O, L84P	I/O, L84P_Y	I/O, L84P	I/O, L84P_Y
I/O, L#N_Y	5	AB8	XC2S100E, 300E, 600E	XC2S600E	I/O, L59N_Y	I/O, L78N	I/O, L83N	I/O, L83N_Y	I/O, L83N	I/O, VREF Bank 5, L83N_Y
I/O, L#P_Y	5	AA8	XC2S100E, 300E, 600E	-	I/O, L59P_Y	I/O, L78P	I/O, L83P	I/O, L83P_Y	I/O, L83P	I/O, L83P_Y
I/O	5	Y8	-	-	-	-	-	I/O	I/O	I/O

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
GCK0, I	4	AA12	-	-	GCK0, I	GCK0, I	GCK0, I	GCK0, I	GCK0, I	GCK0, I
I/O (DLL), L#P	4	Y12	-	-	I/O (DLL), L53P	I/O (DLL), L70P	I/O (DLL), L75P	I/O (DLL), L75P	I/O (DLL), L75P	I/O (DLL), L75P
I/O	4	W12	-	-	-	-	-	I/O	I/O	I/O
I/O, L#N	4	V12	XC2S150E, 300E, 600E	-	-	I/O, L69N_Y	I/O, L74N	I/O, L74N_Y	I/O, L74N	I/O, L74N_Y
I/O, L#P	4	U12	XC2S150E, 300E, 600E	XC2S400E, 600E	I/O, L52N	I/O, L69P_Y	I/O, L74P	I/O, L74P_Y	I/O, VREF Bank 4, L74P	I/O, VREF Bank 4, L74P_Y
I/O, L#N	4	AB13	XC2S300E, 600E	-	I/O, L52P	I/O	I/O, L73N	I/O, L73N_Y	I/O, L73N	I/O, L73N_Y
I/O, L#P	4	AA13	XC2S300E, 600E	-	-	-	I/O, L73P	I/O, L73P_Y	I/O, L73P	I/O, L73P_Y
I/O	4	Y13	-	-	-	-	-	I/O	I/O	I/O
I/O, L#N	4	W13	XC2S200E, 300E, 400E, 600E	-	I/O, L51N	I/O, L68N	I/O, L72N_Y	I/O, L72N_Y	I/O, L72N_Y	I/O, L72N_Y
I/O, VREF Bank 4, L#P	4	V13	XC2S200E, 300E, 400E, 600E	All	I/O, VREF Bank 4, L51P	I/O, VREF Bank 4, L68P	I/O, VREF Bank 4, L72P_Y	I/O, VREF Bank 4, L72P_Y	I/O, VREF Bank 4, L72P_Y	I/O, VREF Bank 4, L72P_Y
I/O	4	U13	-	-	I/O, L50N	I/O, L67N	I/O	I/O	I/O	I/O
I/O, L#N	4	AB14	-	-	I/O, L50P	I/O, L67P	I/O, L71N	I/O, L71N	I/O, L71N	I/O, L71N
I/O, L#P	4	AA14	-	-	-	-	I/O, L71P	I/O, L71P	I/O, L71P	I/O, L71P
I/O	4	AB15	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#N	4	Y14	XC2S100E, 150E, 200E	-	I/O, L49N_Y	I/O, L66N_Y	I/O, L70N_Y	I/O, L70N	I/O, L70N	I/O, L70N
I/O, L#P	4	W14	XC2S100E, 150E, 200E	-	I/O, L49P_Y	I/O, L66P_Y	I/O, L70P_Y	I/O, L70P	I/O, L70P	I/O, L70P
I/O, L#N	4	U14	XC2S150E, 200E	-	-	I/O, L65N_Y	I/O, L69N_Y	I/O, L69N	I/O, L69N	I/O, L69N
I/O, L#P	4	V14	XC2S150E, 200E	-	-	I/O, L65P_Y	I/O, L69P_Y	I/O, L69P	I/O, L69P	I/O, L69P
I/O, L#N	4	AA15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L48N_Y	I/O, L64N	I/O, L68N_Y	I/O, L68N_Y	I/O, L68N_Y	I/O, L68N_Y
I/O, L#P	4	Y15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L48P_Y	I/O, L64P	I/O, L68P_Y	I/O, L68P_Y	I/O, L68P_Y	I/O, L68P_Y
I/O, L#N	4	W15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L47N_Y	I/O, L63N	I/O, L67N_Y	I/O, L67N_Y	I/O, L67N_Y	I/O, L67N_Y
I/O, VREF Bank 4, L#P	4	V15	XC2S100E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 4, L47P_Y	I/O, VREF Bank 4, L63P	I/O, VREF Bank 4, L67P_Y	I/O, VREF Bank 4, L67P_Y	I/O, VREF Bank 4, L67P_Y	I/O, VREF Bank 4, L67P_Y
I/O	4	AB16	-	-	-	-	-	I/O	I/O	I/O
I/O	4	AB17	-	-	I/O	I/O	I/O	I/O	I/O	I/O

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O, L#N	3	V19	XC2S150E, 200E, 300E, 400E	-	-	I/O, L54N_Y	I/O, L58N_Y	I/O, L58N_Y	I/O, L58N_Y	I/O, L58N
I/O, L#P	3	V20	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L54P_Y	I/O, L58P_Y	I/O, L58P_Y	I/O, L58P_Y	I/O, L58P
I/O, L#N	3	V22	XC2S100E, 200E, 300E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L40N_Y	I/O, L53N	I/O, VREF Bank 3, L57N_Y	I/O, VREF Bank 3, L57N_Y	I/O, VREF Bank 3, L57N	I/O, VREF Bank 3, L57N_Y
I/O, L#P	3	U22	XC2S100E, 200E, 300E, 600E	-	I/O, L40P_Y	I/O, L53P	I/O, L57P_Y	I/O, L57P_Y	I/O, L57P	I/O, L57P_Y
I/O	3	U21	-	-	-	-	-	I/O	I/O	I/O
I/O	3	U20	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N	3	U18	XC2S100E, 200E, 300E, 600E	-	I/O, L39N_Y	I/O, L52N	I/O, L56N_Y	I/O, L56N_Y	I/O, L56N	I/O, L56N_Y
I/O, L#P	3	U19	XC2S100E, 200E, 300E, 600E	-	I/O, L39P_Y	I/O, L52P	I/O, L56P_Y	I/O, L56P_Y	I/O, L56P	I/O, L56P_Y
I/O, VREF Bank 3, L#N	3	T21	XC2S150E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 3, L38N	I/O, VREF Bank 3, L51N_Y	I/O, VREF Bank 3, L55N_Y	I/O, VREF Bank 3, L55N_Y	I/O, VREF Bank 3, L55N_Y	I/O, VREF Bank 3, L55N_Y
I/O, L#P	3	T22	XC2S150E, 200E, 300E, 400E, 600E	-	I/O, L38P	I/O, L51P_Y	I/O, L55P_Y	I/O, L55P_Y	I/O, L55P_Y	I/O, L55P_Y
I/O	3	T20	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N	3	T18	XC2S150E, 200E, 300E, 400E	-	-	I/O, L50N_Y	I/O, L54N_Y	I/O, L54N_Y	I/O, L54N_Y	I/O, L54N
I/O, L#P	3	T19	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L50P_Y	I/O, L54P_Y	I/O, L54P_Y	I/O, L54P_Y	I/O, L54P
I/O, L#N	3	R21	XC2S100E, 150E, 300E, 600E	XC2S600E	I/O, L37N_Y	I/O, L49N_Y	I/O, L53N	I/O, L53N_Y	I/O, L53N	I/O, VREF Bank 3, L53N_Y
I/O, L#P	3	R22	XC2S100E, 150E, 300E, 600E	-	I/O, L37P_Y	I/O, L49P_Y	I/O, L53P	I/O, L53P_Y	I/O, L53P	I/O, L53P_Y
I/O	3	R20	-	-	-	-	-	I/O	I/O	I/O
I/O, VREF Bank 3, L#N	3	R18	XC2S300E, 400E, 600E	All	I/O, VREF Bank 3, L36N	I/O, VREF Bank 3, L48N	I/O, VREF Bank 3, L52N	I/O, VREF Bank 3, L52N_Y	I/O, VREF Bank 3, L52N_Y	I/O, VREF Bank 3, L52N_Y
I/O (D6), L#P	3	R19	XC2S300E, 400E, 600E	-	I/O (D6), L36P	I/O (D6), L48P	I/O (D6), L52P	I/O (D6), L52P_Y	I/O (D6), L52P_Y	I/O (D6), L52P_Y
I/O (D5), L#N_YY	3	P22	All	-	I/O (D5), L35N_YY	I/O (D5), L47N_YY	I/O (D5), L51N_YY	I/O (D5), L51N_YY	I/O (D5) L51N_YY	I/O (D5), L51N_YY
I/O, L#P_YY	3	P21	All	-	I/O, L35P_YY	I/O, L47P_YY	I/O, L51P_YY	I/O, L51P_YY	I/O, L51P_YY	I/O, L51P_YY

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O, L#P	2	L17	XC2S100E, 150E, 200E, 300E, 600E	XC2S400E, 600E	I/O, L29N_Y	I/O, L40N_Y	I/O, L43P_Y	I/O, L43P_Y	I/O, VREF Bank 2, L43P	I/O, VREF Bank 2, L43P_Y
I/O, L#N	2	K22	XC2S100E, 150E, 300E, 400E	-	I/O, L29P_Y	I/O, L40P_Y	I/O, L42N	I/O, L42N_Y	I/O, L42N_Y	I/O, L42N
I/O, L#P	2	K21	XC2S300E, 400E	-	-	-	I/O, L42P	I/O, L42P_Y	I/O, L42P_Y	I/O, L42P
I/O	2	K20	-	-	-	-	-	I/O	I/O	I/O
I/O (D3)	2	K19	-	-	I/O (D3)	I/O (D3), L39N	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)
I/O, VREF Bank 2, L#N	2	K18	XC2S100E, 200E, 400E	All	I/O, VREF Bank 2, L28N_Y	I/O, VREF Bank 2, L39P	I/O, VREF Bank 2, L41N_Y	I/O, VREF Bank 2, L41N	I/O, VREF Bank 2, L41N_Y	I/O, VREF Bank 2, L41N
I/O, L#P	2	K17	XC2S100, 150E, 200E, 400E	-	I/O, L28P_Y	I/O, L38N_Y	I/O, L41P_Y	I/O, L41P	I/O, L41P_Y	I/O, L41P
I/O, L#N	2	J22	XC2S150E, 300E, 600E	-	I/O	I/O, L38P_Y	I/O, L40N	I/O, L40N_Y	I/O, L40N	I/O, L40N_Y
I/O, L#P	2	J21	XC2S300E, 600E	-	-	-	I/O, L40P	I/O, L40P_Y	I/O, L40P	I/O, L40P_Y
I/O, L#N	2	J20	XC2S150E, 200E, 300E, 600E	-	-	I/O, L37N_Y	I/O, L39N_Y	I/O, L39N_Y	I/O, L39N	I/O, L39N_Y
I/O, L#P	2	J19	XC2S100E, 150E, 200E, 300E, 600E	-	I/O, L27N_Y	I/O, L37P_Y	I/O, L39P_Y	I/O, L39P_Y	I/O, L39P	I/O, L39P_Y
I/O	2	H22	XC2S100E, 150E	-	I/O, L27P_Y	I/O, L36N_Y	I/O	I/O	I/O	I/O
I/O, L#N	2	J18	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L36P_Y	I/O, L38N_Y	I/O, L38N_Y	I/O, L38N_Y	I/O, L38N_Y
I/O, L#P	2	J17	XC2S200E, 300E, 400E, 600E	-	-	-	I/O, L38P_Y	I/O, L38P_Y	I/O, L38P_Y	I/O, L38P_Y
I/O, L#N	2	H21	XC2S150E, 200E, 300E, 400E, 600E	-	I/O	I/O, L35N_Y	I/O, L37N_Y	I/O, L37N_Y	I/O, L37N_Y	I/O, L37N_Y
I/O (D2), L#P	2	H20	XC2S150E, 200E, 300E, 400E, 600E	-	I/O (D2)	I/O (D2), L35P_Y	I/O (D2), L37P_Y	I/O (D2), L37P_Y	I/O (D2), L37P_Y	I/O (D2), L37P_Y
I/O (D1), L#N	2	H19	XC2S300E, 400E, 600E	-	I/O (D1), L26N	I/O (D1), L34N	I/O (D1), L36N	I/O (D1), L36N_Y	I/O (D1), L36N_Y	I/O (D1), L36N_Y
I/O, VREF Bank 2, L#P	2	H18	XC2S300E, 400E, 600E	All	I/O, VREF Bank 2, L26P	I/O, VREF Bank 2, L34P	I/O, VREF Bank 2, L36P	I/O, VREF Bank 2, L36P_Y	I/O, VREF Bank 2, L36P_Y	I/O, VREF Bank 2, L36P_Y
I/O	2	G22	-	-	-	-	-	I/O	I/O	I/O
I/O	2	F22	-	-	I/O	I/O	I/O	I/O	I/O	I/O

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O	4	AC18	-	-	I/O	I/O
I/O, VREF Bank 4, L114N	4	AB18	-	All	I/O, VREF Bank 4, L114N	I/O, VREF Bank 4, L114N
I/O, L114P	4	AA18	-	-	I/O, L114P	I/O, L114P
I/O, L113N	4	Y18	-	-	I/O, L113N	I/O, L113N
I/O, L113P	4	W18	-	-	I/O, L113P	I/O, L113P
I/O	4	AB19	-	-	I/O	I/O
I/O, L112N	4	AF19	XC2S600E	-	I/O	I/O, L112N_Y
I/O, L112P	4	AE19	XC2S600E	XC2S600E	-	I/O, VREF Bank 4, L112P_Y
I/O, L111N	4	AA19	XC2S600E	-	I/O, L111N	I/O, L111N_Y
I/O, L111P	4	Y19	XC2S600E	-	I/O, L111P	I/O, L111P_Y
I/O	4	AF20	-	-	-	I/O
I/O, L110N	4	AE20	XC2S600E	-	I/O, L110N	I/O, L110N_Y
I/O, L110P	4	AD20	XC2S600E	-	I/O, L110P	I/O, L110P_Y
I/O	4	AC20	-	-	I/O	I/O
I/O, L109N_YY	4	AB20	All	-	I/O, L109N_YY	I/O, L109N_YY
I/O, VREF Bank 4, L109P_YY	4	AA20	All	All	I/O, VREF Bank 4, L109P_YY	I/O, VREF Bank 4, L109P_YY
I/O	4	Y20	-	-	I/O	I/O
I/O, L108N	4	AF21	-	-	I/O, L108N	I/O, L108N
I/O, L108P	4	AE21	-	-	I/O, L108P	I/O, L108P
I/O, L107N	4	AD21	-	-	I/O, L107N	I/O, L107N
I/O, L107P	4	AC21	-	-	I/O, L107P	I/O, L107P
I/O	4	AC22	-	-	-	I/O
I/O, L106N_YY	4	AF22	All	-	I/O, L106N_YY	I/O, L106N_YY
I/O, VREF Bank 4, L106P_YY	4	AE22	All	All	I/O, VREF Bank 4, L106P_YY	I/O, VREF Bank 4, L106P_YY
I/O, L105N_YY	4	AB21	All	-	I/O, L105N_YY	I/O, L105N_YY
I/O, L105P_YY	4	AA21	All	-	I/O, L105P_YY	I/O, L105P_YY
I/O, L104N_YY	4	AF23	All	-	I/O, L104N_YY	I/O, L104N_YY
I/O, L104P_YY	4	AE23	All	-	I/O, L104P_YY	I/O, L104P_YY
I/O, L103N	4	AD23	XC2S600E	-	I/O	I/O, L103N_Y
I/O, L103P	4	AE24	XC2S600E	-	-	I/O, L103P_Y
I/O, L102N_YY	4	AF24	All	-	I/O, L102N_YY	I/O, L102N_YY
I/O, L102P_YY	4	AF25	All	-	I/O, L102P_YY	I/O, L102P_YY

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L64N_YY	2	J25	All	-	I/O, L64N_YY	I/O, L64N_YY
I/O (D2), L64P_YY	2	J24	All	-	I/O (D2), L64P_YY	I/O (D2), L64P_YY
I/O (D1)	2	J23	-	-	I/O (D1)	I/O (D1)
I/O, VREF Bank 2, L63N_YY	2	J22	All	All	I/O, VREF Bank 2, L63N_YY	I/O, VREF Bank 2, L63N_YY
I/O, L63P_YY	2	J21	All	-	I/O, L63P_YY	I/O, L63P_YY
I/O, L62N_YY	2	J20	All	-	I/O, L62N_YY	I/O, L62N_YY
I/O, L62P_YY	2	J19	All	-	I/O, L62P_YY	I/O, L62P_YY
I/O	2	H22	-	-	I/O	I/O
I/O, L61N	2	H26	XC2S600E	-	I/O	I/O, L61N_Y
I/O, L61P	2	H25	XC2S600E	XC2S600E	-	I/O, VREF Bank 2, L61P_Y
I/O, L60N	2	H21	XC2S400E	-	I/O, L60N_Y	I/O, L60N
I/O, L60P	2	H20	XC2S400E	-	I/O, L60P_Y	I/O, L60P
I/O	2	G26	-	-	-	I/O
I/O, L59N_YY	2	G25	All	-	I/O, L59N_YY	I/O, L59N_YY
I/O, L59P_YY	2	G24	All	-	I/O, L59P_YY	I/O, L59P_YY
I/O	2	G23	-	-	I/O	I/O
I/O, L58N_YY	2	G22	All	-	I/O, L58N_YY	I/O, L58N_YY
I/O, VREF Bank 2, L58P_YY	2	G21	All	All	I/O, VREF Bank 2, L58P_YY	I/O, VREF Bank 2, L58P_YY
I/O	2	G20	-	-	I/O	I/O
I/O, L57N_YY	2	F26	All	-	I/O, L57N_YY	I/O, L57N_YY
I/O, L57P_YY	2	F25	All	-	I/O, L57P_YY	I/O, L57P_YY
I/O, L56N	2	F24	XC2S600E	-	I/O, L56N	I/O, L56N_Y
I/O, L56P	2	F23	XC2S600E	-	I/O, L56P	I/O, L56P_Y
I/O	2	F22	-	-	-	I/O
I/O, L55N	2	E26	XC2S600E	-	I/O, L55N	I/O, L55N_Y
I/O, VREF Bank 2, L55P	2	E25	XC2S600E	All	I/O, VREF Bank 2, L55P	I/O, VREF Bank 2, L55P_Y
I/O, L54N	2	E23	XC2S400E	-	I/O, L54N_Y	I/O, L54N
I/O, L54P	2	E22	XC2S400E	-	I/O, L54P_Y	I/O, L54P
I/O, L53N_YY	2	F21	All	-	I/O, L53N_YY	I/O, L53N_YY
I/O, L53P_YY	2	E21	All	-	I/O, L53P_YY	I/O, L53P_YY
I/O, L52N	2	D26	XC2S600E	-	I/O	I/O, L52N_Y
I/O, L52P	2	D25	XC2S600E	-	-	I/O, L52P_Y