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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1176
Number of Logic Elements/Cells	5292
Total RAM Bits	57344
Number of I/O	146
Number of Gates	200000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s200e-6pq208c

Spartan-IIE FPGA Family: Introduction and Ordering Information

DS077-1 (v3.0) August 9, 2013

Product Specification

Introduction

The Spartan®-IIE Field-Programmable Gate Array family gives users high performance, abundant logic resources, and a rich feature set, all at an exceptionally low price. The seven-member family offers densities ranging from 50,000 to 600,000 system gates, as shown in Table 1. System performance is supported beyond 200 MHz.

Features include block RAM (to 288K bits), distributed RAM (to 221,184 bits), 19 selectable I/O standards, and four DLLs (Delay-Locked Loops). Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

The Spartan-IIE family is a superior alternative to mask-programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary (impossible with ASICs).

Features

- Second generation ASIC replacement technology
  - Densities as high as 15,552 logic cells with up to 600,000 system gates
  - Streamlined features based on Virtex®-E FPGA architecture
  - Unlimited in-system reprogrammability
  - Very low cost
  - Cost-effective 0.15 micron technology
- System level features
  - SelectRAM™ hierarchical memory:
    - 16 bits/LUT distributed RAM
    - Configurable 4K-bit true dual-port block RAM
    - Fast interfaces to external RAM
  - Fully 3.3V PCI compliant to 64 bits at 66 MHz and CardBus compliant
  - Low-power segmented routing architecture
  - Dedicated carry logic for high-speed arithmetic
  - Efficient multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with enable, set, reset
  - Four dedicated DLLs for advanced clock control
    - Eliminate clock distribution delay
    - Multiply, divide, or phase shift
  - Four primary low-skew global clock distribution nets
  - IEEE 1149.1 compatible boundary scan logic
- Versatile I/O and packaging
  - Pb-free package options
  - Low-cost packages available in all densities
  - Family footprint compatibility in common packages
  - 19 high-performance interface standards
    - LVTTL, LVCMOS, HSTL, SSTL, AGP, CTT, GTL
    - LVDS and LVPECL differential I/O
  - Up to 205 differential I/O pairs that can be input, output, or bidirectional
  - Hot swap I/O (CompactPCI friendly)
- Core logic powered at 1.8V and I/Os powered at 1.5V, 2.5V, or 3.3V
- Fully supported by powerful Xilinx® ISE® development system
  - Fully automatic mapping, placement, and routing
  - Integrated with design entry and verification tools
  - Extensive IP library including DSP functions and soft processors

Table 1: **Spartan-IIE FPGA Family Members**

Device	Logic Cells	Typical System Gate Range (Logic and RAM)	CLB Array (R x C)	Total CLBs	Maximum Available User I/O(1)	Maximum Differential I/O Pairs	Distributed RAM Bits	Block RAM Bits
XC2S50E	1,728	23,000 - 50,000	16 x 24	384	182	83	24,576	32K
XC2S100E	2,700	37,000 - 100,000	20 x 30	600	202	86	38,400	40K
XC2S150E	3,888	52,000 - 150,000	24 x 36	864	265	114	55,296	48K
XC2S200E	5,292	71,000 - 200,000	28 x 42	1,176	289	120	75,264	56K
XC2S300E	6,912	93,000 - 300,000	32 x 48	1,536	329	120	98,304	64K
XC2S400E	10,800	145,000 - 400,000	40 x 60	2,400	410	172	153,600	160K
XC2S600E	15,552	210,000 - 600,000	48 x 72	3,456	514	205	221,184	288K

Notes:
1. User I/O counts include the four global clock/user input pins. See details in Table 2, page 5

Spartan-IIE FPGA Family: Functional Description

DS077-2 (v3.0) August 9, 2013 **Product Specification**

Architectural Description

Spartan-IIE FPGA Array

The Spartan®-IIE user-programmable gate array, shown in Figure 3, is composed of five major configurable elements:

- IOBs provide the interface between the package pins and the internal logic
- CLBs provide the functional elements for constructing most logic
- Dedicated block RAM memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- Versatile multi-level interconnect structure

As can be seen in Figure 3, the CLBs form the central logic structure with easy access to all support and routing structures. The IOBs are located around all the logic and memory elements for easy and quick routing of signals on and off the chip.

Values stored in static memory cells control all the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

Each of these elements will be discussed in detail in the following sections.

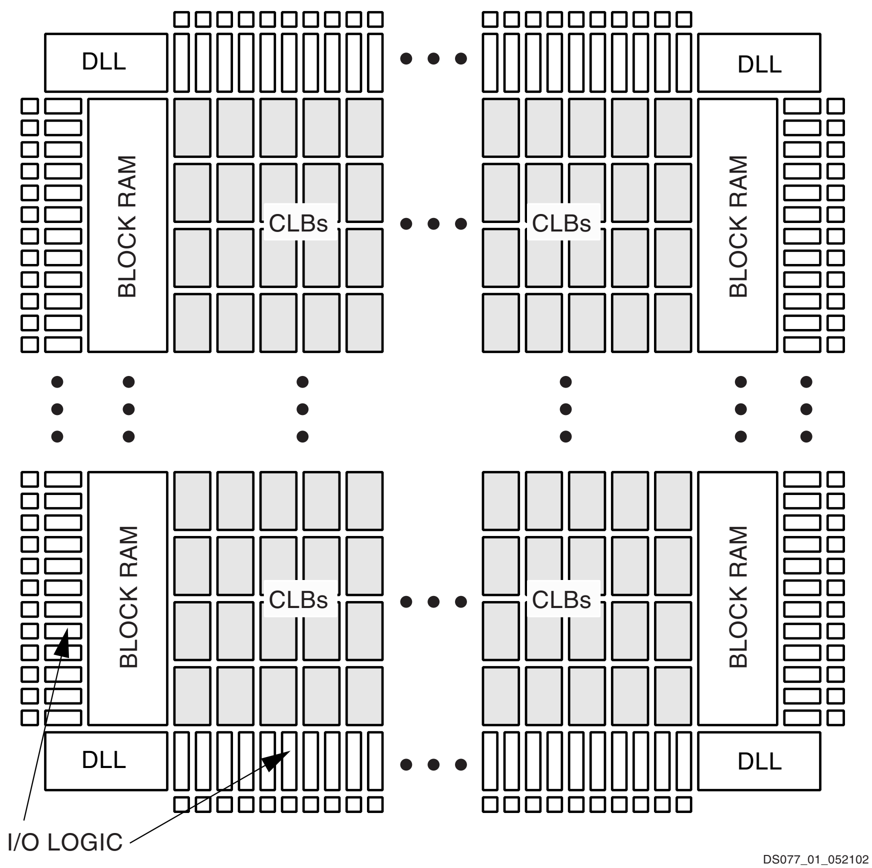

Figure 3: **Basic Spartan-IIE Family FPGA Block Diagram**

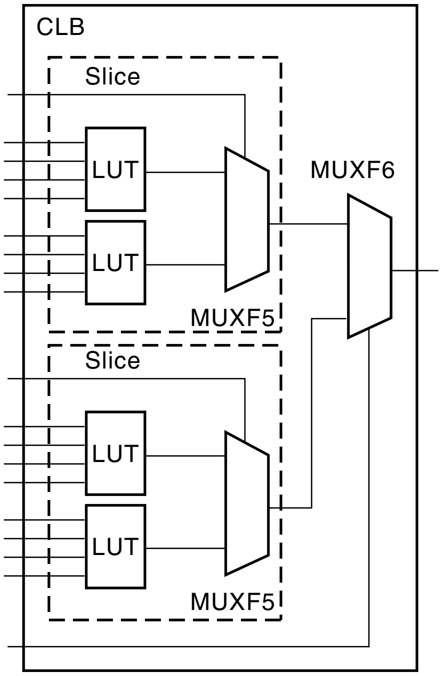

Figure 7: **F5 and F6 Multiplexers**

Each CLB has four direct feedthrough paths, one per LC. These paths provide extra data input lines or additional local routing that does not consume logic resources.

Arithmetic Logic

Dedicated carry logic provides capability for high-speed arithmetic functions. The Spartan-IIE FPGA CLB supports two separate carry chains, one per slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 1-bit full adder to be implemented within an LC. In addition, a dedicated AND gate improves the efficiency of multiplier implementations.

The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

BUFTs

Each Spartan-IIE FPGA CLB contains two 3-state drivers (BUFTs) that can drive on-chip busses. The IOBs on the left and right sides can also drive the on-chip busses. See Dedicated Routing, page 17. Each Spartan-IIE FPGA BUFT has an independent 3-state control pin and an independent input pin. The 3-state control pin is an active-Low enable (T). When all BUFTs on a net are disabled, the net is High. There is no need to instantiate a pull-up unless desired for simulation purposes. Simultaneously driving BUFTs onto the same net will not cause contention. If driven both High and Low, the net will be Low.

Block RAM

Spartan-IIE FPGAs incorporate several large block RAM memories. These complement the distributed RAM Look-Up Tables (LUTs) that provide shallow memory structures implemented in CLBs.

Block RAM memory blocks are organized in columns. Most Spartan-IIE devices contain two such columns, one along each vertical edge. The XC2S400E has four block RAM columns and the XC2S600E has six block RAM columns. These columns extend the full height of the chip. Each memory block is four CLBs high, and consequently, a Spartan-IIE device 16 CLBs high will contain four memory blocks per column, and a total of eight blocks.

Table 6: **Spartan-IIE Block RAM Amounts**

Spartan-IIE Device	# of Blocks	Total Block RAM Bits
XC2S50E	8	32K
XC2S100E	10	40K
XC2S150E	12	48K
XC2S200E	14	56K
XC2S300E	16	64K
XC2S400E	40	160K
XC2S600E	72	288K

Each block RAM cell, as illustrated in Figure 8, is a fully synchronous dual-ported 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

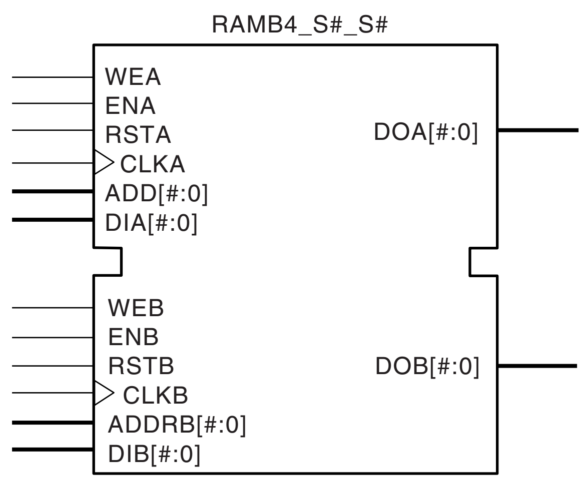

Figure 8: **Dual-Port Block RAM**

Table 7 shows the depth and width aspect ratios for the block RAM.

Table 7: **Block RAM Port Aspect Ratios**

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

The Spartan-IIE FPGA block RAM also includes dedicated routing to provide an efficient interface with both CLBs and other block RAMs. See Xilinx Application Note XAPP173 for more information on block RAM.

Programmable Routing

It is the longest delay path that limits the speed of any design. Consequently, the Spartan-IIE FPGA routing architecture and its place-and-route software were defined jointly to minimize long-path delays and yield the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

The software automatically uses the best available routing based on user timing requirements. The details are provided here for reference.

Local Routing

The local routing resources, as shown in Figure 9, provide the following three types of connections:

- Interconnections among the LUTs, flip-flops, and General Routing Matrix (GRM), described below.
- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM

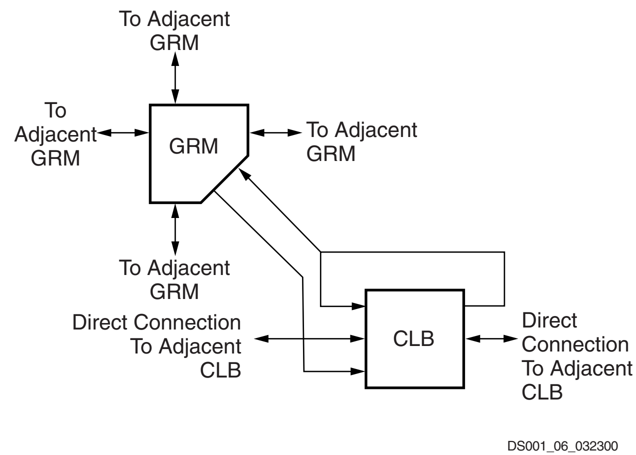

Figure 9: **Spartan-IIE Local Routing**

General Purpose Routing

Most Spartan-IIE FPGA signals are routed on the general purpose routing, and consequently, the majority of interconnect resources are associated with this level of the routing hierarchy. The general routing resources are located in horizontal and vertical routing channels associated with the rows and columns of CLBs. The general-purpose routing resources are listed below.

- Adjacent to each CLB is a General Routing Matrix (GRM). The GRM is the switch matrix through which horizontal and vertical routing resources connect, and is also the means by which the CLB gains access to the general purpose routing.
- 24 single-length lines route GRM signals to adjacent GRMs in each of the four directions.
- 96 buffered Hex lines route GRM signals to other GRMs six blocks away in each one of the four directions. Organized in a staggered pattern, Hex lines may be driven only at their endpoints. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source). One third of the Hex lines are bidirectional, while the remaining ones are unidirectional.
- 12 Longlines are buffered, bidirectional wires that distribute signals across the device quickly and efficiently. Vertical Longlines span the full height of the device, and horizontal ones span the full width of the device.

I/O Routing

Spartan-IIE devices have additional routing resources around their periphery that form an interface between the CLB array and the IOBs. This additional routing, called the VersaRing™ routing, facilitates pin-swapping and pin-locking, such that logic redesigns can adapt to existing PCB layouts. Time-to-market is reduced, since PCBs and other system components can be manufactured while the logic design is still in progress.

design, thus allowing the most convenient entry method to be used for each portion of the design.

Design Implementation

The place-and-route tools automatically provide the implementation flow described in this section. The partitioner takes the EDIF netlist for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floorplanning.

The implementation software incorporates timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines then recognize these user-specified requirements and accommodate them.

Timing requirements are entered in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the netlist for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the static timing analyzer.

For in-circuit debugging, Xilinx offers a download cable, which connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can read back the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

Configuration

Configuration is the process by which the bitstream of a design, as generated by the Xilinx development software, is loaded into the internal configuration memory of the FPGA. Spartan-IIE devices support both serial configuration, using the master/slave serial and JTAG modes, as well as byte-wide configuration employing the Slave Parallel mode.

Configuration File

Spartan-IIE devices are configured by sequentially loading frames of data that have been concatenated into a configuration file. Table 10 shows how much nonvolatile storage space is needed for Spartan-IIE devices.

It is important to note that, while a PROM is commonly used to store configuration data before loading them into the FPGA, it is by no means required. Any of a number of different kinds of under populated nonvolatile storage already available either on or off the board (for example, hard drives, FLASH cards, and so on) can be used.

Table 10: **Spartan-IIE Configuration File Size**

Device	Configuration File Size (Bits)
XC2S50E	630,048
XC2S100E	863,840
XC2S150E	1,134,496
XC2S200E	1,442,016
XC2S300E	1,875,648
XC2S400E	2,693,440
XC2S600E	3,961,632

Modes

Spartan-IIE devices support the following four configuration modes:

- Slave Serial mode
- Master Serial mode
- Slave Parallel mode
- Boundary-scan mode

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to the end of configuration. The selection codes are listed in Table 11.

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected.

Revision History

Date	Version	Description
11/15/2001	1.0	Initial Xilinx release.
11/18/2002	2.0	Added XC2S400E and XC2S600E. Removed Preliminary designation. Clarified details of I/O standards, boundary scan, and configuration.
07/09/2003	2.1	Added hot swap description (see Hot Swap, Hot Insertion, Hot Socketing Support). Added Table 9 containing JTAG IDCODE values. Clarified configuration PROM support.
06/18/2008	2.3	Added note that TDI, TMS, and TCK have a default pull-up resistor. Add note on maximum daisy-chain limit. Updated Figure 19 since Mode pins can be pulled up to either 2.5V or 3.3V. Updated all modules for continuous page, figure, and table numbering. Updated links. Synchronized all modules to v2.3.
08/09/2013	3.0	This product is obsolete/discontinued per XCN12026.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL I	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	8	–8
HSTL III	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	24	–8
HSTL IV	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	48	–8
SSTL3 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	–8
SSTL3 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	–16
SSTL2 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.61	V_{REF} + 0.61	7.6	–7.6
SSTL2 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	15.2	–15.2
CTT	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.4	V_{REF} + 0.4	8	–8
AGP	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	Note (2)	Note (2)

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested.
2. Tested according to the relevant specifications.

LVDS DC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		2.375	2.5	2.625	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	1.25	1.425	1.6	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	0.9	1.075	1.25	V
V_{ODIFF}	Differential output voltage (Q – $\overline{Q}$), Q = High or ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	250	350	450	mV
V_{OCM}	Output common-mode voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.125	1.25	1.375	V
V_{IDIFF}	Differential input voltage (Q – $\overline{Q}$), Q = High or ($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25 V	100	350	-	mV
V_{ICM}	Input common-mode voltage	Differential input voltage = ±350 mV	0.2	1.25	2.2	V

LVPECL DC Specifications

These values are valid at the output of the source termination pack shown under LVPECL, with a 100Ω differential load only. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. The following table summarizes the DC output specifications of LVPECL.

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential input voltage	0.3	-	0.3	-	0.3	-	V

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in IOB Output Delay Adjustments for Different Standards(1), page 40.

Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Propagation Delays						
T_{IOOP}	O input to pad	1.0	2.7	1.0	2.9	ns
T_{IOOLP}	O input to pad via transparent latch	1.2	3.1	1.2	3.4	ns
3-state Delays						
T_{IOTHZ}	T input to pad high impedance(1)	0.7	1.7	0.7	1.9	ns
T_{IOTON}	T input to valid data on pad	1.1	2.9	1.1	3.1	ns
$T_{IOTLPHZ}$	T input to pad high impedance via transparent latch(1)	0.8	2.0	0.8	2.2	ns
$T_{IOTLPON}$	T input to valid data on pad via transparent latch	1.2	3.2	1.2	3.4	ns
T_{GTS}	GTS to pad high impedance(1)	1.9	4.6	1.9	4.9	ns
Sequential Delays						
T_{IOCKP}	Clock CLK to pad	0.9	2.8	0.9	2.9	ns
T_{IOCKHZ}	Clock CLK to pad high impedance (synchronous)(1)	0.7	2.0	0.7	2.2	ns
T_{IOCKON}	Clock CLK to valid data on pad (synchronous)	1.1	3.2	1.1	3.4	ns
Setup/Hold Times with Respect to Clock CLK						
T_{IOOCK} / T_{IOCKO}	O input	1.0 / 0	-	1.1 / 0	-	ns
$T_{IOOCECK}$ / $T_{IOCKOCE}$	OCE input	0.7 / 0	-	0.7 / 0	-	ns
$T_{IOSRCKO}$ / $T_{IOCKOSR}$	SR input (OFF)	0.9 / 0	-	1.0 / 0	-	ns
T_{IOTCK} / T_{IOCKT}	3-state setup times, T input	0.6 / 0	-	0.7 / 0	-	ns
$T_{IOTCECK}$ / $T_{IOCKTCE}$	3-state setup times, TCE input	0.6 / 0	-	0.8 / 0	-	ns
$T_{IOSRCKT}$ / $T_{IOCKTSR}$	3-state setup times, SR input (TFF)	0.9 / 0	-	1.0 / 0	-	ns
Set/Reset Delays						
T_{IOSRP}	SR input to pad (asynchronous)	1.2	3.3	1.2	3.5	ns
T_{IOSRHZ}	SR input to pad high impedance (asynchronous)(1)	1.0	2.4	1.0	2.7	ns
T_{IOSRON}	SR input to valid data on pad (asynchronous)	1.4	3.7	1.4	3.9	ns
T_{IOGSRQ}	GSR to pad	3.8	8.5	3.8	9.7	ns

Notes:
1. Three-state turn-off delays should not be adjusted.

IOB Output Delay Adjustments for Different Standards(1)

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade		Units
			-7	-6	
Output Delay Adjustments (Adj)					
T_{OLVTTL_S2}	Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, C_{SL})	LVTTL, Slow, 2 mA	14.7	14.7	ns
T_{OLVTTL_S4}		4 mA	7.5	7.5	ns
T_{OLVTTL_S6}		6 mA	4.8	4.8	ns
T_{OLVTTL_S8}		8 mA	3.0	3.0	ns
T_{OLVTTL_S12}		12 mA	1.9	1.9	ns
T_{OLVTTL_S16}		16 mA	1.7	1.7	ns
T_{OLVTTL_S24}		24 mA	1.3	1.3	ns
T_{OLVTTL_F2}		LVTTL, Fast, 2 mA	13.1	13.1	ns
T_{OLVTTL_F4}		4 mA	5.3	5.3	ns
T_{OLVTTL_F6}		6 mA	3.1	3.1	ns
T_{OLVTTL_F8}		8 mA	1.0	1.0	ns
T_{OLVTTL_F12}		12 mA	0	0	ns
T_{OLVTTL_F16}		16 mA	–0.05	–0.05	ns
T_{OLVTTL_F24}		24 mA	–0.20	–0.20	ns
$T_{OLVCMOS2}$		LVCMOS2	0.09	0.09	ns
$T_{OLVCMOS18}$		LVCMOS18	0.7	0.7	ns
T_{OLVDS}		LVDS	–1.2	–1.2	ns
$T_{OLVPECL}$		LVPECL	–0.41	–0.41	ns
T_{OPCI33_3}		PCI, 33 MHz, 3.3V	2.3	2.3	ns
T_{OPCI66_3}		PCI, 66 MHz, 3.3V	–0.41	–0.41	ns
T_{OGTL}		GTL	0.49	0.49	ns
T_{OGTLP}		GTL+	0.8	0.8	ns
T_{OHSTL_I}		HSTL I	–0.51	–0.51	ns
T_{OHSTL_III}		HSTL III	–0.91	–0.91	ns
T_{OHSTL_IV}		HSTL IV	–1.01	–1.01	ns
T_{OSSTL2_I}		SSTL2 I	–0.51	–0.51	ns
T_{OSSLT2_II}		SSTL2 II	–0.91	–0.91	ns
T_{OSSTL3_I}		SSTL3 I	–0.51	–0.51	ns
T_{OSSTL3_II}		SSTL3 II	–1.01	–1.01	ns
T_{OCTT}		CTT	–0.61	–0.61	ns
T_{OAGP}		AGP	–0.91	–0.91	ns

Notes:

1. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see the tables Constants for Calculating T_{IOOP} and Delay Measurement Methodology, page 41.

Revision History

Date	Version	Description
11/15/2001	1.0	Initial Xilinx release.
06/28/2002	1.1	Added -7 speed grade and extended DLL specs to Industrial.
11/18/2002	2.0	Added XC2S400E and XC2S600E. Added minimum specifications. Added reference to XAPP450 for Power-On Requirements. Removed Preliminary designation.
07/09/2003	2.1	Added I_{CCINTQ} typical values. Reduced ICCPO power-on current requirements. Relaxed TCCPO power-on ramp requirements. Added IHSPO to describe current in hot-swap applications. Updated TPSFD / TPHFD description to indicate use of delay element.
06/18/2008	2.3	Updated I/O measurement thresholds. Updated all modules for continuous page, figure, and table numbering. Updated links. Synchronized all modules to v2.3.
08/09/2013	3.0	This product is obsolete/discontinued per XCN12026.

Low Voltage Differential Signals (LVDS and LVPECL)

The Spartan-IIE family features low-voltage differential signaling (LVDS and LVPECL). Each signal utilizes two pins on the Spartan-IIE device, known as differential pin pairs. Each differential pin pair has a Positive (P) and a Negative (N) pin. These pairs are labeled in the following manner.

I/O, L#[P/N][-/_Y/_YY]

where

L = LVDS or LVPECL pin

= Pin pair number

P = Positive

N = Negative

_Y = Asynchronous output allowed (device-dependent)

_YY = Asynchronous output allowed (all devices)

Available Differential Pairs According to Package Type

Device	TQ144	PQ208	FT256	FG456	FG676
XC2S50E	28	50	83	-	-
XC2S100E	28	50	83	86	-
XC2S150E	-	50	83	114	-
XC2S200E	-	50	83	120	-
XC2S300E	-	50	83	120	-
XC2S400E	-	-	83	120	172
XC2S600E	-	-	-	120	205

Synchronous or Asynchronous

I/O pins for differential signals can either be synchronous or asynchronous, input or output. Differential signaling requires the pins of each pair to switch simultaneously. If the output signals driving the pins are from IOB flip-flops, they are synchronous. If the signals driving the pins are from internal logic, they are asynchronous, and therefore more care must be taken that they are simultaneous. Any differential pairs can be used for synchronous input and output signals as well as asynchronous input signals.

However, only the differential pairs with the _Y or _YY suffix can be used for asynchronous output signals.

Asynchronous Output Pad Name Designation

Because of differences between densities, the differential pairs that can be used for asynchronous outputs vary by device. The pairs that are available in all densities for a given package have the _YY suffix. These pins should be used for differential asynchronous outputs if the design may later move to a different density. All other differential pairs that can be used for asynchronous outputs have the _Y suffix.

To simplify the following tables, the "Pad Name" column shows the part of the name that is common across densities. The "Pad Name" column leaves out the _Y suffix and the "LVDS Asynchronous Output Option" column indicates the densities that allow asynchronous outputs for LVDS or LVPECL on the given pin.

DLL Pins

Pins labeled "I/O (DLL)" can be used as general-purpose I/O or as inputs to the DLL. Adjacent DLL pins form a differential pair. They reside in two different banks, so if they are outputs the V_{CCO} level must be the same for both banks. Each DLL pin can also be paired with the adjacent GCK clock pin for a differential clock input. The "I/O (DLL)" pin always becomes the N terminal when paired with GCK, even if it is labeled "P" for its pairing with the adjacent DLL pin.

VREF Pins

Pins labeled "I/O, VREF" can be used as either an I/O or a VREF pin. If any I/O pin within the bank requires a VREF input, all the VREF pins in the bank must be connected to the same voltage. See the I/O banking rules in the Functional Description module for more detail. If no pin in a given bank requires VREF, then that bank's VREF pins can be used as general I/O.

To simplify the following tables, the "Pad Name" column shows the part of the name that is common across densities. When VREF is only available in limited densities, the "Pad Name" column leaves out the VREF designation and the "VREF Option" column indicates the densities that provide VREF on the given pin.

VCCO Banks

In the TQ144 and PQ208 packages, the eight banks have VCCO connected together. Thus, only one VCCO is allowed in these packages, although different VREF values are allowed in each of the eight banks. See I/O Banking.

TQ144 Pinouts (XC2S50E and XC2S100E) *(Continued)*

Pad Name			LVDS Async. Output Option	V_{REF} Option
Function	Bank	Pin		
I/O (DLL), L17P	4	P56	-	-
I/O	4	P57	-	-
I/O, VREF Bank 4	4	P58	-	All
I/O, L16N_YY	4	P59	All	-
I/O, L16P_YY	4	P60	All	-
VCCINT	-	P61	-	-
GND	-	P62	-	-
I/O, L15N_YY	4	P63	All	-
I/O, L15P_YY	4	P64	All	XC2S100E
I/O	4	P65	-	-
I/O, VREF Bank 4	4	P66	-	All
I/O	4	P67	-	-
I/O, L14N_YY	4	P68	All	-
I/O, L14P_YY	4	P69	All	-
GND	-	P70	-	-
DONE	3	P71	-	-
VCCO	-	P72	-	-
PROGRAM	-	P73	-	-
I/O (INIT), L13N_YY	3	P74	All	-
I/O (D7), L13P_YY	3	P75	All	-
I/O	3	P76	-	-
I/O, VREF Bank 3	3	P77	-	All
I/O	3	P78	-	-
I/O, L12N	3	P79	XC2S50E	XC2S100E
I/O (D6), L12P	3	P80	XC2S50E	-
GND	-	P81	-	-
I/O (D5), L11N_YY	3	P82	All	-
I/O, L11P_YY	3	P83	All	-
I/O	3	P84	-	-

TQ144 Pinouts (XC2S50E and XC2S100E) *(Continued)*

Pad Name			LVDS Async. Output Option	V_{REF} Option
Function	Bank	Pin		
I/O, VREF Bank 3, L10N	3	P85	XC2S50E	All
I/O (D4), L10P	3	P86	XC2S50E	-
I/O	3	P87	-	-
VCCINT	-	P88	-	-
I/O (TRDY)	3	P89	-	-
VCCO	-	P90	-	-
GND	-	P91	-	-
I/O (IRDY)	2	P92	-	-
I/O	2	P93	-	-
I/O (D3), L9N	2	P94	XC2S50E	-
I/O, VREF Bank 2, L9P	2	P95	XC2S50E	All
I/O	2	P96	-	-
I/O, L8N_YY	2	P97	All	-
I/O (D2), L8P_YY	2	P98	All	-
GND	-	P99	-	-
I/O (D1), L7N	2	P100	XC2S50E	-
I/O, L7P	2	P101	XC2S50E	XC2S100E
I/O	2	P102	-	-
I/O, VREF Bank 2	2	P103	-	All
I/O	2	P104	-	-
I/O (DIN, D0), L6N_YY	2	P105	All	-
I/O (DOUT, BUSY), L6P_YY	2	P106	All	-
CCLK	2	P107	-	-
VCCO	-	P108	-	-
TDO	2	P109	-	-
GND	-	P110	-	-
TDI	-	P111	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O	2	P134	-	-
I/O (D3), L17N	2	P135	XC2S50E, 300E	-
I/O, VREF Bank 2, L17P	2	P136	XC2S50E, 300E	All
GND	-	P137	-	-
I/O, L16N_YY	2	P138	All	-
I/O, L16P_YY	2	P139	All	-
I/O, L15N_YY	2	P140	All	-
I/O (D2), L15P_YY	2	P141	All	-
VCCINT	-	P142	-	-
VCCO	-	P143	-	-
GND	-	P144	-	-
I/O (D1), L14N	2	P145	XC2S50E, 300E	-
I/O, L14P	2	P146	XC2S50E, 300E	XC2S100E, 150E, 200E, 300E
I/O	2	P147	-	-
I/O	2	P148	-	-
I/O	2	P149	-	-
I/O, VREF Bank 2, L13N	2	P150	XC2S100E, 150E	All
I/O, L13P	2	P151	XC2S100E, 150E	-
I/O	2	P152	-	XC2S200E, 300E
I/O (DIN, D0), L12N_YY	2	P153	All	-
I/O (DOUT, BUSY), L12P_YY	2	P154	All	-
CCLK	2	P155	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
VCCO	-	P156	-	-
TDO	2	P157	-	-
GND	-	P158	-	-
TDI	-	P159	-	-
I/O ($\overline{CS}$), L11P_YY	1	P160	All	-
I/O ($\overline{WRITE}$), L11N_YY	1	P161	All	-
I/O	1	P162	-	XC2S200E, 300E
I/O	1	P163	-	-
I/O, VREF Bank 1, L10P_YY	1	P164	All	All
I/O, L10N_YY	1	P165	All	-
I/O	1	P166	-	-
I/O	1	P167	-	-
I/O, L9P	1	P168	XC2S50E, 100E, 200E, 300E	XC2S100E, 150E, 200E, 300E
I/O, L9N	1	P169	XC2S50E, 100E, 200E, 300E	-
GND	-	P170	-	-
VCCO	-	P171	-	-
VCCINT	-	P172	-	-
I/O, L8P	1	P173	XC2S50E, 100E, 200E, 300E	-
I/O, L8N	1	P174	XC2S50E, 100E, 200E, 300E	-
I/O, L7P	1	P175	XC2S50E, 200E, 300E	-
I/O, L7N	1	P176	XC2S50E, 200E, 300E	-
GND	-	P177	-	-

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
TMS	-	E4	-	-	TMS	TMS	TMS	TMS	TMS	TMS
I/O	7	D3	XC2S150E	-	I/O	I/O, L113P_Y	I/O	I/O	I/O	I/O
I/O	7	C2	-	-	-	-	-	I/O	I/O	I/O
I/O	7	C1	XC2S150E	-	-	I/O, L113N_Y	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	D2	XC2S150E, 200E, 300E, 400E	-	-	I/O, L112P_Y	I/O, L119P_Y	I/O, L119P_Y	I/O, L119P_Y	I/O, L119P
I/O, L#N_Y	7	D1	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L112N_Y	I/O, L119N_Y	I/O, L119N_Y	I/O, L119N_Y	I/O, L119N
I/O, L#P_Y	7	E2	XC2S100E, 200E, 300E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L85P_Y	I/O, L111P	I/O, VREF Bank 7, L118P_Y	I/O, VREF Bank 7, L118P_Y	I/O, VREF Bank 7, L118P	I/O, VREF Bank 7, L118P_Y
I/O, L#N_Y	7	E3	XC2S100E, 200E, 300E, 600E	-	I/O, L85N_Y	I/O, L111N	I/O, L118N_Y	I/O, L118N_Y	I/O, L118N	I/O, L118N_Y
I/O	7	E1	-	-	-	-	-	I/O	I/O	I/O
I/O	7	F5	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	F4	XC2S100E, 200E, 300E, 600E	-	I/O, L84P_Y	I/O, L110P	I/O, L117P_Y	I/O, L117P_Y	I/O, L117P	I/O, L117P_Y
I/O, L#N_Y	7	F3	XC2S100E, 200E, 300E, 600E	-	I/O, L84N_Y	I/O, L110N	I/O, L117N_Y	I/O, L117N_Y	I/O, L117N	I/O, L117N_Y
I/O, VREF Bank 7, L#P_Y	7	F2	XC2S150E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 7, L83P	I/O, VREF Bank 7, L109P_Y	I/O, VREF Bank 7, L116P_Y	I/O, VREF Bank 7, L116P_Y	I/O, VREF Bank 7, L116P_Y	I/O, VREF Bank 7, L116P_Y
I/O, L#N_Y	7	F1	XC2S150E, 200E, 300E, 400E, 600E	-	I/O, L83N	I/O, L109N_Y	I/O, L116N_Y	I/O, L116N_Y	I/O, L116N_Y	I/O, L116N_Y
I/O	7	G5	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	G4	XC2S150E, 200E, 300E, 400E	-	-	I/O, L108P_Y	I/O, L115P_Y	I/O, L115P_Y	I/O, L115P_Y	I/O, L115P
I/O, L#N_Y	7	G3	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L108N_Y	I/O, L115N_Y	I/O, L115N_Y	I/O, L115N_Y	I/O, L115N
I/O, L#P_Y	7	G2	XC2S100E, 150E, 300E, 600E	XC2S600E	I/O, L82P_Y	I/O, L107P_Y	I/O, L114P	I/O, L114P_Y	I/O, L114P	I/O, VREF Bank 7, L114P_Y
I/O, L#N_Y	7	G1	XC2S100E, 150E, 300E, 600E	-	I/O, L82N_Y	I/O, L107N_Y	I/O, L114N	I/O, L114N_Y	I/O, L114N	I/O, L114N_Y

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O (WRITE), L#N_YY	1	A20	All	-	I/O (WRITE), L20N_YY	I/O (WRITE), L26N_YY	I/O (WRITE), L28N_YY	I/O (WRITE), L28N_YY	I/O (WRITE), L28N_YY	I/O (WRITE), L28N_YY
I/O	1	D18	-	-	-	-	-	I/O	I/O	I/O
I/O	1	C18	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P	1	B19	XC2S200E, 300E, 400E, 600E	-	-	I/O, L25P	I/O, L27P_Y	I/O, L27P_Y	I/O, L27P_Y	I/O, L27P_Y
I/O, L#N	1	A19	XC2S200E, 300E, 400E, 600E	-	I/O	I/O, L25N	I/O, L27N_Y	I/O, L27N_Y	I/O, L27N_Y	I/O, L27N_Y
I/O, L#P	1	B18	XC2S100E, 200E, 300E, 400E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L19P_Y	I/O, L24P	I/O, VREF Bank 1, L26P_Y	I/O, VREF Bank 1, L26P_Y	I/O, VREF Bank 1, L26P_Y	I/O, VREF Bank 1, L26P_Y
I/O, L#N	1	A18	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L19N_Y	I/O, L24N	I/O, L26N_Y	I/O, L26N_Y	I/O, L26N_Y	I/O, L26N_Y
I/O	1	D17	-	-	-	-	-	I/O	I/O	I/O
I/O	1	C17	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P_YY	1	B17	All	-	I/O, L18P_YY	I/O, L23P_YY	I/O, L25P_YY	I/O, L25P_YY	I/O, L25P_YY	I/O, L25P_YY
I/O, L#N_YY	1	A17	All	-	I/O, L18N_YY	I/O, L23N_YY	I/O, L25N_YY	I/O, L25N_YY	I/O, L25N_YY	I/O, L25N_YY
I/O, VREF Bank 1, L#P_YY	1	E16	All	All	I/O, VREF Bank 1, L17P_YY	I/O, VREF Bank 1, L22P_YY	I/O, VREF Bank 1, L24P_YY	I/O, VREF Bank 1, L24P_YY	I/O, VREF Bank 1, L24P_YY	I/O, VREF Bank 1, L24P_YY
I/O, L#N_YY	1	E17	All	-	I/O, L17N_YY	I/O, L22N_YY	I/O, L24N_YY	I/O, L24N_YY	I/O, L24N_YY	I/O, L24N_YY
I/O	1	E15	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P	1	D16	XC2S300E, 600E	-	-	I/O, L21P	I/O, L23P	I/O, L23P_Y	I/O, L23P	I/O, L23P_Y
I/O, L#N	1	C16	XC2S300E, 600E	-	I/O	I/O, L21N	I/O, L23N	I/O, L23N_Y	I/O, L23N	I/O, L23N_Y
I/O, L#P	1	B16	XC2S100E, 300E, 600E	XC2S600E	I/O, L16P_Y	I/O, L20P	I/O, L22P	I/O, L22P_Y	I/O, L22P	I/O, VREF Bank 1, L22P_Y
I/O, L#N	1	A16	XC2S100E, 300E, 600E	-	I/O, L16N_Y	I/O, L20N	I/O, L22N	I/O, L22N_Y	I/O, L22N	I/O, L22N_Y
I/O	1	F14	-	-	-	-	-	I/O	I/O	I/O
I/O, VREF Bank 1, L#P	1	D15	XC2S100E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 1, L15P_Y	I/O, VREF Bank 1, L19P	I/O, VREF Bank 1, L21P_Y	I/O, VREF Bank 1, L21P_Y	I/O, VREF Bank 1, L21P_Y	I/O, VREF Bank 1, L21P_Y
I/O, L#N	1	C15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L15N_Y	I/O, L19N	I/O, L21N_Y	I/O, L21N_Y	I/O, L21N_Y	I/O, L21N_Y
I/O, L#P	1	B15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L14P_Y	I/O, L18P	I/O, L20P_Y	I/O, L20P_Y	I/O, L20P_Y	I/O, L20P_Y

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L188P	7	L8	XC2S400E	-	I/O, L188P_Y	I/O, L188P
I/O, L188N	7	L7	XC2S400E	-	I/O, L188N_Y	I/O, L188N
I/O, L187P	7	L6	XC2S600E	-	I/O, L187P	I/O, L187P_Y
I/O, L187N	7	L5	XC2S600E	-	I/O, L187N	I/O, L187N_Y
I/O	7	L3	-	-	-	I/O
I/O, L186P	7	L2	XC2S600E	-	I/O, L186P	I/O, L186P_Y
I/O, L186N	7	L1	XC2S600E	-	I/O, L186N	I/O, L186N_Y
I/O	7	M9	-	-	-	I/O
I/O, L185P	7	M8	XC2S600E	-	I/O, L185P	I/O, L185P_Y
I/O, L185N	7	M7	XC2S600E	-	I/O, L185N	I/O, L185N_Y
I/O, VREF Bank 7, L184P_YY	7	M6	All	All	I/O, VREF Bank 7, L184P_YY	I/O, VREF Bank 7, L184P_YY
I/O, L184N_YY	7	M5	All	-	I/O, L184N_YY	I/O, L184N_YY
I/O	7	M4	-	-	-	I/O
I/O, L183P_YY	7	M2	All	-	I/O, L183P_YY	I/O, L183P_YY
I/O, L183N_YY	7	M1	All	-	I/O, L183N_YY	I/O, L183N_YY
I/O	7	N9	-	-	-	I/O
I/O, L182P	7	N8	XC2S400E	-	I/O, L182P_Y	I/O, L182P
I/O, L182N	7	N7	XC2S400E	-	I/O, L182N_Y	I/O, L182N
I/O, VREF Bank 7, L181P	7	N6	XC2S600E	All	I/O, VREF Bank 7, L181P	I/O, VREF Bank 7, L181P_Y
I/O, L181N	7	N5	XC2S600E	-	I/O, L181N	I/O, L181N_Y
I/O	7	N4	-	-	-	I/O
I/O, L180P_YY	7	N3	All	-	I/O, L180P_YY	I/O, L180P_YY
I/O, L180N_YY	7	N2	All	-	I/O, L180N_YY	I/O, L180N_YY
I/O	7	N1	-	-	-	I/O
I/O, L179P_YY	7	P1	All	-	I/O, L179P_YY	I/O, L179P_YY
I/O (IRDY), L179N_YY	7	P2	All	-	I/O (IRDY), L179N_YY	I/O (IRDY), L179N_YY
I/O (TRDY), L178P	6	P3	XC2S600E	-	I/O (TRDY)	I/O (TRDY), L178P_Y
I/O, L178N	6	P4	XC2S600E	-	-	I/O, L178N_Y
I/O, L177P	6	P5	XC2S600E	-	-	I/O, L177P_Y
I/O, L177N	6	P6	XC2S600E	-	I/O	I/O, L177N_Y
I/O	6	P7	-	-	I/O	I/O
I/O, L176P	6	P8	XC2S600E	-	I/O, L176P	I/O, L176P_Y

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
DONE	3	AE26	-	-	DONE	DONE
PROGRAM	-	AC24	-	-	PROGRAM	PROGRAM
I/O (INIT), L101N_YY	3	AD25	All	-	I/O (INIT), L101N_YY	I/O (INIT), L101N_YY
I/O (D7), L101P_YY	3	AD26	All	-	I/O (D7), L101P_YY	I/O (D7), L101P_YY
I/O, L100N	3	AC25	-	-	-	I/O, L100N
I/O, L100P	3	AC26	-	-	-	I/O, L100P
I/O, L99N	3	AB22	XC2S600E	-	-	I/O, L99N_Y
I/O, L99P	3	AB23	XC2S600E	-	I/O	I/O, L99P_Y
I/O, L98N_YY	3	AB25	All	-	I/O, L98N_YY	I/O, L98N_YY
I/O, L98P_YY	3	AB26	All	-	I/O, L98P_YY	I/O, L98P_YY
I/O, L97N	3	AA23	-	-	I/O, L97N_Y	I/O, L97N
I/O, L97P	3	AA24	-	-	I/O, L97P_Y	I/O, L97P
I/O, VREF Bank 3, L96N	3	AA25	XC2S600E	All	I/O, VREF Bank 3, L96N	I/O, VREF Bank 3, L96N_Y
I/O, L96P	3	AA26	XC2S600E	-	I/O, L96P	I/O, L96P_Y
I/O, L95N	3	AA22	XC2S600E	-	-	I/O, L95N_Y
I/O, L95P	3	Y22	XC2S600E	-	I/O	I/O, L95P_Y
I/O, L94N	3	Y23	XC2S400E	-	I/O, L94N_Y	I/O, L94N
I/O, L94P	3	Y24	XC2S400E	-	I/O, L94P_Y	I/O, L94P
I/O, L93N	3	Y25	XC2S600E	-	I/O, L93N	I/O, L93N_Y
I/O, L93P	3	Y26	XC2S600E	-	I/O, L93P	I/O, L93P_Y
I/O, VREF Bank 3, L92N_YY	3	W21	All	All	I/O, VREF Bank 3, L92N_YY	I/O, VREF Bank 3, L92N_YY
I/O, L92P_YY	3	W22	All	-	I/O, L92P_YY	I/O, L92P_YY
I/O	3	Y21	-	-	-	I/O
I/O, L91N_YY	3	W25	All	-	I/O, L91N_YY	I/O, L91N_YY
I/O, L91P_YY	3	W26	All	-	I/O, L91P_YY	I/O, L91P_YY
I/O	3	W20	-	-	I/O	I/O
I/O, L90N	3	V19	XC2S400E	-	I/O, L90N_Y	I/O, L90N
I/O, L90P	3	V20	XC2S400E	-	I/O, L90P_Y	I/O, L90P
I/O, L89N	3	V21	XC2S600E	XC2S600E	-	I/O, VREF Bank 3, L89N_Y
I/O, L89P	3	V22	XC2S600E	-	I/O	I/O, L89P_Y
I/O	3	V23	-	-	I/O	I/O
I/O, L88N_YY	3	V24	All	-	I/O, L88N_YY	I/O, L88N_YY

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L64N_YY	2	J25	All	-	I/O, L64N_YY	I/O, L64N_YY
I/O (D2), L64P_YY	2	J24	All	-	I/O (D2), L64P_YY	I/O (D2), L64P_YY
I/O (D1)	2	J23	-	-	I/O (D1)	I/O (D1)
I/O, VREF Bank 2, L63N_YY	2	J22	All	All	I/O, VREF Bank 2, L63N_YY	I/O, VREF Bank 2, L63N_YY
I/O, L63P_YY	2	J21	All	-	I/O, L63P_YY	I/O, L63P_YY
I/O, L62N_YY	2	J20	All	-	I/O, L62N_YY	I/O, L62N_YY
I/O, L62P_YY	2	J19	All	-	I/O, L62P_YY	I/O, L62P_YY
I/O	2	H22	-	-	I/O	I/O
I/O, L61N	2	H26	XC2S600E	-	I/O	I/O, L61N_Y
I/O, L61P	2	H25	XC2S600E	XC2S600E	-	I/O, VREF Bank 2, L61P_Y
I/O, L60N	2	H21	XC2S400E	-	I/O, L60N_Y	I/O, L60N
I/O, L60P	2	H20	XC2S400E	-	I/O, L60P_Y	I/O, L60P
I/O	2	G26	-	-	-	I/O
I/O, L59N_YY	2	G25	All	-	I/O, L59N_YY	I/O, L59N_YY
I/O, L59P_YY	2	G24	All	-	I/O, L59P_YY	I/O, L59P_YY
I/O	2	G23	-	-	I/O	I/O
I/O, L58N_YY	2	G22	All	-	I/O, L58N_YY	I/O, L58N_YY
I/O, VREF Bank 2, L58P_YY	2	G21	All	All	I/O, VREF Bank 2, L58P_YY	I/O, VREF Bank 2, L58P_YY
I/O	2	G20	-	-	I/O	I/O
I/O, L57N_YY	2	F26	All	-	I/O, L57N_YY	I/O, L57N_YY
I/O, L57P_YY	2	F25	All	-	I/O, L57P_YY	I/O, L57P_YY
I/O, L56N	2	F24	XC2S600E	-	I/O, L56N	I/O, L56N_Y
I/O, L56P	2	F23	XC2S600E	-	I/O, L56P	I/O, L56P_Y
I/O	2	F22	-	-	-	I/O
I/O, L55N	2	E26	XC2S600E	-	I/O, L55N	I/O, L55N_Y
I/O, VREF Bank 2, L55P	2	E25	XC2S600E	All	I/O, VREF Bank 2, L55P	I/O, VREF Bank 2, L55P_Y
I/O, L54N	2	E23	XC2S400E	-	I/O, L54N_Y	I/O, L54N
I/O, L54P	2	E22	XC2S400E	-	I/O, L54P_Y	I/O, L54P
I/O, L53N_YY	2	F21	All	-	I/O, L53N_YY	I/O, L53N_YY
I/O, L53P_YY	2	E21	All	-	I/O, L53P_YY	I/O, L53P_YY
I/O, L52N	2	D26	XC2S600E	-	I/O	I/O, L52N_Y
I/O, L52P	2	D25	XC2S600E	-	-	I/O, L52P_Y