AMD Xilinx - XC2S200E-6PQ208I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1176
Number of Logic Elements/Cells	5292
Total RAM Bits	57344
Number of I/O	146
Number of Gates	200000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s200e-6pq208i

General Overview

The Spartan-IIE family of FPGAs have a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), surrounded by a perimeter of programmable Input/Output Blocks (IOBs). There are four Delay-Locked Loops (DLLs), one at each corner of the die. Two columns of block RAM lie on opposite sides of the die, between the CLBs and the IOB columns. The XC2S400E has four columns and the XC2S600E has six columns of block RAM. These functional elements are interconnected by a powerful hierarchy of versatile routing channels (see Figure 1).

Spartan-IIE FPGAs are customized by loading configuration data into internal static memory cells. Unlimited reprogramming cycles are possible with this approach. Stored values in these cells determine logic functions and interconnections implemented in the FPGA. Configuration data can be read from an external serial PROM (master serial mode), or written into the FPGA in slave serial, slave parallel, or Boundary Scan modes. Xilinx offers multiple types of low-cost configuration solutions including the Platform Flash in-system programmable configuration PROMs.

Spartan-IIE FPGAs are typically used in high-volume applications where the versatility of a fast programmable solution adds benefits. Spartan-IIE FPGAs are ideal for shortening product development cycles while offering a cost-effective solution for high volume production.

Spartan-IIE FPGAs achieve high-performance, low-cost operation through advanced architecture and semiconductor technology. Spartan-IIE devices provide system clock rates beyond 200 MHz. In addition to the conventional benefits of high-volume programmable logic solutions, Spartan-IIE FPGAs also offer on-chip synchronous single-port and dual-port RAM (block and distributed form), DLL clock drivers, programmable set and reset on all flip-flops, fast carry logic, and many other features.

Spartan-IIE Family Compared to Spartan-II Family

- Higher density and more I/O
- Higher performance
- Unique pinouts in cost-effective packages
- Differential signaling
  - LVDS, Bus LVDS, LVPECL
- V_{CCINT} = 1.8V
  - Lower power
  - 5V tolerance with external resistor
  - 3V tolerance directly
- PCI, LVTTL, and LVCMOS2 input buffers powered by V_{CCO} instead of V_{CCINT}
- Unique larger bitstream

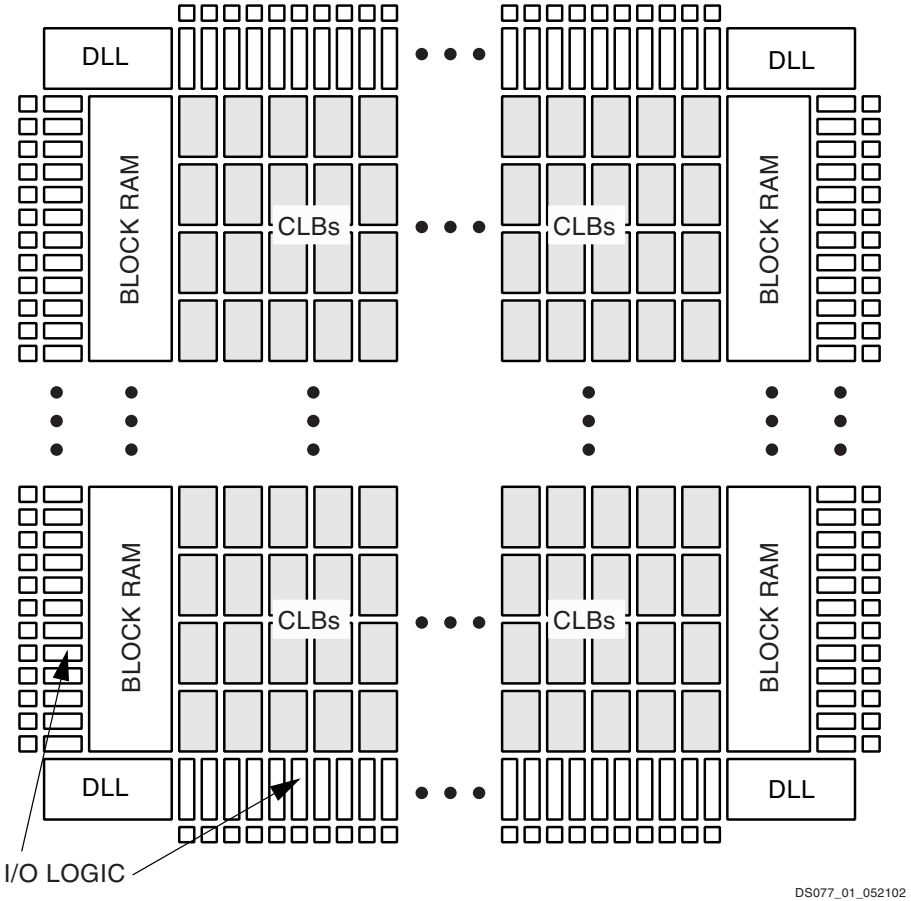


Figure 1: **Basic Spartan-IIE Family FPGA Block Diagram**

is required for most output standards and for LVTTL, LVCMOS, and PCI inputs.

Table 4: **Compatible Standards**

V_{CCO}	Compatible Standards
3.3V	PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, LVPECL, GTL, GTL+
2.5V	SSTL2 I, SSTL2 II, LVCMOS2, LVDS, Bus LVDS, GTL, GTL+
1.8V	LVCMOS18, GTL, GTL+
1.5V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage, V_{REF}. In this case, certain user-I/O pins are automatically configured as inputs for the V_{REF} voltage. About one in six of the I/O pins in the bank assume this role.

V_{REF} pins within a bank are interconnected internally and consequently only one V_{REF} voltage can be used within each bank. All V_{REF} pins in the bank, however, must be connected to the external voltage source for correct operation.

In a bank, inputs requiring V_{REF} can be mixed with those that do not but only one V_{REF} voltage may be used within a bank. The V_{CCO} and V_{REF} pins for each bank appear in the device pinout tables.

Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device. All V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage, and not used for I/O.

Table 5: **I/O Banking**

Package	TQ144, PQ208	FT256, FG456, FG676
V_{CCO} Banks	Interconnected as 1	8 independent
V_{REF} Banks	8 independent	8 independent

See Xilinx® Application Note XAPP179 for more information on I/O resources.

Hot Swap, Hot Insertion, Hot Socketing Support

The I/O pins support hot swap — also called hot insertion and hot socketing — and are considered CompactPCI Friendly according to the PCI Bus v2.2 Specification. Consequently, an unpowered Spartan-IIE FPGA can be plugged directly into a powered system or backplane without affecting or damaging the system or the FPGA. The hot swap functionality is built into every XC2S150E, XC2S400E, and XC2S600E device. All other Spartan-IIE devices built after Product Change Notice PCN2002-05 also include hot swap functionality.

To support hot swap, Spartan-IIE devices include the following I/O features.

- Signals can be applied to Spartan-IIE FPGA I/O pins before powering the FPGA's V_{CCINT} or V_{CCO} supply inputs.
- Spartan-IIE FPGA I/O pins are high-impedance (i.e., three-stated) before and throughout the power-up and configuration processes when employing a configuration mode that does not enable the preconfiguration weak pull-up resistors (see Table 11, page 22).
- There is no current path from the I/O pin back to the V_{CCINT} or V_{CCO} voltage supplies.
- Spartan-IIE FPGAs are immune to latch-up during hot swap.

Once connected to the system, each pin adds a small amount of capacitance (C_{IN}). Likewise, each I/O consumes a small amount of DC current, equivalent to the input leakage specification (I_L). There also may be a small amount of temporary AC current (I_{HSPO}) when the pin input voltage exceeds V_{CCO} plus 0.4V, which lasts less than 10 ns.

A weak-keeper circuit within each user-I/O pin is enabled during the last frame of configuration data and has no noticeable effect on robust system signals driven by an active driver or a strong pull-up or pull-down resistor. Undriven or floating system signals may be affected. The specific effect depends on how the I/O pin is configured. User-I/O pins configured as outputs or enabled outputs have a weak pull-up resistor to V_{CCO} during the last configuration frame. User-I/O pins configured as inputs or bidirectional I/Os have weak pull-down resistors. The weak-keeper circuit turns off when the DONE pin goes High, provided that it is not used in the configured application.

Configurable Logic Block

The basic building block of the Spartan-IIE FPGA CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and storage element. The output from the function generator in each LC drives the CLB output or the D input of the flip-flop. Each Spartan-IIE FPGA CLB contains four LCs, organized in two similar slices; a single slice is shown in Figure 6.

In addition to the four basic LCs, the Spartan-IIE FPGA CLB contains logic that combines function generators to provide functions of five or six inputs.

Look-Up Tables

Spartan-IIE FPGA function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16 x 1-bit dual-port synchronous RAM.

The Spartan-IIE FPGA LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

Storage Elements

Storage elements in the Spartan-IIE FPGA slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals may be configured to operate asynchronously.

All control signals are independently invertible, and are shared by the two flip-flops within the slice.

edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

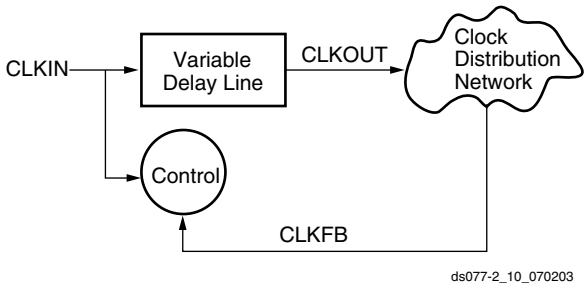


Figure 12: **Delay-Locked Loop Block Diagram**

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16. The phase-shifted output have optional duty-cycle correction (Figure 13).

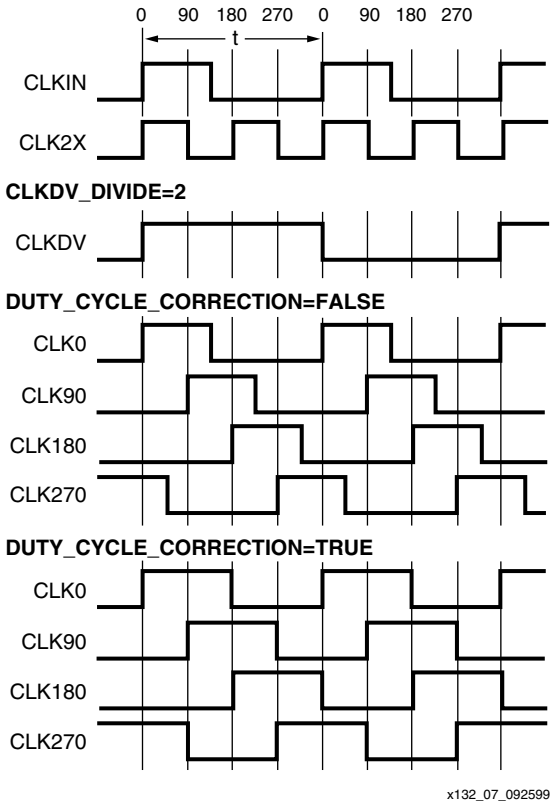


Figure 13: **DLL Output Characteristics**

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to deskew a board level clock among multiple Spartan-IIE devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock. If the DLL uses external feedback, apply a reset after startup to ensure consistent locking to the external signal. See Xilinx Application Note XAPP174 for more information on DLLs.

Boundary Scan

Spartan-IIE devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, and HIGHZ instructions. The TAP also supports two USERCODE instructions, internal scan chains, and configuration/readback of the device.

The TAP uses dedicated package pins that always operate using LVTTL. For TDO to operate using LVTTL, the V_{CCO} for Bank 2 must be 3.3V. Otherwise, TDO switches rail-to-rail between ground and V_{CCO}. The boundary-scan input pins (TDI, TMS, TCK) do not have a V_{CCO} requirement and operate with either 2.5V or 3.3V input signaling levels. TDI, TMS, and TCK hava a default internal weak pull-up resistor, and TDO has no default resistor. Bitstream options allow setting any of the four TAP pins to have an internal pull-up, pull-down, or neither.

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including unbonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections.

Table 8 lists the boundary-scan instructions supported in Spartan-IIE FPGAs. Internal signals can be captured during EXTEST by connecting them to unbonded or unused IOBs. They may also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Table 8: **Boundary-Scan Instructions**

Boundary-Scan Command	Binary Code[4:0]	Description
EXTEST	00000	Enables boundary-scan EXTEST operation
SAMPLE/ PRELOAD	00001	Enables boundary-scan SAMPLE/PRELOAD operation
USER1	00010	Access user-defined register 1
USER2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for Readback
CFG_IN	00101	Access the configuration bus for Configuration

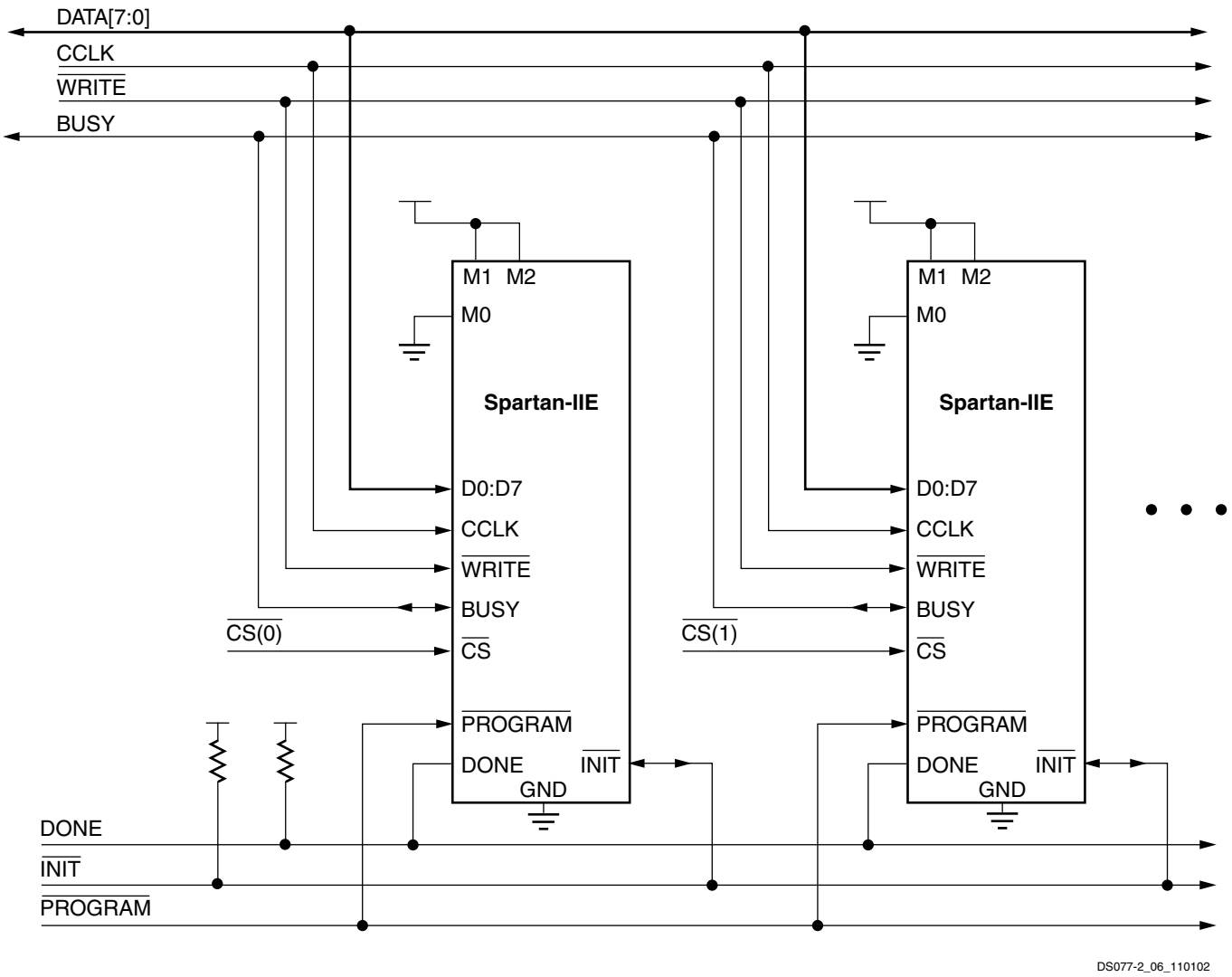


Figure 20: **Slave Parallel Configuration Circuit Diagram**

Multiple Spartan-IIE FPGAs can be configured using the Slave Parallel mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, $\overline{\text{WRITE}}$, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the $\overline{\text{CS}}$ pin of each device in turn and writing the appropriate data. Sync-to-DONE start-up timing is used to ensure that the start-up sequence does not begin until all the FPGAs have been loaded. See Start-up, page 23.

Write

When using the Slave Parallel Mode, write operations send packets of byte-wide configuration data into the FPGA. Figure 21, page 28 shows a flowchart of the write sequence used to load data into the Spartan-IIE FPGA. This is an expansion of the "Load Configuration Data Frames" block in Figure 16, page 23.

The timing for Slave Parallel mode is shown in Figure 26, page 50.

For the present example, the user holds $\overline{\text{WRITE}}$ and $\overline{\text{CS}}$ Low throughout the sequence of write operations. Note that when $\overline{\text{CS}}$ is asserted on successive CCLKs, $\overline{\text{WRITE}}$ must remain either asserted or deasserted. Otherwise an abort will be initiated, as in the next section.

1. Drive data onto D0-D7. Note that to avoid contention, the data source should not be enabled while $\overline{\text{CS}}$ is Low and $\overline{\text{WRITE}}$ is High. Similarly, while $\overline{\text{WRITE}}$ is High, no more than one device's $\overline{\text{CS}}$ should be asserted.
2. On the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this happens.
3. Repeat steps 1 and 2 until all the data has been sent.
4. Deassert $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$.

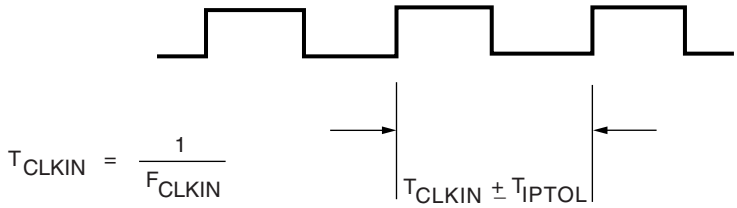
IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in IOB Output Delay Adjustments for Different Standards(1), page 40.

Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Propagation Delays						
T_{IOOP}	O input to pad	1.0	2.7	1.0	2.9	ns
T_{IOOLP}	O input to pad via transparent latch	1.2	3.1	1.2	3.4	ns
3-state Delays						
T_{IOTHZ}	T input to pad high impedance(1)	0.7	1.7	0.7	1.9	ns
T_{IOTON}	T input to valid data on pad	1.1	2.9	1.1	3.1	ns
$T_{IOTLPHZ}$	T input to pad high impedance via transparent latch(1)	0.8	2.0	0.8	2.2	ns
$T_{IOTLPON}$	T input to valid data on pad via transparent latch	1.2	3.2	1.2	3.4	ns
T_{GTS}	GTS to pad high impedance(1)	1.9	4.6	1.9	4.9	ns
Sequential Delays						
T_{IOCKP}	Clock CLK to pad	0.9	2.8	0.9	2.9	ns
T_{IOCKHZ}	Clock CLK to pad high impedance (synchronous)(1)	0.7	2.0	0.7	2.2	ns
T_{IOCKON}	Clock CLK to valid data on pad (synchronous)	1.1	3.2	1.1	3.4	ns
Setup/Hold Times with Respect to Clock CLK						
T_{IOOCK} / T_{IOCKO}	O input	1.0 / 0	-	1.1 / 0	-	ns
$T_{IOOCECK}$ / $T_{IOCKOCE}$	OCE input	0.7 / 0	-	0.7 / 0	-	ns
$T_{IOSRCKO}$ / $T_{IOCKOSR}$	SR input (OFF)	0.9 / 0	-	1.0 / 0	-	ns
T_{IOTCK} / T_{IOCKT}	3-state setup times, T input	0.6 / 0	-	0.7 / 0	-	ns
$T_{IOTCECK}$ / $T_{IOCKTCE}$	3-state setup times, TCE input	0.6 / 0	-	0.8 / 0	-	ns
$T_{IOSRCKT}$ / $T_{IOCKTSR}$	3-state setup times, SR input (TFF)	0.9 / 0	-	1.0 / 0	-	ns
Set/Reset Delays						
T_{IOSRP}	SR input to pad (asynchronous)	1.2	3.3	1.2	3.5	ns
T_{IOSRHZ}	SR input to pad high impedance (asynchronous)(1)	1.0	2.4	1.0	2.7	ns
T_{IOSRON}	SR input to valid data on pad (asynchronous)	1.4	3.7	1.4	3.9	ns
T_{IOGSRQ}	GSR to pad	3.8	8.5	3.8	9.7	ns

Notes:
1. Three-state turn-off delays should not be adjusted.

Period Tolerance: the allowed input clock period change in nanoseconds.



Output Jitter: the difference between an ideal reference clock edge and the actual design.

Phase Offset and Maximum Phase Difference

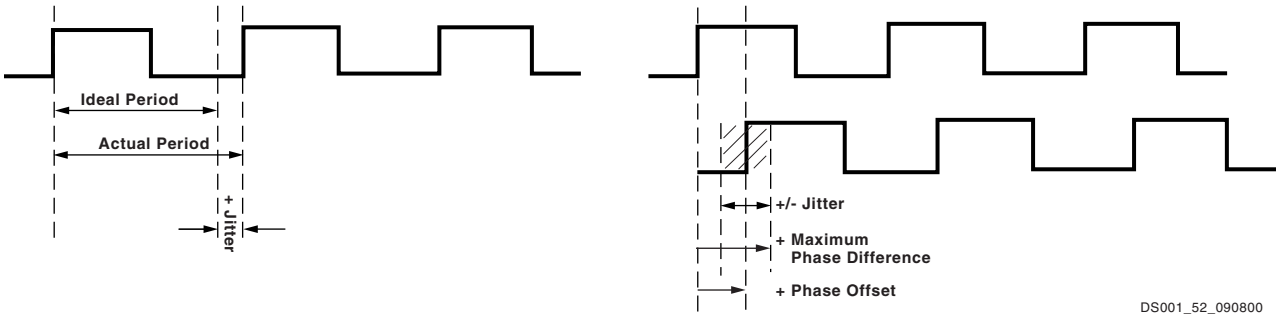


Figure 22: **Period Tolerance and Clock Jitter**

CLB Distributed RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Sequential Delays						
$T_{SHCKO16}$	Clock CLK to X/Y outputs (WE active, 16 x 1 mode)	0.6	1.5	0.6	1.7	ns
$T_{SHCKO32}$	Clock CLK to X/Y outputs (WE active, 32 x 1 mode)	0.8	1.9	0.8	2.1	ns
Setup/Hold Times with Respect to Clock CLK						
T_{AS} / T_{AH}	F/G address inputs	0.42 / 0	-	0.5 / 0	-	ns
T_{DS} / T_{DH}	BX/BY data inputs (DIN)	0.53 / 0	-	0.6 / 0	-	ns
T_{WS} / T_{WH}	CE input (WS)	0.7 / 0	-	0.8 / 0	-	ns
Clock CLK						
T_{WPH}	Pulse width, High	2.1	-	2.4	-	ns
T_{WPL}	Pulse width, Low	2.1	-	2.4	-	ns
T_{WC}	Clock period to meet address write cycle time	4.2	-	4.8	-	ns

CLB Shift Register Switching Characteristics

Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Sequential Delays						
T_{REG}	Clock CLK to X/Y outputs	1.2	2.9	1.2	3.2	ns
Setup/Hold Times with Respect to Clock CLK						
T_{SHDICK}	BX/BY data inputs (DIN)	0.53 / 0	-	0.6 / 0	-	ns
T_{SHCECK}	CE input (WS)	0.7 / 0	-	0.8 / 0	-	ns
Clock CLK						
T_{SRPH}	Pulse width, High	2.1	-	2.4	-	ns
T_{SRPL}	Pulse width, Low	2.1	-	2.4	-	ns

Block RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Sequential Delays						
T_{BCKO}	Clock CLK to DOUT output	0.6	3.1	0.6	3.5	ns
Setup/Hold Times with Respect to Clock CLK						
T_{BACK} / T_{BCKA}	ADDR inputs	1.0 / 0	-	1.1 / 0	-	ns
T_{BDCK}/ T_{BCKD}	DIN inputs	1.0 / 0	-	1.1 / 0	-	ns
T_{BECK}/ T_{BCKE}	EN inputs	2.2 / 0	-	2.5 / 0	-	ns
T_{BRCK}/ T_{BCKR}	RST input	2.1 / 0	-	2.3 / 0	-	ns
T_{BWCK}/ T_{BCKW}	WEN input	2.0 / 0	-	2.2 / 0	-	ns
Clock CLK						
T_{BPWH}	Pulse width, High	1.4	-	1.5	-	ns
T_{BPWL}	Pulse width, Low	1.4	-	1.5	-	ns
T_{BCCS}	CLKA -> CLKB setup time for different ports	2.7	-	3.0	-	ns

Low Voltage Differential Signals (LVDS and LVPECL)

The Spartan-IIE family features low-voltage differential signaling (LVDS and LVPECL). Each signal utilizes two pins on the Spartan-IIE device, known as differential pin pairs. Each differential pin pair has a Positive (P) and a Negative (N) pin. These pairs are labeled in the following manner.

I/O, L#[P/N][-/_Y/_YY]

where

L = LVDS or LVPECL pin

= Pin pair number

P = Positive

N = Negative

_Y = Asynchronous output allowed (device-dependent)

_YY = Asynchronous output allowed (all devices)

Available Differential Pairs According to Package Type

Device	TQ144	PQ208	FT256	FG456	FG676
XC2S50E	28	50	83	-	-
XC2S100E	28	50	83	86	-
XC2S150E	-	50	83	114	-
XC2S200E	-	50	83	120	-
XC2S300E	-	50	83	120	-
XC2S400E	-	-	83	120	172
XC2S600E	-	-	-	120	205

Synchronous or Asynchronous

I/O pins for differential signals can either be synchronous or asynchronous, input or output. Differential signaling requires the pins of each pair to switch simultaneously. If the output signals driving the pins are from IOB flip-flops, they are synchronous. If the signals driving the pins are from internal logic, they are asynchronous, and therefore more care must be taken that they are simultaneous. Any differential pairs can be used for synchronous input and output signals as well as asynchronous input signals.

However, only the differential pairs with the _Y or _YY suffix can be used for asynchronous output signals.

Asynchronous Output Pad Name Designation

Because of differences between densities, the differential pairs that can be used for asynchronous outputs vary by device. The pairs that are available in all densities for a given package have the _YY suffix. These pins should be used for differential asynchronous outputs if the design may later move to a different density. All other differential pairs that can be used for asynchronous outputs have the _Y suffix.

To simplify the following tables, the "Pad Name" column shows the part of the name that is common across densities. The "Pad Name" column leaves out the _Y suffix and the "LVDS Asynchronous Output Option" column indicates the densities that allow asynchronous outputs for LVDS or LVPECL on the given pin.

DLL Pins

Pins labeled "I/O (DLL)" can be used as general-purpose I/O or as inputs to the DLL. Adjacent DLL pins form a differential pair. They reside in two different banks, so if they are outputs the V_{CCO} level must be the same for both banks. Each DLL pin can also be paired with the adjacent GCK clock pin for a differential clock input. The "I/O (DLL)" pin always becomes the N terminal when paired with GCK, even if it is labeled "P" for its pairing with the adjacent DLL pin.

VREF Pins

Pins labeled "I/O, VREF" can be used as either an I/O or a VREF pin. If any I/O pin within the bank requires a VREF input, all the VREF pins in the bank must be connected to the same voltage. See the I/O banking rules in the Functional Description module for more detail. If no pin in a given bank requires VREF, then that bank's VREF pins can be used as general I/O.

To simplify the following tables, the "Pad Name" column shows the part of the name that is common across densities. When VREF is only available in limited densities, the "Pad Name" column leaves out the VREF designation and the "VREF Option" column indicates the densities that provide VREF on the given pin.

VCCO Banks

In the TQ144 and PQ208 packages, the eight banks have VCCO connected together. Thus, only one VCCO is allowed in these packages, although different VREF values are allowed in each of the eight banks. See I/O Banking.

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 6, L39P	6	P45	XC2S100E, 150E	All
I/O, L39N	6	P46	XC2S100E, 150E	-
I/O	6	P47	-	XC2S200E, 300E
I/O, L38P_YY	6	P48	All	-
I/O, L38N_YY	6	P49	All	-
M1	-	P50	-	-
GND	-	P51	-	-
M0	-	P52	-	-
VCCO	-	P53	-	-
M2	-	P54	-	-
I/O, L37N_YY	5	P55	All	-
I/O, L37P_YY	5	P56	All	-
I/O	5	P57	-	XC2S200E, 300E
I/O	5	P58	-	-
I/O, VREF Bank 5, L36N_YY	5	P59	All	All
I/O, L36P_YY	5	P60	All	-
I/O, L35N	5	P61	XC2S50E, 100E, 300E	-
I/O, L35P	5	P62	XC2S50E, 100E, 300E	-
I/O, L34N	5	P63	XC2S50E, 100E, 200E, 300E	XC2S100E, 150E, 200E, 300E
I/O, L34P	5	P64	XC2S50E, 100E, 200E, 300E	-
GND	-	P65	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
VCCO	-	P66	-	-
VCCINT	-	P67	-	-
I/O, L33N	5	P68	XC2S50E, 100E, 200E, 300E	-
I/O, L33P	5	P69	XC2S50E, 100E, 200E, 300E	-
I/O	5	P70	-	-
I/O, L32N	5	P71	XC2S100E, 150E	-
GND	-	P72	-	-
I/O, VREF Bank 5, L32P	5	P73	XC2S100E, 150E	All
I/O	5	P74	-	-
I/O (DLL), L31N	5	P75	-	-
VCCINT	-	P76	-	-
GCK1, I	5	P77	-	-
VCCO	-	P78	-	-
GND	-	P79	-	-
GCK0, I	4	P80	-	-
I/O (DLL), L31P	4	P81	-	-
I/O	4	P82	-	-
I/O, L30N	4	P83	XC2S50E, 200E, 300E	-
I/O, VREF Bank 4, L30P	4	P84	XC2S50E, 200E, 300E	All
GND	-	P85	-	-
I/O, L29N	4	P86	XC2S50E, 200E, 300E	-
I/O, L29P	4	P87	XC2S50E, 200E, 300E	-
I/O, L28N	4	P88	XC2S50E, 100E, 200E, 300E	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 1, L6P	1	P178	XC2S50E, 200E, 300E	All
I/O, L6N	1	P179	XC2S50E, 200E, 300E	-
I/O	1	P180	-	-
I/O (DLL), L5P	1	P181	-	-
GCK2, I	1	P182	-	-
GND	-	P183	-	-
VCCO	-	P184	-	-
GCK3, I	0	P185	-	-
VCCINT	-	P186	-	-
I/O (DLL), L5N	0	P187	-	-
I/O, L4P	0	P188	XC2S50E, 200E, 300E	-
I/O, VREF Bank 0, L4N	0	P189	XC2S50E, 200E, 300E	All
GND	-	P190	-	-
I/O, L3P	0	P191	XC2S50E, 200E, 300E	-
I/O, L3N	0	P192	XC2S50E, 200E, 300E	-
I/O, L2P	0	P193	XC2S50E, 100E, 200E, 300E	-
I/O, L2N	0	P194	XC2S50E, 100E, 200E, 300E	-
VCCINT	-	P195	-	-
VCCO	-	P196	-	-
GND	-	P197	-	-
I/O, L1P	0	P198	XC2S50E, 100E, 200E, 300E	-
I/O, L1N	0	P199	XC2S50E, 100E, 200E, 300E	XC2S100E, 150E, 200E, 300E
I/O	0	P200	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O	0	P201	-	-
I/O, L0P_YY	0	P202	All	-
I/O, VREF Bank 0, L0N_YY	0	P203	All	All
I/O	0	P204	-	-
I/O	0	P205	-	XC2S200E, 300E
I/O	0	P206	-	-
TCK	-	P207	-	-
VCCO	-	P208	-	-

PQ208 Differential Clock Pins

Clock	Bank	P		N	
		Pin	Name	Pin	Name
GCK0	4	P80	GCK0, I	P81	I/O (DLL), L31P
GCK1	5	P77	GCK1, I	P75	I/O (DLL), L31N
GCK2	1	P182	GCK2, I	P181	I/O (DLL), L5P
GCK3	0	P185	GCK3, I	P187	I/O (DLL), L5N

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L6P	0	C7	XC2S50E, 200E, 300E, 400E	-
I/O, L6N	0	B7	XC2S50E, 200E, 300E, 400E	-
I/O	0	A6	-	-
I/O, L5P	0	B6	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L5N	0	C6	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L4P	0	A5	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L4N	0	B5	XC2S50E, 100E, 200E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L3P	0	D6	XC2S50E, 100E, 300E	-
I/O, L3N	0	E6	XC2S50E, 100E, 300E	-
I/O, L2P_YY	0	D5	All	-
I/O, VREF Bank 0, L2N_YY	0	C5	All	All
I/O, L1P_YY	0	B4	All	-
I/O, L1N_YY	0	C4	All	-
I/O, L0P_YY	0	A4	All	-
I/O, L0N_YY	0	A3	All	XC2S200E, 300E, 400E
I/O	0	B3	-	-
TCK	-	A2	-	-

Notes:
1. Although designated with the _YY suffix in the XC2S50E, XC2S100E, XC2S150E, XC2S200E, and XC2S300E, these differential pairs are not asynchronous in the XC2S400E.
2. There is no pair L37.

FT256 Differential Clock Pins

Clock	Bank	P		N	
		Pin	Name	Pin	Name
GCK0	4	T9	GCK0, I	R9	I/O (DLL), L52P
GCK1	5	T8	GCK1, I	R8	I/O (DLL), L52N
GCK2	1	B8	GCK2, I	A8	I/O (DLL), L8P
GCK3	0	C8	GCK3, I	D8	I/O (DLL), L8N

Additional FT256 Package Pins

VCCINT Pins				
C3	C14	D4	D13	E5
E12	M5	M12	N4	N13
P3	P14	-	-	-
VCCO Bank 0 Pins				
E8	F7	F8	-	-
VCCO Bank 1 Pins				
E9	F9	F10	-	-
VCCO Bank 2 Pins				
G11	H11	H12	-	-
VCCO Bank 3 Pins				
J11	J12	K11	-	-
VCCO Bank 4 Pins				
L9	L10	M9	-	-

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O, L#P_YY	7	L5	All	-	I/O, L75P_YY	I/O, L99P_YY	I/O, L105P_YY	I/O, L105P_YY	I/O, L105P_YY	I/O, L105P_YY
I/O (IRDY), L#N_YY	7	L6	All	-	I/O (IRDY), L75N_YY	I/O (IRDY), L99N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY
I/O (TRDY)	6	M1	-	-	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)
I/O	6	M2	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P_Y	6	M3	XC2S200E, 300E, 600E	-	-	I/O	I/O, L104P_Y	I/O, L104P_Y	I/O, L104P	I/O, L104P_Y
I/O, L#N_Y	6	M4	XC2S100E, 150E, 200E, 300E, 600E	XC2S400E, 600E	I/O, L74P_Y	I/O, L98P_Y	I/O, L104N_Y	I/O, L104N_Y	I/O, VREF Bank 6, L104N	I/O, VREF Bank 6, L104N_Y
I/O, L#P_Y	6	M5	XC2S100E, 150E, 300E, 400E	-	I/O, L74N_Y	I/O, L98N_Y	I/O, L103P	I/O, L103P_Y	I/O, L103P_Y	I/O, L103P
I/O, L#N_Y	6	M6	XC2S300E, 400E	-	-	-	I/O, L103N	I/O, L103N_Y	I/O, L103N_Y	I/O, L103N
I/O	6	N1	-	-	-	-	-	I/O	I/O	I/O
I/O	6	N2	-	-	I/O, L73P	I/O, L97P	I/O	I/O	I/O	I/O
I/O, VREF Bank 6, L#P	6	N3	XC2S200E, 400E	All	I/O, VREF Bank 6, L73N	I/O, VREF Bank 6, L97N	I/O, VREF Bank 6, L102P_Y	I/O, VREF Bank 6, L102P	I/O, VREF Bank 6, L102P_Y	I/O, VREF Bank 6, L102P
I/O, L#N	6	N4	XC2S100E, 150E, 200E, 400E	-	I/O, L72P_Y	I/O, L96P_Y	I/O, L102N_Y	I/O, L102N	I/O, L102N_Y	I/O, L102N
I/O, L#P_Y	6	N5	XC2S100E, 150E, 300E, 600E	-	I/O, L72N_Y	I/O, L96N_Y	I/O, L101P	I/O, L101P_Y	I/O, L101P	I/O, L101P_Y
I/O, L#N_Y	6	N6	XC2S300E, 600E	-	-	-	I/O, L101N	I/O, L101N_Y	I/O, L101N	I/O, L101N_Y
I/O, L#P_Y	6	P1	XC2S150E, 200E, 300E, 600E	-	-	I/O, L95P_Y	I/O, L100P_Y	I/O, L100P_Y	I/O, L100P	I/O, L100P_Y
I/O, L#N_Y	6	P2	XC2S100E, 150E, 200E, 300E, 600E	-	I/O, L71P_Y	I/O, L95N_Y	I/O, L100N_Y	I/O, L100N_Y	I/O, L100N	I/O, L100N_Y
I/O	6	R1	XC2S100E, 150E	-	I/O, L71N_Y	I/O, L94P_Y	I/O	I/O	I/O	I/O
I/O, L#P_Y	6	P3	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L94N_Y	I/O, L99P_Y	I/O, L99P_Y	I/O, L99P_Y	I/O, L99P_Y
I/O, L#N_Y	6	P4	XC2S200E, 300E, 400E, 600E	-	-	-	I/O, L99N_Y	I/O, L99N_Y	I/O, L99N_Y	I/O, L99N_Y
I/O, L#P_YY	6	P5	All	-	I/O, L70P_YY	I/O, L93P_YY	I/O, L98P_YY	I/O, L98P_YY	I/O, L98P_YY	I/O, L98P_YY
I/O, L#N_YY	6	P6	All	-	I/O, L70N_YY	I/O, L93N_YY	I/O, L98N_YY	I/O, L98N_YY	I/O, L98N_YY	I/O, L98N_YY

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O, L#N	3	V19	XC2S150E, 200E, 300E, 400E	-	-	I/O, L54N_Y	I/O, L58N_Y	I/O, L58N_Y	I/O, L58N_Y	I/O, L58N
I/O, L#P	3	V20	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L54P_Y	I/O, L58P_Y	I/O, L58P_Y	I/O, L58P_Y	I/O, L58P
I/O, L#N	3	V22	XC2S100E, 200E, 300E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L40N_Y	I/O, L53N	I/O, VREF Bank 3, L57N_Y	I/O, VREF Bank 3, L57N_Y	I/O, VREF Bank 3, L57N	I/O, VREF Bank 3, L57N_Y
I/O, L#P	3	U22	XC2S100E, 200E, 300E, 600E	-	I/O, L40P_Y	I/O, L53P	I/O, L57P_Y	I/O, L57P_Y	I/O, L57P	I/O, L57P_Y
I/O	3	U21	-	-	-	-	-	I/O	I/O	I/O
I/O	3	U20	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N	3	U18	XC2S100E, 200E, 300E, 600E	-	I/O, L39N_Y	I/O, L52N	I/O, L56N_Y	I/O, L56N_Y	I/O, L56N	I/O, L56N_Y
I/O, L#P	3	U19	XC2S100E, 200E, 300E, 600E	-	I/O, L39P_Y	I/O, L52P	I/O, L56P_Y	I/O, L56P_Y	I/O, L56P	I/O, L56P_Y
I/O, VREF Bank 3, L#N	3	T21	XC2S150E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 3, L38N	I/O, VREF Bank 3, L51N_Y	I/O, VREF Bank 3, L55N_Y	I/O, VREF Bank 3, L55N_Y	I/O, VREF Bank 3, L55N_Y	I/O, VREF Bank 3, L55N_Y
I/O, L#P	3	T22	XC2S150E, 200E, 300E, 400E, 600E	-	I/O, L38P	I/O, L51P_Y	I/O, L55P_Y	I/O, L55P_Y	I/O, L55P_Y	I/O, L55P_Y
I/O	3	T20	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N	3	T18	XC2S150E, 200E, 300E, 400E	-	-	I/O, L50N_Y	I/O, L54N_Y	I/O, L54N_Y	I/O, L54N_Y	I/O, L54N
I/O, L#P	3	T19	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L50P_Y	I/O, L54P_Y	I/O, L54P_Y	I/O, L54P_Y	I/O, L54P
I/O, L#N	3	R21	XC2S100E, 150E, 300E, 600E	XC2S600E	I/O, L37N_Y	I/O, L49N_Y	I/O, L53N	I/O, L53N_Y	I/O, L53N	I/O, VREF Bank 3, L53N_Y
I/O, L#P	3	R22	XC2S100E, 150E, 300E, 600E	-	I/O, L37P_Y	I/O, L49P_Y	I/O, L53P	I/O, L53P_Y	I/O, L53P	I/O, L53P_Y
I/O	3	R20	-	-	-	-	-	I/O	I/O	I/O
I/O, VREF Bank 3, L#N	3	R18	XC2S300E, 400E, 600E	All	I/O, VREF Bank 3, L36N	I/O, VREF Bank 3, L48N	I/O, VREF Bank 3, L52N	I/O, VREF Bank 3, L52N_Y	I/O, VREF Bank 3, L52N_Y	I/O, VREF Bank 3, L52N_Y
I/O (D6), L#P	3	R19	XC2S300E, 400E, 600E	-	I/O (D6), L36P	I/O (D6), L48P	I/O (D6), L52P	I/O (D6), L52P_Y	I/O (D6), L52P_Y	I/O (D6), L52P_Y
I/O (D5), L#N_YY	3	P22	All	-	I/O (D5), L35N_YY	I/O (D5), L47N_YY	I/O (D5), L51N_YY	I/O (D5), L51N_YY	I/O (D5) L51N_YY	I/O (D5), L51N_YY
I/O, L#P_YY	3	P21	All	-	I/O, L35P_YY	I/O, L47P_YY	I/O, L51P_YY	I/O, L51P_YY	I/O, L51P_YY	I/O, L51P_YY

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O, L#N	1	A15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L14N_Y	I/O, L18N	I/O, L20N_Y	I/O, L20N_Y	I/O, L20N_Y	I/O, L20N_Y
I/O	1	E14	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#P	1	D14	XC2S150E, 300E, 400E, 600E	-	-	I/O, L17P_Y	I/O, L19P	I/O, L19P_Y	I/O, L19P_Y	I/O, L19P_Y
I/O, L#N	1	C14	XC2S100E, 150E, 300E, 400E, 600E	-	I/O, L13P_Y	I/O, L17N_Y	I/O, L19N	I/O, L19N_Y	I/O, L19N_Y	I/O, L19N_Y
I/O, L#P	1	B14	XC2S100E, 150E, 300E, 400E, 600E	-	I/O, L13N_Y	I/O, L16P_Y	I/O, L18P	I/O, L18P_Y	I/O, L18P_Y	I/O, L18P_Y
I/O, L#N	1	A14	XC2S150E, 300E, 400E, 600E	-	-	I/O, L16N_Y	I/O, L18N	I/O, L18N_Y	I/O, L18N_Y	I/O, L18N_Y
I/O	1	E13	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#P	1	D13	XC2S200E, 300E, 400E, 600E	-	I/O, L12P	I/O, L15P	I/O, L17P_Y	I/O, L17P_Y	I/O, L17P_Y	I/O, L17P_Y
I/O, L#N	1	C13	XC2S200E, 300E, 400E, 600E	-	I/O, L12N	I/O, L15N	I/O, L17N_Y	I/O, L17N_Y	I/O, L17N_Y	I/O, L17N_Y
I/O, VREF Bank 1, L#P	1	B13	XC2S200E, 300E, 400E, 600E	All	I/O, VREF Bank 1, L11P	I/O, VREF Bank 1, L14P	I/O, VREF Bank 1, L16P_Y	I/O, VREF Bank 1, L16P_Y	I/O, VREF Bank 1, L16P_Y	I/O, VREF Bank 1, L16P_Y
I/O, L#N	1	A13	XC2S200E, 300E, 400E, 600E	-	I/O, L11N	I/O, L14N	I/O, L16N_Y	I/O, L16N_Y	I/O, L16N_Y	I/O, L16N_Y
I/O	1	F13	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P	1	C12	XC2S300E, 600E	-	-	-	I/O, L15P	I/O, L15P_Y	I/O, L15P	I/O, L15P_Y
I/O, L#N	1	B12	XC2S300E, 600E	-	I/O, L10P	I/O	I/O, L15N	I/O, L15N_Y	I/O, L15N	I/O, L15N_Y
I/O, L#P	1	D12	XC2S150E, 300E, 600E	XC2S400E, 600E	I/O, L10N	I/O, L13P_Y	I/O, L14P	I/O, L14P_Y	I/O, VREF Bank 1, L14P	I/O, VREF Bank 1, L14P_Y
I/O, L#N	1	E12	XC2S150E, 300E, 600E	-	-	I/O, L13N_Y	I/O, L14N	I/O, L14N_Y	I/O, L14N	I/O, L14N_Y
I/O	1	F12	-	-	-	-	-	I/O	I/O	I/O
I/O (DLL), L#P	1	A12	-	-	I/O (DLL), L9P	I/O (DLL), L12P	I/O (DLL), L13P	I/O (DLL), L13P	I/O (DLL), L13P	I/O (DLL), L13P
GCK2, I	1	A11	-	-	GCK2, I	GCK2, I	GCK2, I	GCK2, I	GCK2, I	GCK2, I
GCK3, I	0	C11	-	-	GCK3, I	GCK3, I	GCK3, I	GCK3, I	GCK3, I	GCK3, I
I/O (DLL), L#N	0	B11	-	-	I/O (DLL), L9N	I/O (DLL), L12N	I/O (DLL), L13N	I/O (DLL), L13N	I/O (DLL), L13N	I/O (DLL), L13N
I/O	0	D11	-	-	-	-	-	I/O	I/O	I/O

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O	0	F11	-	XC2S400E, 600E	-	-	I/O	I/O	I/O, VREF Bank 0	I/O, VREF Bank 0
I/O, L#P	0	A10	XC2S300E, 600E	-	I/O	I/O, L11P	I/O, L12P	I/O, L12P_Y	I/O, L12P	I/O,L12P_Y
I/O, L#N	0	B10	XC2S300E, 600E	-	-	I/O, L11N	I/O, L12N	I/O, L12N_Y	I/O, L12N	I/O, L12N_Y
I/O	0	E11	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P	0	C10	XC2S200E, 300E, 400E, 600E	-	I/O, L8P	I/O, L10P	I/O, L11P_Y	I/O, L11P_Y	I/O,L11P_Y	I/O,L11P_Y
I/O, VREF Bank 0, L#N	0	D10	XC2S200E, 300E, 400E, 600E	All	I/O, VREF Bank 0, L8N	I/O, VREF Bank 0, L10N	I/O, VREF Bank 0, L11N_Y	I/O, VREF Bank 0, L11N_Y	I/O, VREF Bank 0, L11N_Y	I/O, VREF Bank 0, L11N_Y
I/O	0	F10	-	-	I/O, L7P	I/O	I/O	I/O	I/O	I/O
I/O, L#P	0	A9	-	-	I/O, L7N	I/O	I/O, L10P	I/O, L10P	I/O, L10P	I/O, L10P
I/O, L#N	0	B9	-	-	-	-	I/O, L10N	I/O, L10N	I/O, L10N	I/O, L10N
I/O	0	E10	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#P	0	C9	XC2S100E, 150E, 200E	-	I/O, L6P_Y	I/O, L9P_Y	I/O, L9P_Y	I/O, L9P	I/O, L9P	I/O, L9P
I/O, L#N	0	D9	XC2S100E, 150E, 200E	-	I/O, L6N_Y	I/O, L9N_Y	I/O, L9N_Y	I/O, L9N	I/O, L9N	I/O, L9N
I/O, L#P	0	F9	XC2S150E, 200E	-	-	I/O, L8P_Y	I/O, L8P_Y	I/O, L8P	I/O, L8P	I/O, L8P
I/O, L#N	0	E9	XC2S150E, 200E	-	-	I/O, L8N_Y	I/O, L8N_Y	I/O, L8N	I/O, L8N	I/O, L8N
I/O, L#P	0	A8	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L5P_Y	I/O, L7P	I/O, L7P_Y	I/O, L7P_Y	I/O, L7P_Y	I/O, L7P_Y
I/O, L#N	0	B8	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L5N_Y	I/O, L7N	I/O, L7N_Y	I/O, L7N_Y	I/O, L7N_Y	I/O, L7N_Y
I/O, L#P	0	C8	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L4P_Y	I/O, L6P	I/O, L6P_Y	I/O, L6P_Y	I/O, L6P_Y	I/O, L6P_Y
I/O, VREF Bank 0, L#N	0	D8	XC2S100E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 0, L4N_Y	I/O, VREF Bank 0, L6N	I/O, VREF Bank 0, L6N_Y	I/O, VREF Bank 0, L6N_Y	I/O, VREF Bank 0, L6N_Y	I/O, VREF Bank 0, L6N_Y
I/O	0	A7	-	-	-	-	-	I/O	I/O	I/O
I/O	0	B7	-	-	I/O	I/O	I/O	I/O	I/O	I/O
I/O, L#P	0	C7	XC2S150E, 200E	XC2S600E	I/O, L3P	I/O, L5P_Y	I/O, L5P_Y	I/O, L5P	I/O, L5P	I/O, VREF Bank 0, L5P
I/O, L#N	0	D7	XC2S150E, 200E	-	I/O, L3N	I/O, L5N_Y	I/O, L5N_Y	I/O, L5N	I/O, L5N	I/O, L5N
I/O, L#P	0	E8	XC2S150E, 200E	-	-	I/O, L4P_Y	I/O, L4P_Y	I/O, L4P	I/O, L4P	I/O, L4P
I/O, L#N	0	E7	XC2S150E, 200E	-	-	I/O, L4N_Y	I/O, L4N_Y	I/O, L4N	I/O, L4N	I/O, L4N

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L88P_YY	3	V25	All	-	I/O, L88P_YY	I/O, L88P_YY
I/O	3	V26	-	-	I/O	I/O
I/O, VREF Bank 3, L87N_YY	3	U19	All	All	I/O, VREF Bank 3, L87N_YY	I/O, VREF Bank 3, L87N_YY
I/O (D6), L87P_YY	3	U20	All	-	I/O (D6), L87P_YY	I/O (D6), L87P_YY
I/O (D5), L86N_YY	3	U22	All	-	I/O (D5), L86N_YY	I/O (D5), L86N_YY
I/O, L86P_YY	3	U23	All	-	I/O, L86P_YY	I/O, L86P_YY
I/O	3	U24	-	-	-	I/O
I/O, L85N	3	U25	XC2S600E	-	-	I/O, L85N_Y
I/O, L85P	3	U26	XC2S600E	-	I/O	I/O, L85P_Y
I/O	3	R18	-	-	I/O	I/O
I/O, L84N	3	T19	XC2S400E	-	I/O, L84N_Y	I/O, L84N
I/O, L84P	3	T20	XC2S400E	-	I/O, L84P_Y	I/O, L84P
I/O, L83N	3	T21	XC2S600E	-	I/O, L83N	I/O, L83N_Y
I/O, L83P	3	T22	XC2S600E	-	I/O, L83P	I/O, L83P_Y
I/O	3	T24	-	-	-	I/O
I/O, L82N	3	T25	XC2S600E	-	I/O, L82N	I/O, L82N_Y
I/O, L82P	3	T26	XC2S600E	-	I/O, L82P	I/O, L82P_Y
I/O	3	R19	-	-	-	I/O
I/O, L81N	3	R20	XC2S600E	-	I/O, L81N	I/O, L81N_Y
I/O, L81P	3	R21	XC2S600E	-	I/O, L81P	I/O, L81P_Y
I/O, VREF Bank 3, L80N_YY	3	R22	All	All	I/O, VREF Bank 3, L80N_YY	I/O, VREF Bank 3, L80N_YY
I/O (D4), L80P_YY	3	R23	All	-	I/O (D4), L80P_YY	I/O (D4), L80P_YY
I/O	3	P18	-	-	-	I/O
I/O, L79N_YY	3	R25	All	-	I/O, L79N_YY	I/O, L79N_YY
I/O, L79P_YY	3	R26	All	-	I/O, L79P_YY	I/O, L79P_YY
I/O	3	P19	-	-	-	I/O
I/O, L78N	3	P20	XC2S400E	-	I/O, L78N_Y	I/O, L78N
I/O, L78P	3	P21	XC2S400E	-	I/O, L78P_Y	I/O, L78P
I/O, VREF Bank 3, L77N	3	P22	XC2S600E	All	I/O, VREF Bank 3, L77N	I/O, VREF Bank 3, L77N_Y
I/O, L77P	3	P23	XC2S600E	-	I/O, L77P	I/O, L77P_Y
I/O	3	P24	-	-	-	I/O
I/O, L76N_YY	3	P25	All	-	I/O, L76N_YY	I/O, L76N_YY
I/O, L76P_YY	3	P26	All	-	I/O, L76P_YY	I/O, L76P_YY

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L2N_YY	0	E5	All	-	I/O, L2N_YY	I/O, L2N_YY
I/O, L1P_YY	0	B4	All	-	I/O, L1P_YY	I/O, L1P_YY
I/O, L1N_YY	0	C4	All	-	I/O, L1N_YY	I/O, L1N_YY
I/O, L0P	0	A3	XC2S600E	-	I/O	I/O, L0P_Y
I/O, L0N	0	B3	XC2S600E	-	-	I/O, L0N_Y
I/O	0	A4	-	-	I/O	I/O
TCK	-	A2	-	-	TCK	TCK

FG676 Differential Clock Pins

Clock	Bank	P Input		N Input	
		Pin	Name	Pin	Name
GCK0	4	AF14	GCK0, I	AE14	I/O (DLL), L126P
GCK1	5	AF13	GCK1, I	AE13	I/O (DLL), L126N
GCK2	1	A14	GCK2, I	B14	I/O (DLL), L23P
GCK3	0	A13	GCK3, I	B13	I/O (DLL), L23N

Additional FG676 Package Pins

VCCINT Pins						
H8	H19	J9	J18	K10	K11	K16
K17	L10	L17	T10	T17	U10	U11
U16	U17	V9	V18	W8	W19	-
VCCO Bank 0 Pins						
C5	C8	D11	J10	J11	K12	K13
VCCO Bank 1 Pins						
C19	C22	D16	J16	J17	K14	K15
VCCO Bank 2 Pins						
E24	H24	K18	L18	L23	M17	N17
VCCO Bank 3 Pins						
P17	R17	T18	T23	U18	W24	AB24
VCCO Bank 4 Pins						
U14	U15	V16	V17	AC16	AD19	AD22
VCCO Bank 5 Pins						
U12	U13	V10	V11	AC11	AD5	AD8
VCCO Bank 6 Pins						
P10	R10	T4	T9	U9	W3	AB3
VCCO Bank 7 Pins						
H3	K9	L4	L9	M10	N10	E3