# AMD Xilinx - XC2S200E-6PQG208C Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

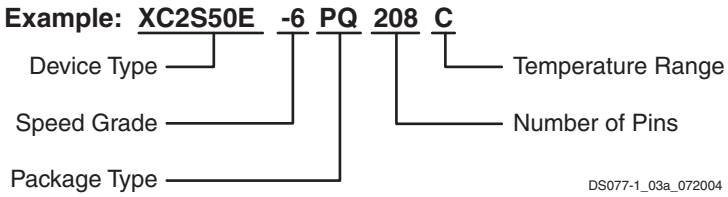
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 1176 |
| Number of Logic Elements/Cells | 5292 |
| Total RAM Bits | 57344 |
| Number of I/O | 146 |
| Number of Gates | 200000 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2s200e-6pqg208c |

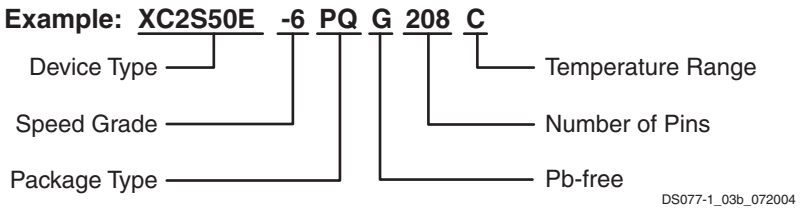
# Ordering Information

Spartan-IIE devices are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a special "G" character in the ordering code.

### *Standard Packaging*




### *Pb-Free Packaging*




## Device Ordering Options

| Device |
|---|
| XC2S50E |
| XC2S100E |
| XC2S150E |
| XC2S200E |
| XC2S300E |
| XC2S400E |
| XC2S600E |

| Speed Grade | |
|---|---|
| -6 | Standard Performance |
| -7 | Higher Performance(1) |

| Package Type / Number of Pins | |
|---|---|
| TQ(G)144 | 144-pin Plastic Thin QFP |
| PQ(G)208 | 208-pin Plastic QFP |
| FT(G)256 | 256-ball Fine Pitch BGA |
| FG(G)456 | 456-ball Fine Pitch BGA |
| FG(G)676 | 676-ball Fine Pitch BGA |

| Temperature Range ($T_J$)(2) | |
|---|---|
| C = Commercial | 0°C to +85°C |
| I = Industrial | –40°C to +100°C |

**Notes:**
1. The -7 speed grade is exclusively available in the Commercial temperature range.
2. See www.xilinx.com for information on automotive temperature range devices.

## Device Part Marking

Figure 2 is a top marking example for Spartan-IIE FPGAs in the quad-flat packages. The markings for BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator.

The "7C" and "6I" Speed Grade/Temperature Range part combinations may be dual marked as "7C/6I". Devices with the dual mark can be used as either -7C or -6I devices. Devices with a single mark are only guaranteed for the marked speed grade and temperature range.

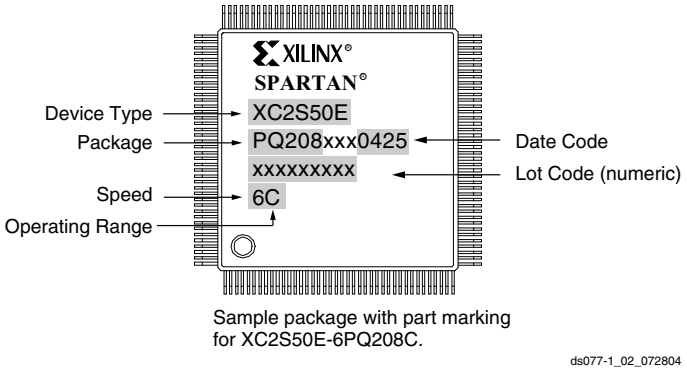



*Figure 2:* **Spartan-IIE QFP Marking Example**

Table 7 shows the depth and width aspect ratios for the block RAM.

*Table 7:* **Block RAM Port Aspect Ratios**

| Width | Depth | ADDR Bus | Data Bus |
|---|---|---|---|
| 1 | 4096 | ADDR<11:0> | DATA<0> |
| 2 | 2048 | ADDR<10:0> | DATA<1:0> |
| 4 | 1024 | ADDR<9:0> | DATA<3:0> |
| 8 | 512 | ADDR<8:0> | DATA<7:0> |
| 16 | 256 | ADDR<7:0> | DATA<15:0> |

The Spartan-IIE FPGA block RAM also includes dedicated routing to provide an efficient interface with both CLBs and other block RAMs. See Xilinx Application Note XAPP173 for more information on block RAM.

## Programmable Routing

It is the longest delay path that limits the speed of any design. Consequently, the Spartan-IIE FPGA routing architecture and its place-and-route software were defined jointly to minimize long-path delays and yield the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

The software automatically uses the best available routing based on user timing requirements. The details are provided here for reference.

### *Local Routing*

The local routing resources, as shown in Figure 9, provide the following three types of connections:

- Interconnections among the LUTs, flip-flops, and General Routing Matrix (GRM), described below.
- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM

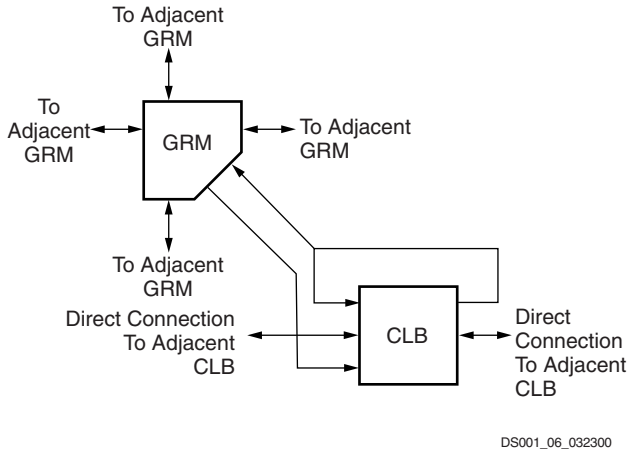



*Figure 9:* **Spartan-IIE Local Routing**

### *General Purpose Routing*

Most Spartan-IIE FPGA signals are routed on the general purpose routing, and consequently, the majority of interconnect resources are associated with this level of the routing hierarchy. The general routing resources are located in horizontal and vertical routing channels associated with the rows and columns of CLBs. The general-purpose routing resources are listed below.

- Adjacent to each CLB is a General Routing Matrix (GRM). The GRM is the switch matrix through which horizontal and vertical routing resources connect, and is also the means by which the CLB gains access to the general purpose routing.
- 24 single-length lines route GRM signals to adjacent GRMs in each of the four directions.
- 96 buffered Hex lines route GRM signals to other GRMs six blocks away in each one of the four directions. Organized in a staggered pattern, Hex lines may be driven only at their endpoints. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source). One third of the Hex lines are bidirectional, while the remaining ones are unidirectional.
- 12 Longlines are buffered, bidirectional wires that distribute signals across the device quickly and efficiently. Vertical Longlines span the full height of the device, and horizontal ones span the full width of the device.

### *I/O Routing*

Spartan-IIE devices have additional routing resources around their periphery that form an interface between the CLB array and the IOBs. This additional routing, called the VersaRing™ routing, facilitates pin-swapping and pin-locking, such that logic redesigns can adapt to existing PCB layouts. Time-to-market is reduced, since PCBs and other system components can be manufactured while the logic design is still in progress.

*Table 11:* **Configuration Modes**

| Configuration Mode | Preconfiguration Pull-ups | M0 | M1 | M2 | CCLK Direction | Data Width | Serial $D_{OUT}$ |
|---|---|---|---|---|---|---|---|
| Master Serial mode | No | 0 | 0 | 0 | Out | 1 | Yes |
| | Yes | 0 | 0 | 1 | | | |
| Slave Parallel mode (SelectMAP) | Yes | 0 | 1 | 0 | In | 8 | No |
| | No | 0 | 1 | 1 | | | |
| Boundary-Scan mode | Yes | 1 | 0 | 0 | N/A | 1 | No |
| | No | 1 | 0 | 1 | | | |
| Slave Serial mode | Yes | 1 | 1 | 0 | In | 1 | Yes |
| | No | 1 | 1 | 1 | | | |

**Notes:**
1. During power-on and throughout configuration, the I/O drivers will be in a high-impedance state. After configuration, all unused I/Os (those not assigned signals) will remain in a high-impedance state. Pins used as outputs may pulse High at the end of configuration (see Answer 10504).
2. If the Mode pins are set for preconfiguration pull-ups, those resistors go into effect once the rising edge of INIT samples the Mode pins. They will stay in effect until GTS is released during startup, after which the UnusedPin bitstream generator option will determine whether the unused I/Os have a pull-up, pull-down, or no resistor.

## Signals

There are two kinds of pins that are used to configure Spartan-IIE devices: Dedicated pins perform only specific configuration-related functions; the other pins can serve as general purpose I/Os once user operation has begun.

The dedicated pins comprise the mode pins (M2, M1, M0), the configuration clock pin (CCLK), the $\overline{\text{PROGRAM}}$ pin, the DONE pin and the boundary-scan pins (TDI, TDO, TMS, TCK). Depending on the selected configuration mode, CCLK may be an output generated by the FPGA, or may be generated externally, and provided to the FPGA as an input.

Note that some configuration pins can act as outputs. For correct operation, these pins require a $V_{CCO}$ of 3.3V to drive an LVTTL signal or 2.5V to drive an LVCMOS signal. All the relevant pins fall in banks 2 or 3. The $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$ pins for Slave Parallel mode are located in bank 1.

For a more detailed description than that given below, see ***Module 1*** and XAPP176***,*** *Configuration and Readback of the Spartan-II and Spartan-IIE FPGA Families.*

## The Process

The sequence of steps necessary to configure Spartan-IIE devices are shown in Figure 16. The overall flow can be divided into three different phases.

- Initiating configuration
- Configuration memory clear
- Loading data frames
- Start-up

The memory clearing and start-up phases are the same for all configuration modes; however, the steps for the loading of data frames are different. Thus, the details for data frame loading are described separately in the sections devoted to each mode.

### *Initiating Configuration*

There are two different ways to initiate the configuration process: applying power to the device or asserting the $\overline{\text{PROGRAM}}$ input.

Configuration on power-up occurs automatically unless it is delayed by the user, as described in a separate section below. The waveform for configuration on power-up is shown in Configuration Switching Characteristics, page 48. Before configuration can begin, $V_{CCO}$ Bank 2 must be greater than 1.0V. Furthermore, all $V_{CCINT}$ power pins must be connected to a 1.8V supply. For more information on delaying configuration, see Clearing Configuration Memory, page 23.

Once in user operation, the device can be re-configured simply by pulling the $\overline{\text{PROGRAM}}$ pin Low. The device acknowledges the beginning of the configuration process by driving DONE Low, then enters the memory-clearing phase.

During start-up, the device performs four operations:

1. The assertion of DONE. The failure of DONE to go High may indicate the unsuccessful loading of configuration data.
2. The release of the Global Three State (GTS). This activates all the I/Os to which signals are assigned. The remaining I/Os stay in a high-impedance state with internal weak pull-up resistors present.
3. The release of the Global Set Reset (GSR). This allows all flip-flops to change state.
4. The assertion of Global Write Enable (GWE). This allows all RAMs and flip-flops to change state.

By default, these operations are synchronized to CCLK. The entire start-up sequence lasts eight cycles, called C0-C7, after which the loaded design is fully functional. The four operations can be selected to switch on any CCLK cycle C1-C6 through settings in the Xilinx Development Software. The default timing for start-up is shown in the top half of Figure 17; heavy lines show default settings.

The default Start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The bottom half of Figure 17 shows another commonly used version of the start-up timing known as Sync-to-DONE. This version makes the GTS, GSR, and GWE events conditional upon the DONE pin going High. This timing is important for a daisy chain of multiple FPGAs in serial mode, since it ensures that all FPGAs go through start-up together, after all their DONE pins have gone High.

Sync-to-DONE timing is selected by setting the GTS, GSR, and GWE cycles to a value of DONE in the configuration options. This causes these signals to transition one clock cycle after DONE externally transitions High.

The sequence can also be paused at any stage until lock has been achieved on any or all DLLs.

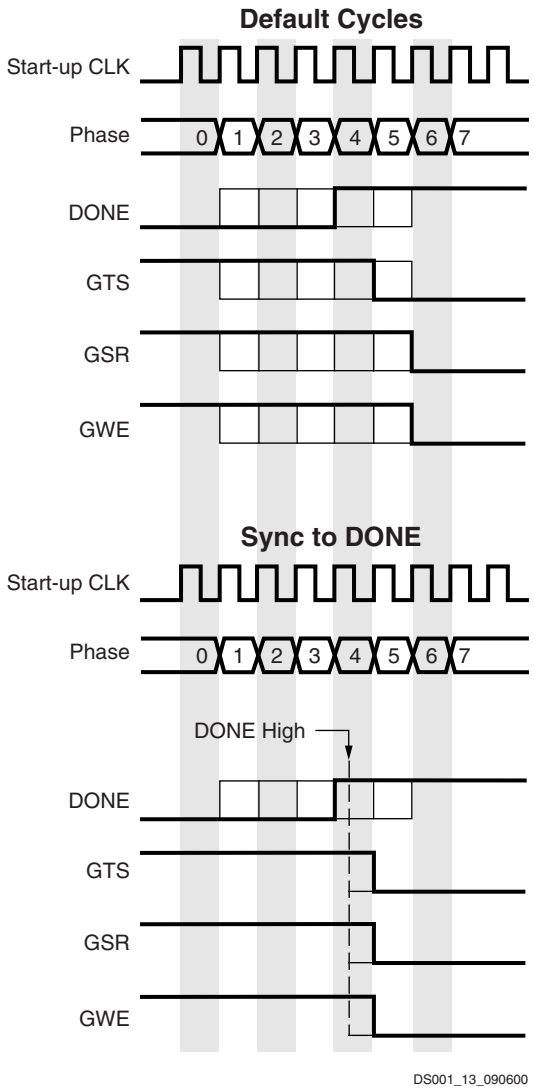



*Figure 17:* **Start-Up Waveforms**

## Serial Modes

There are two serial configuration modes. In Master Serial mode, the FPGA controls the configuration process by driving CCLK as an output. In Slave Serial mode, the FPGA passively receives CCLK as an input from an external agent (e.g., a microprocessor, CPLD, or second FPGA in master mode) that is controlling the configuration process. In both modes, the FPGA is configured by loading one bit per CCLK cycle. The MSB of each configuration data byte is always written to the DIN pin first.

See Figure 18 for the sequence for loading data into the Spartan-IIE FPGA serially. This is an expansion of the "Load Configuration Data Frames" block in Figure 16, page 23. Note that $\overline{CS}$ and $\overline{WRITE}$ are not normally used during serial configuration. To ensure successful loading of the FPGA, do not toggle $\overline{WRITE}$ with $\overline{CS}$ Low during serial configuration.

## Revision History

| Date | Version | Description |
|---|---|---|
| 11/15/2001 | 1.0 | Initial Xilinx release. |
| 11/18/2002 | 2.0 | Added XC2S400E and XC2S600E. Removed Preliminary designation. Clarified details of I/O standards, boundary scan, and configuration. |
| 07/09/2003 | 2.1 | Added hot swap description (see Hot Swap, Hot Insertion, Hot Socketing Support). Added Table 9 containing JTAG IDCODE values. Clarified configuration PROM support. |
| 06/18/2008 | 2.3 | Added note that TDI, TMS, and TCK have a default pull-up resistor. Add note on maximum daisy-chain limit. Updated Figure 19 since Mode pins can be pulled up to either 2.5V or 3.3V. Updated all modules for continuous page, figure, and table numbering. Updated links. Synchronized all modules to v2.3. |
| 08/09/2013 | 3.0 | This product is obsolete/discontinued per XCN12026. |

## Global Clock Setup and Hold for LVTTL Standard, *with* DLL (Pin-to-Pin)

| Symbol | Description | Speed Grade | | Units |
|---|---|---|---|---|
| | | -7 | -6 | |
| | | Min | Min | |
| $T_{PSDLL}$ / $T_{PHDLL}$ | Input setup and hold time relative to global clock input signal for LVTTL standard, no delay, IFF,(1) *with* DLL | 1.6 / 0 | 1.7 / 0 | ns |

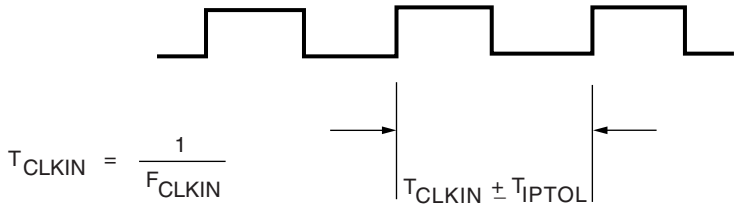
**Notes:**
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DLL output jitter is already included in the timing calculation.
4. For data input with different standards, adjust the setup time delay by the values shown in IOB Input Delay Adjustments for Different Standards, page 38. For a global clock input with standards other than LVTTL, adjust delays with values from the I/O Standard Global Clock Input Adjustments, page 42.
5. A zero hold time listing indicates no hold time or a negative hold time.

## Global Clock Setup and Hold for LVTTL Standard, *without* DLL (Pin-to-Pin)

| Symbol | Description | Device | Speed Grade | | Units |
|---|---|---|---|---|---|
| | | | -7 | -6 | |
| | | | Min | Min | |
| $T_{PSFD}$ / $T_{PHFD}$ | Input setup and hold time relative to global clock input signal for LVTTL standard, with delay, IFF,(1) *without* DLL | XC2S50E | 1.8 / 0 | 1.8 / 0 | ns |
| | | XC2S100E | 1.8 / 0 | 1.8 / 0 | ns |
| | | XC2S150E | 1.9 / 0 | 1.9 / 0 | ns |
| | | XC2S200E | 1.9 / 0 | 1.9 / 0 | ns |
| | | XC2S300E | 2.0 / 0 | 2.0 / 0 | ns |
| | | XC2S400E | 2.0 / 0 | 2.0 / 0 | ns |
| | | XC2S600E | 2.1 / 0 | 2.1 / 0 | ns |

**Notes:**
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. For data input with different standards, adjust the setup time delay by the values shown in IOB Input Delay Adjustments for Different Standards, page 38. For a global clock input with standards other than LVTTL, adjust delays with values from the I/O Standard Global Clock Input Adjustments, page 42.

***Period Tolerance:*** the allowed input clock period change in nanoseconds.




***Output Jitter:*** the difference between an ideal reference clock edge and the actual design.

***Phase Offset and Maximum Phase Difference***

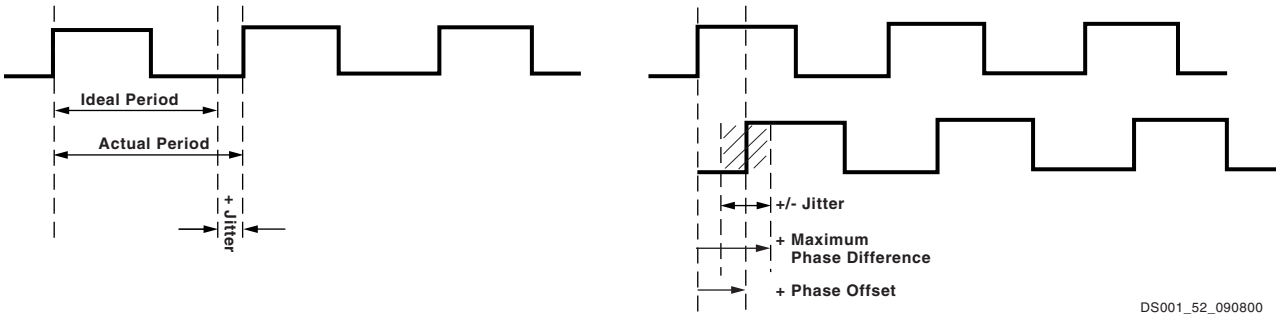



*Figure 22:* **Period Tolerance and Clock Jitter**

## CLB Distributed RAM Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -7 | | -6 | | |
| | | Min | Max | Min | Max | |
| **Sequential Delays** | | | | | | |
| $T_{SHCKO16}$ | Clock CLK to X/Y outputs (WE active, 16 x 1 mode) | 0.6 | 1.5 | 0.6 | 1.7 | ns |
| $T_{SHCKO32}$ | Clock CLK to X/Y outputs (WE active, 32 x 1 mode) | 0.8 | 1.9 | 0.8 | 2.1 | ns |
| **Setup/Hold Times with Respect to Clock CLK** | | | | | | |
| $T_{AS}$ / $T_{AH}$ | F/G address inputs | 0.42 / 0 | - | 0.5 / 0 | - | ns |
| $T_{DS}$ / $T_{DH}$ | BX/BY data inputs (DIN) | 0.53 / 0 | - | 0.6 / 0 | - | ns |
| $T_{WS}$ / $T_{WH}$ | CE input (WS) | 0.7 / 0 | - | 0.8 / 0 | - | ns |
| **Clock CLK** | | | | | | |
| $T_{WPH}$ | Pulse width, High | 2.1 | - | 2.4 | - | ns |
| $T_{WPL}$ | Pulse width, Low | 2.1 | - | 2.4 | - | ns |
| $T_{WC}$ | Clock period to meet address write cycle time | 4.2 | - | 4.8 | - | ns |

## CLB Shift Register Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -7 | | -6 | | |
| | | Min | Max | Min | Max | |
| **Sequential Delays** | | | | | | |
| $T_{REG}$ | Clock CLK to X/Y outputs | 1.2 | 2.9 | 1.2 | 3.2 | ns |
| **Setup/Hold Times with Respect to Clock CLK** | | | | | | |
| $T_{SHDICK}$ | BX/BY data inputs (DIN) | 0.53 / 0 | - | 0.6 / 0 | - | ns |
| $T_{SHCECK}$ | CE input (WS) | 0.7 / 0 | - | 0.8 / 0 | - | ns |
| **Clock CLK** | | | | | | |
| $T_{SRPH}$ | Pulse width, High | 2.1 | - | 2.4 | - | ns |
| $T_{SRPL}$ | Pulse width, Low | 2.1 | - | 2.4 | - | ns |

## Block RAM Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -7 | | -6 | | |
| | | Min | Max | Min | Max | |
| **Sequential Delays** | | | | | | |
| $T_{BCKO}$ | Clock CLK to DOUT output | 0.6 | 3.1 | 0.6 | 3.5 | ns |
| **Setup/Hold Times with Respect to Clock CLK** | | | | | | |
| $T_{BACK}$ / $T_{BCKA}$ | ADDR inputs | 1.0 / 0 | - | 1.1 / 0 | - | ns |
| $T_{BDCK}$/ $T_{BCKD}$ | DIN inputs | 1.0 / 0 | - | 1.1 / 0 | - | ns |
| $T_{BECK}$/ $T_{BCKE}$ | EN inputs | 2.2 / 0 | - | 2.5 / 0 | - | ns |
| $T_{BRCK}$/ $T_{BCKR}$ | RST input | 2.1 / 0 | - | 2.3 / 0 | - | ns |
| $T_{BWCK}$/ $T_{BCKW}$ | WEN input | 2.0 / 0 | - | 2.2 / 0 | - | ns |
| **Clock CLK** | | | | | | |
| $T_{BPWH}$ | Pulse width, High | 1.4 | - | 1.5 | - | ns |
| $T_{BPWL}$ | Pulse width, Low | 1.4 | - | 1.5 | - | ns |
| $T_{BCCS}$ | CLKA -> CLKB setup time for different ports | 2.7 | - | 3.0 | - | ns |

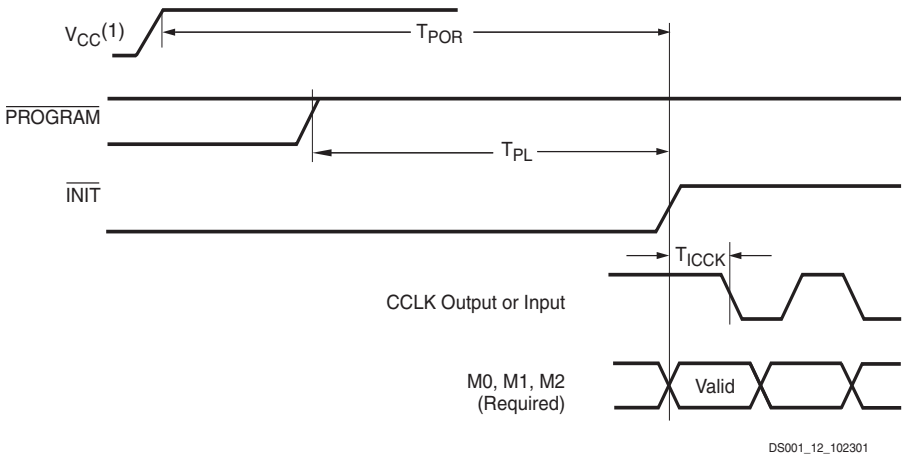
## TBUF Switching Characteristics

| Symbol | Description | Speed Grade | | Units |
|---|---|---|---|---|
| | | -7 | -6 | |
| | | Max | Max | |
| $T_{IO}$ | IN input to OUT output | 0 | 0 | ns |
| $T_{OFF}$ | TRI input to OUT output high impedance | 0.1 | 0.11 | ns |
| $T_{ON}$ | TRI input to valid data on OUT output | 0.1 | 0.11 | ns |

## JTAG Test Access Port Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -7 | | -6 | | |
| | | Min | Max | Min | Max | |
| **Setup/Hold Times with Respect to TCK** | | | | | | |
| $T_{TAPTCK}$ / $T_{TCKTAP}$ | TMS and TDI setup times and hold times | 4.0 / 2.0 | - | 4.0 / 2.0 | - | ns |
| **Sequential Delays** | | | | | | |
| $T_{TCKTDO}$ | Output delay from clock TCK to output TDO | - | 11.0 | - | 11.0 | ns |
| FTCK | TCK clock frequency | - | 33 | - | 33 | MHz |

## Configuration Switching Characteristics




| Symbol | Description | All Devices | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| $T_{POR}$ | Power-on reset | - | 2 | ms |
| $T_{PL}$ | Program latency | - | 100 | µs |
| $T_{ICCK}$ | CCLK output delay (Master serial mode only) | 0.5 | 4 | µs |
| $T_{PROGRAM}$ | Program pulse width | 300 | - | ns |

**Notes:**
1. Before configuration can begin, $V_{CCINT}$ and $V_{CCO}$ Bank 2 must reach the recommended operating voltage.

*Figure 23:* **Configuration Timing on Power-Up**

# Spartan-IIE FPGA Family: Pinout Tables

DS077-4 (v3.0) August 9, 2013

**Product Specification**

## Introduction

This section describes how the various pins on a Spartan®-IIE FPGA connect within the supported component packages, and provides device-specific thermal characteristics. Spartan-IIE FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a “G” to the middle of the package code. Except for the thermal characteristics, all information for the standard package applies equally to the Pb-free package.

## Pin Types

Most pins on a Spartan-IIE FPGA are general-purpose, user-defined I/O pins. There are, however, different functional types of pins on Spartan-IIE FPGA packages, as outlined below.

## Pin Definitions

| Pad Name | Dedicated Pin | Direction | Description |
|---|---|---|---|
| GCK0, GCK1, GCK2, GCK3 | No | Input | Clock input pins that connect to Global Clock buffers or DLL inputs. These pins become user inputs when not needed for clocks. |
| DLL | No | Input | Clock input pins that connect to DLL input or feedback clocks. Differential clock input (N input of pair) when paired with adjacent GCK input. Becomes a user I/O when not needed for clocks. |
| M0, M1, M2 | Yes | Input | Mode pins used to specify the configuration mode. |
| CCLK | Yes | Input or Output | The configuration Clock I/O pin. It is an input for Slave Parallel and Slave Serial modes, and output in Master Serial mode. After configuration, it is an input only with Don’t Care logic levels. |
| $\overline{\text{PROGRAM}}$ | Yes | Input | Initiates a configuration sequence when asserted Low. |
| DONE | Yes | Bidirectional | Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output may be open drain. |
| $\overline{\text{INIT}}$ | No | Bidirectional (Open-drain) | When Low, indicates that the configuration memory is being cleared. Goes High to indicate the end of initialization. Goes back Low to indicate a CRC error. This pin becomes a user I/O after configuration. |
| DOUT/BUSY | No | Output | In Slave Parallel mode, BUSY controls the rate at which configuration data can be loaded. It is not needed below 50 MHz. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.<br>In serial modes, DOUT provides configuration data to downstream devices in a daisy-chain. This pin becomes a user I/O after configuration. |

## PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| I/O | 2 | P134 | - | - |
| I/O (D3), L17N | 2 | P135 | XC2S50E, 300E | - |
| I/O, VREF Bank 2, L17P | 2 | P136 | XC2S50E, 300E | All |
| GND | - | P137 | - | - |
| I/O, L16N_YY | 2 | P138 | All | - |
| I/O, L16P_YY | 2 | P139 | All | - |
| I/O, L15N_YY | 2 | P140 | All | - |
| I/O (D2), L15P_YY | 2 | P141 | All | - |
| VCCINT | - | P142 | - | - |
| VCCO | - | P143 | - | - |
| GND | - | P144 | - | - |
| I/O (D1), L14N | 2 | P145 | XC2S50E, 300E | - |
| I/O, L14P | 2 | P146 | XC2S50E, 300E | XC2S100E, 150E, 200E, 300E |
| I/O | 2 | P147 | - | - |
| I/O | 2 | P148 | - | - |
| I/O | 2 | P149 | - | - |
| I/O, VREF Bank 2, L13N | 2 | P150 | XC2S100E, 150E | All |
| I/O, L13P | 2 | P151 | XC2S100E, 150E | - |
| I/O | 2 | P152 | - | XC2S200E, 300E |
| I/O (DIN, D0), L12N_YY | 2 | P153 | All | - |
| I/O (DOUT, BUSY), L12P_YY | 2 | P154 | All | - |
| CCLK | 2 | P155 | - | - |

## PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| VCCO | - | P156 | - | - |
| TDO | 2 | P157 | - | - |
| GND | - | P158 | - | - |
| TDI | - | P159 | - | - |
| | | | | |
| I/O ($\overline{CS}$), L11P_YY | 1 | P160 | All | - |
| I/O ($\overline{WRITE}$), L11N_YY | 1 | P161 | All | - |
| I/O | 1 | P162 | - | XC2S200E, 300E |
| I/O | 1 | P163 | - | - |
| I/O, VREF Bank 1, L10P_YY | 1 | P164 | All | All |
| I/O, L10N_YY | 1 | P165 | All | - |
| I/O | 1 | P166 | - | - |
| I/O | 1 | P167 | - | - |
| I/O, L9P | 1 | P168 | XC2S50E, 100E, 200E, 300E | XC2S100E, 150E, 200E, 300E |
| I/O, L9N | 1 | P169 | XC2S50E, 100E, 200E, 300E | - |
| GND | - | P170 | - | - |
| VCCO | - | P171 | - | - |
| VCCINT | - | P172 | - | - |
| I/O, L8P | 1 | P173 | XC2S50E, 100E, 200E, 300E | - |
| I/O, L8N | 1 | P174 | XC2S50E, 100E, 200E, 300E | - |
| I/O, L7P | 1 | P175 | XC2S50E, 200E, 300E | - |
| I/O, L7N | 1 | P176 | XC2S50E, 200E, 300E | - |
| GND | - | P177 | - | - |

## FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| I/O, L51P | 4 | N9 | XC2S50E, 150E, 200E, 400E | - |
| I/O, L50N | 4 | T10 | XC2S50E, 200E, 300E, 400E | - |
| I/O, VREF Bank 4, L50P | 4 | R10 | XC2S50E, 200E, 300E, 400E | All |
| I/O, L49N | 4 | P10 | XC2S50E, 200E, 300E, 400E | - |
| I/O, L49P | 4 | R11 | XC2S50E, 200E, 300E, 400E | - |
| I/O | 4 | T11 | - | - |
| I/O, L48N | 4 | N10 | XC2S50E, 100E, 200E, 300E, 400E | - |
| I/O, L48P | 4 | M10 | XC2S50E, 100E, 200E, 300E, 400E | - |
| I/O, L47N | 4 | P11 | XC2S50E, 100E, 200E, 300E, 400E | - |
| I/O, L47P | 4 | R12 | XC2S50E, 100E, 200E, 300E, 400E | XC2S100E, 150E, 200E, 300E, 400E |
| I/O, L46N | 4 | T12 | XC2S50E, 100E, 150E, 300E | - |
| I/O, L46P | 4 | T13 | XC2S50E, 100E, 150E, 300E | - |
| I/O, L45N_YY | 4 | N11 | All | - |
| I/O, VREF Bank 4, L45P_YY | 4 | M11 | All | All |
| I/O, L44N_YY | 4 | P12 | All | - |
| I/O, L44P_YY | 4 | N12 | All | - |

## FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| I/O, L43N | 4 | R13 | XC2S50E, 150E | XC2S200E, 300E, 400E |
| I/O, L43P | 4 | P13 | XC2S50E, 150E | - |
| I/O, L42N_YY | 4 | T14 | All | - |
| I/O, L42P_YY | 4 | R14 | All | - |
| | | | | |
| DONE | 3 | T15 | - | - |
| $\overline{\text{PROGRAM}}$ | - | R16 | - | - |
| I/O ($\overline{\text{INIT}}$), L41N_YY | 3 | P15 | All | - |
| I/O (D7), L41P_YY | 3 | P16 | All | - |
| I/O, L40N | 3 | N15 | XC2S100E, 150E, 400E | - |
| I/O, L40P | 3 | N16 | XC2S100E, 150E, 400E | XC2S200E, 300E, 400E |
| I/O, L39N | 3 | N14 | XC2S50E, 100E, 150E, 200E, 300E(1) | - |
| I/O, L39P | 3 | M14 | XC2S50E, 100E, 150E, 200E, 300E(1) | - |
| I/O, VREF Bank 3, L38N | 3 | M15 | XC2S50E, 150E, 200E, 300E, 400E | All |
| I/O, L38P | 3 | M16 | XC2S50E, 150E, 200E, 300E, 400E | - |
| I/O(2) | 3 | M13 | - | - |
| I/O(2) | 3 | L14 | - | - |
| I/O, L36N | 3 | L15 | XC2S50E, 300E, 400E | XC2S100E, 150E, 200E, 300E, 400E |
| I/O (D6), L36P | 3 | L16 | XC2S50E, 300E, 400E | - |

## Additional FT256 Package Pins *(Continued)*

| | | | | |
|---|---|---|---|---|
| **VCCO Bank 5 Pins** | | | | |
| L7 | L8 | M8 | - | - |
| **VCCO Bank 6 Pins** | | | | |
| J5 | J6 | K6 | - | - |
| **VCCO Bank 7 Pins** | | | | |
| G6 | H5 | H6 | - | - |
| **GND Pins** | | | | |
| A1 | A16 | B2 | B15 | F6 |
| F11 | G7 | G8 | G9 | G10 |
| H7 | H8 | H9 | H10 | J7 |
| J8 | J9 | J10 | K7 | K8 |
| K9 | K10 | L6 | L11 | R2 |
| R15 | T1 | T16 | - | - |

## FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

| Pad Name | | | LVDS Async. Output Option | $V_{REF}$ Option | Device-Specific Pinouts: XC2S | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Function | Bank | Pin | | | 100E | 150E | 200E | 300E | 400E | 600E |
| I/O, L#P_Y | 6 | R2 | XC2S300E, 400E, 600E | - | I/O, L69P | I/O, L92P | I/O, L97P | I/O, L97P_Y | I/O, L97P_Y | I/O, L97P_Y |
| I/O, VREF Bank 6, L#N_Y | 6 | R3 | XC2S300E, 400E, 600E | All | I/O, VREF Bank 6, L69N | I/O, VREF Bank 6, L92N | I/O, VREF Bank 6, L97N | I/O, VREF Bank 6, L97N_Y | I/O, VREF Bank 6, L97N_Y | I/O, VREF Bank 6, L97N_Y |
| I/O | 6 | R4 | - | - | - | - | - | I/O | I/O | I/O |
| I/O | 6 | R5 | - | - | I/O | I/O | I/O | I/O | I/O | I/O |
| I/O, L#P | 6 | T2 | XC2S200E, 400E, 600E | XC2S600E | I/O, L68P | I/O, L91P | I/O, L96P_Y | I/O, L96P | I/O, L96P_Y | I/O, VREF Bank 6, L96P_Y |
| I/O, L#N | 6 | T3 | XC2S200E, 400E, 600E | - | I/O, L68N | I/O, L91N | I/O, L96N_Y | I/O, L96N | I/O, L96N_Y | I/O, L96N_Y |
| I/O, L#P_Y | 6 | T4 | XC2S150E, 300E, 400E | - | - | I/O, L90P_Y | I/O, L95P | I/O, L95P_Y | I/O, L95P_Y | I/O, L95P |
| I/O, L#N_Y | 6 | T5 | XC2S150E, 300E, 400E | - | - | I/O, L90N_Y | I/O, L95N | I/O, L95N_Y | I/O, L95N_Y | I/O, L95N |
| I/O, L#P_Y | 6 | T1 | XC2S150E, 200E, 300E, 400E, 600E | - | I/O, L67P | I/O, L89P_Y | I/O, L94P_Y | I/O, L94P_Y | I/O, L94P_Y | I/O, L94P_Y |
| I/O, VREF Bank 6, L#N_Y | 6 | U1 | XC2S150E, 200E, 300E, 400E, 600E | All | I/O, VREF Bank 6, L67N | I/O, VREF Bank 6, L89N_Y | I/O, VREF Bank 6, L94N_Y | I/O, VREF Bank 6, L94N_Y | I/O, VREF Bank 6, L94N_Y | I/O, VREF Bank 6, L94N_Y |
| I/O | 6 | U2 | XC2S100E | - | I/O, L66P_Y | I/O | I/O | I/O | I/O | I/O |
| I/O, L#P_Y | 6 | U3 | XC2S100E, 150E, 200E, 300E, 400E, 600E | - | I/O, L66N_Y | I/O, L88P_Y | I/O, L93P_Y | I/O, L93P_Y | I/O, L93P_Y | I/O, L93P_Y |
| I/O, L#N_Y | 6 | U4 | XC2S150E, 200E, 300E, 400E, 600E | - | - | I/O, L88N_Y | I/O, L93N_Y | I/O, L93N_Y | I/O, L93N_Y | I/O, L93N_Y |
| I/O | 6 | V1 | - | - | - | - | - | I/O | I/O | I/O |
| I/O, L#P_Y | 6 | W1 | XC2S100E, 200E, 300E, 600E | - | I/O, L65P_Y | I/O, L87P | I/O, L92P_Y | I/O, L92P_Y | I/O, L92P | I/O, L92P_Y |
| I/O, L#N_Y | 6 | V2 | XC2S100E, 200E, 300E, 600E | XC2S200E, 300E, 400E, 600E | I/O, L65N_Y | I/O, L87N | I/O, VREF Bank 6, L92N_Y | I/O, VREF Bank 6, L92N_Y | I/O, VREF Bank 6, L92N | I/O, VREF Bank 6, L92N_Y |
| I/O | 6 | W2 | - | - | I/O | I/O | I/O | I/O | I/O | I/O |
| I/O, L#P_Y | 6 | V3 | XC2S200E, 300E, 400E | - | - | I/O, L86P | I/O, L91P_Y | I/O, L91P_Y | I/O, L91P_Y | I/O, L91P |
| I/O, L#N_Y | 6 | V4 | XC2S200E, 300E, 400E | - | - | I/O, L86N | I/O, L91N_Y | I/O, L91N_Y | I/O, L91N_Y | I/O, L91N |
| I/O | 6 | Y1 | - | - | - | - | - | I/O | I/O | I/O |
| I/O, L#P_YY | 6 | Y2 | All | - | I/O, L64P_YY | I/O, L85P_YY | I/O, L90P_YY | I/O, L90P_YY | I/O, L90P_YY | I/O, L90P_YY |
| I/O, L#N_YY | 6 | W3 | All | - | I/O, L64N_YY | I/O, L85N_YY | I/O, L90N_YY | I/O, L90N_YY | I/O, L90N_YY | I/O, L90N_YY |
| M1 | - | U5 | - | - | M1 | M1 | M1 | M1 | M1 | M1 |

## FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

| Pad Name | | | LVDS Async. Output Option | $V_{REF}$ Option | Device-Specific Pinouts: XC2S | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Function | Bank | Pin | | | 100E | 150E | 200E | 300E | 400E | 600E |
| I/O, L#N | 4 | AA16 | XC2S150E, 200E, 400E | XC2S600E | I/O, L46N | I/O, L62N_Y | I/O, L66N_Y | I/O, L66N | I/O, L66N_Y | I/O, VREF Bank 4, L66N |
| I/O, L#P | 4 | Y16 | XC2S150E, 200E, 400E | - | I/O, L46P | I/O, L62P_Y | I/O, L66P_Y | I/O, L66P | I/O, L66P_Y | I/O, L66P |
| I/O, L#N | 4 | W16 | XC2S150E, 200E | - | - | I/O, L61N_Y | I/O, L65N_Y | I/O, L65N | I/O, L65N | I/O, L65N |
| I/O, L#P | 4 | V16 | XC2S150E, 200E | - | - | I/O, L61P_Y | I/O, L65P_Y | I/O, L65P | I/O, L65P | I/O, L65P |
| I/O, L#N_YY | 4 | AA17 | All | - | I/O, L45N_YY | I/O, L60N_YY | I/O, L64N_YY | I/O, L64N_YY | I/O, L64N_YY | I/O, L64N_YY |
| I/O, VREF Bank 4, L#P_YY | 4 | Y17 | All | All | I/O, VREF Bank 4, L45P_YY | I/O, VREF Bank 4, L60P_YY | I/O, VREF Bank 4, L64P_YY | I/O, VREF Bank 4, L64P_YY | I/O, VREF Bank 4, L64P_YY | I/O, VREF Bank 4, L64P_YY |
| I/O | 4 | AB18 | XC2S100E | - | I/O, L44N_Y | I/O | I/O | I/O | I/O | I/O |
| I/O, L#N | 4 | W17 | XC2S100E, 400E, 600E | - | I/O, L44P_Y | I/O, L59N | I/O, L63N | I/O, L63N | I/O, L63N_Y | I/O, L63N_Y |
| I/O, L#P | 4 | V17 | XC2S400E, 600E | - | - | I/O, L59P | I/O, L63P | I/O, L63P | I/O, L63P_Y | I/O, L63P_Y |
| I/O | 4 | AA18 | - | - | - | - | - | I/O | I/O | I/O |
| I/O, L#N | 4 | Y18 | XC2S100E, 200E, 300E, 400E, 600E | - | I/O, L43N_Y | I/O, L58N | I/O, L62N_Y | I/O, L62N_Y | I/O, L62N_Y | I/O, L62N_Y |
| I/O, L#P | 4 | W18 | XC2S100E, 200E, 300E, 400E, 600E | XC2S200E, 300E, 400E, 600E | I/O, L43P_Y | I/O, L58P | I/O, VREF Bank 4, L62P_Y | I/O, VREF Bank 4, L62P_Y | I/O, VREF Bank 4, L62P_Y | I/O, VREF Bank 4, L62P_Y |
| I/O | 4 | AB19 | - | - | I/O | I/O | I/O | I/O | I/O | I/O |
| I/O, L#N | 4 | AA19 | XC2S150E, 400E | - | - | I/O, L57N_Y | I/O, L61N | I/O, L61N | I/O, L61N_Y | I/O, L61N |
| I/O, L#P | 4 | Y19 | XC2S150E, 400E | - | - | I/O, L57P_Y | I/O, L61P | I/O, L61P | I/O, L61P_Y | I/O, L61P |
| I/O | 4 | AB21 | - | - | - | - | - | I/O | I/O | I/O |
| I/O, L#N_YY | 4 | AB20 | All | - | I/O, L42N_YY | I/O, L56N_YY | I/O, L60N_YY | I/O, L60N_YY | I/O, L60N_YY | I/O, L60N_YY |
| I/O, L#P_YY | 4 | AA20 | All | - | I/O, L42P_YY | I/O, L56P_YY | I/O, L60P_YY | I/O, L60P_YY | I/O, L60P_YY | I/O, L60P_YY |
| | | | | | | | | | | |
| DONE | 3 | W20 | - | - | DONE | DONE | DONE | DONE | DONE | DONE |
| $\overline{\text{PROGRAM}}$ | - | Y21 | - | - | $\overline{\text{PROGRAM}}$ | $\overline{\text{PROGRAM}}$ | $\overline{\text{PROGRAM}}$ | $\overline{\text{PROGRAM}}$ | $\overline{\text{PROGRAM}}$ | $\overline{\text{PROGRAM}}$ |
| I/O ($\overline{\text{INIT}}$), L#N_YY | 3 | W21 | All | - | I/O ($\overline{\text{INIT}}$), L41N_YY | I/O ($\overline{\text{INIT}}$), L55N_YY | I/O ($\overline{\text{INIT}}$), L59N_YY | I/O ($\overline{\text{INIT}}$), L59N_YY | I/O ($\overline{\text{INIT}}$), L59N_YY | I/O ($\overline{\text{INIT}}$), L59N_YY |
| I/O (D7), L#P_YY | 3 | Y22 | All | - | I/O (D7), L41P_YY | I/O (D7), L55P_YY | I/O (D7), L59P_YY | I/O (D7), L59P_YY | I/O (D7), L59P_YY | I/O (D7), L59P_YY |
| I/O | 3 | W22 | - | - | - | - | - | I/O | I/O | I/O |
| I/O | 3 | V21 | - | - | - | I/O | I/O | I/O | I/O | I/O |

## FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

| Pad Name | | Pin | LVDS Async. Output Option | VREF Option | Device-Specific Pinouts | |
|---|---|---|---|---|---|---|
| Function | Bank | | | | XC2S400E | XC2S600E |
| I/O, L164N | 6 | W2 | XC2S600E | XC2S600E | I/O, L164N | I/O, VREF Bank 6, L164N_Y |
| I/O, L163P | 6 | W5 | XC2S400E | - | I/O, L163P_Y | I/O, L163P |
| I/O, L163N | 6 | W6 | XC2S400E | - | I/O, L163N_Y | I/O, L163N |
| I/O | 6 | W7 | - | - | I/O | I/O |
| I/O, L162P_YY | 6 | Y1 | All | - | I/O, L162P_YY | I/O, L162P_YY |
| I/O, L162N_YY | 6 | Y2 | All | - | I/O, L162N_YY | I/O, L162N_YY |
| I/O | 6 | Y3 | - | - | - | I/O |
| I/O, L161P_YY | 6 | Y4 | All | - | I/O, L161P_YY | I/O, L161P_YY |
| I/O, VREF Bank 6, L161N_YY | 6 | Y5 | All | All | I/O, VREF Bank 6, L161N_YY | I/O, VREF Bank 6, L161N_YY |
| I/O | 6 | Y6 | - | - | I/O | I/O |
| I/O, L160P_YY | 6 | AA1 | All | - | I/O, L160P_YY | I/O, L160P_YY |
| I/O, L160N_YY | 6 | AA2 | All | - | I/O, L160N_YY | I/O, L160N_YY |
| I/O, L159P | 6 | AA3 | XC2S600E | - | I/O, L159P | I/O, L159P_Y |
| I/O, L159N | 6 | AA4 | XC2S600E | - | I/O, L159N | I/O, L159N_Y |
| I/O | 6 | Y7 | - | - | - | I/O |
| I/O, L158P | 6 | AA5 | XC2S600E | - | I/O, L158P | I/O, L158P_Y |
| I/O, VREF Bank 6, L158N | 6 | AB5 | XC2S600E | All | I/O, VREF Bank 6, L158N | I/O, VREF Bank 6, L158N_Y |
| I/O, L157P | 6 | AB1 | XC2S400E | - | I/O, L157P_Y | I/O, L157P |
| I/O, L157N | 6 | AB2 | XC2S400E | - | I/O, L157N_Y | I/O, L157N |
| I/O, L156P | 6 | AC1 | XC2S600E | - | - | I/O, L156P_Y |
| I/O, L156N | 6 | AC2 | XC2S600E | - | I/O | I/O, L156N_Y |
| I/O, L155P_YY | 6 | AC3 | All | - | I/O, L155P_YY | I/O, L155P_YY |
| I/O, L155N_YY | 6 | AB4 | All | - | I/O, L155N_YY | I/O, L155N_YY |
| I/O, L154P | 6 | AD1 | - | - | - | I/O, L154P |
| I/O, L154N | 6 | AD2 | - | - | - | I/O, L154N |
| I/O, L153P_YY | 6 | AE1 | All | - | I/O, L153P_YY | I/O, L153P_YY |
| I/O, L153N_YY | 6 | AF2 | All | - | I/O, L153N_YY | I/O, L153N_YY |
| M1 | - | AE3 | - | - | M1 | M1 |
| M0 | - | AF3 | - | - | M0 | M0 |
| M2 | - | AD4 | - | - | M2 | M2 |

## FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

| Pad Name | | Pin | LVDS Async. Output Option | VREF Option | Device-Specific Pinouts | |
|---|---|---|---|---|---|---|
| Function | Bank | | | | XC2S400E | XC2S600E |
| I/O, L138P_YY | 5 | Y10 | All | - | I/O, L138P_YY | I/O, L138P_YY |
| I/O, L137N_YY | 5 | AB10 | All | - | I/O, L137N_YY | I/O, L137N_YY |
| I/O, L137P_YY | 5 | AC10 | All | - | I/O, L137P_YY | I/O, L137P_YY |
| I/O | 5 | AD10 | - | - | - | I/O |
| I/O, L136N | 5 | AE10 | XC2S600E | - | I/O, L136N | I/O, L136N_Y |
| I/O, L136P | 5 | AF10 | XC2S600E | - | I/O, L136P | I/O, L136P_Y |
| I/O | 5 | AD11 | - | - | - | I/O |
| I/O, L135N_YY | 5 | W11 | All | - | I/O, L135N_YY | I/O, L135N_YY |
| I/O, L135P_YY | 5 | Y11 | All | - | I/O, L135P_YY | I/O, L135P_YY |
| I/O, L134N_YY | 5 | AA11 | All | - | I/O, L134N_YY | I/O, L134N_YY |
| I/O, L134P_YY | 5 | AB11 | All | - | I/O, L134P_YY | I/O, L134P_YY |
| I/O | 5 | V12 | - | - | - | I/O |
| I/O, L133N | 5 | AE11 | - | - | I/O, L133N | I/O, L133N |
| I/O, L133P | 5 | AF11 | - | - | I/O, L133P | I/O, L133P |
| I/O | 5 | W12 | - | - | - | I/O |
| I/O, L132N_YY | 5 | Y12 | All | - | I/O, L132N_YY | I/O, L132N_YY |
| I/O, L132P_YY | 5 | AA12 | All | - | I/O, L132P_YY | I/O, L132P_YY |
| I/O, VREF Bank 5, L131N_YY | 5 | AB12 | All | All | I/O, VREF Bank 5, L131N_YY | I/O, VREF Bank 5, L131N_YY |
| I/O, L131P_YY | 5 | AC12 | All | - | I/O, L131P_YY | I/O, L131P_YY |
| I/O | 5 | V13 | - | - | - | I/O |
| I/O, L130N_YY | 5 | AE12 | All | - | I/O, L130N_YY | I/O, L130N_YY |
| I/O, L130P_YY | 5 | AF12 | All | - | I/O, L130P_YY | I/O, L130P_YY |
| I/O | 5 | W13 | - | - | - | I/O |
| I/O, L129N | 5 | Y13 | XC2S600E | - | I/O, L129N | I/O, L129N_Y |
| I/O, L129P | 5 | AA13 | XC2S600E | - | I/O, L129P | I/O, L129P_Y |
| I/O, VREF Bank 5, L128N | 5 | AB13 | XC2S600E | All | I/O, VREF Bank 5, L128N | I/O, VREF Bank 5, L128N_Y |
| I/O, L128P | 5 | AC13 | XC2S600E | - | I/O, L128P | I/O, L128P_Y |
| I/O | 5 | AD13 | - | - | - | I/O |
| I/O, L127N | 5 | V14 | - | - | I/O | I/O, L127N |
| I/O, L127P | 5 | W14 | - | - | - | I/O, L127P |
| I/O (DLL), L126N | 5 | AE13 | - | - | I/O (DLL), L126N | I/O (DLL), L126N |
| GCK1, I | 5 | AF13 | - | - | GCK1, I | GCK1, I |

## FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

| Pad Name | | Pin | LVDS Async. Output Option | VREF Option | Device-Specific Pinouts | |
|---|---|---|---|---|---|---|
| Function | Bank | | | | XC2S400E | XC2S600E |
| | | | | | | |
| DONE | 3 | AE26 | - | - | DONE | DONE |
| $\overline{\text{PROGRAM}}$ | - | AC24 | - | - | $\overline{\text{PROGRAM}}$ | $\overline{\text{PROGRAM}}$ |
| I/O ($\overline{\text{INIT}}$), L101N_YY | 3 | AD25 | All | - | I/O ($\overline{\text{INIT}}$), L101N_YY | I/O ($\overline{\text{INIT}}$), L101N_YY |
| I/O (D7), L101P_YY | 3 | AD26 | All | - | I/O (D7), L101P_YY | I/O (D7), L101P_YY |
| I/O, L100N | 3 | AC25 | - | - | - | I/O, L100N |
| I/O, L100P | 3 | AC26 | - | - | - | I/O, L100P |
| I/O, L99N | 3 | AB22 | XC2S600E | - | - | I/O, L99N_Y |
| I/O, L99P | 3 | AB23 | XC2S600E | - | I/O | I/O, L99P_Y |
| I/O, L98N_YY | 3 | AB25 | All | - | I/O, L98N_YY | I/O, L98N_YY |
| I/O, L98P_YY | 3 | AB26 | All | - | I/O, L98P_YY | I/O, L98P_YY |
| I/O, L97N | 3 | AA23 | - | - | I/O, L97N_Y | I/O, L97N |
| I/O, L97P | 3 | AA24 | - | - | I/O, L97P_Y | I/O, L97P |
| I/O, VREF Bank 3, L96N | 3 | AA25 | XC2S600E | All | I/O, VREF Bank 3, L96N | I/O, VREF Bank 3, L96N_Y |
| I/O, L96P | 3 | AA26 | XC2S600E | - | I/O, L96P | I/O, L96P_Y |
| I/O, L95N | 3 | AA22 | XC2S600E | - | - | I/O, L95N_Y |
| I/O, L95P | 3 | Y22 | XC2S600E | - | I/O | I/O, L95P_Y |
| I/O, L94N | 3 | Y23 | XC2S400E | - | I/O, L94N_Y | I/O, L94N |
| I/O, L94P | 3 | Y24 | XC2S400E | - | I/O, L94P_Y | I/O, L94P |
| I/O, L93N | 3 | Y25 | XC2S600E | - | I/O, L93N | I/O, L93N_Y |
| I/O, L93P | 3 | Y26 | XC2S600E | - | I/O, L93P | I/O, L93P_Y |
| I/O, VREF Bank 3, L92N_YY | 3 | W21 | All | All | I/O, VREF Bank 3, L92N_YY | I/O, VREF Bank 3, L92N_YY |
| I/O, L92P_YY | 3 | W22 | All | - | I/O, L92P_YY | I/O, L92P_YY |
| I/O | 3 | Y21 | - | - | - | I/O |
| I/O, L91N_YY | 3 | W25 | All | - | I/O, L91N_YY | I/O, L91N_YY |
| I/O, L91P_YY | 3 | W26 | All | - | I/O, L91P_YY | I/O, L91P_YY |
| I/O | 3 | W20 | - | - | I/O | I/O |
| I/O, L90N | 3 | V19 | XC2S400E | - | I/O, L90N_Y | I/O, L90N |
| I/O, L90P | 3 | V20 | XC2S400E | - | I/O, L90P_Y | I/O, L90P |
| I/O, L89N | 3 | V21 | XC2S600E | XC2S600E | - | I/O, VREF Bank 3, L89N_Y |
| I/O, L89P | 3 | V22 | XC2S600E | - | I/O | I/O, L89P_Y |
| I/O | 3 | V23 | - | - | I/O | I/O |
| I/O, L88N_YY | 3 | V24 | All | - | I/O, L88N_YY | I/O, L88N_YY |

## FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

| Pad Name | | Pin | LVDS Async. Output Option | VREF Option | Device-Specific Pinouts | |
|---|---|---|---|---|---|---|
| Function | Bank | | | | XC2S400E | XC2S600E |
| I/O, VREF Bank 1, L25P | 1 | D14 | XC2S600E | All | I/O, VREF Bank 1, L25P | I/O, VREF Bank 1, L25P_Y |
| I/O, L25N | 1 | C14 | XC2S600E | - | I/O, L25N | I/O, L25N_Y |
| I/O | 1 | J13 | - | - | - | I/O |
| I/O, L24P | 1 | C13 | - | - | I/O, L24P | I/O, L24P |
| I/O, L24N | 1 | D13 | - | - | I/O, L24N | I/O, L24N |
| I/O | 1 | H13 | - | - | - | I/O |
| I/O (DLL), L23P | 1 | B14 | - | - | I/O (DLL), L23P | I/O (DLL), L23P |
| GCK2, I | 1 | A14 | - | - | GCK2, I | GCK2, I |
| | | | | | | |
| GCK3, I | 0 | A13 | - | - | GCK3, I | GCK3, I |
| I/O (DLL), L23N | 0 | B13 | - | - | I/O (DLL), L23N | I/O (DLL), L23N |
| I/O | 0 | E13 | - | - | - | I/O |
| I/O, L22P_YY | 0 | F13 | All | - | I/O, L22P_YY | I/O, L22P_YY |
| I/O, L22N_YY | 0 | G13 | All | - | I/O, L22N_YY | I/O, L22N_YY |
| I/O, L21P | 0 | A12 | XC2S600E | - | - | I/O, L21P_Y |
| I/O, VREF Bank 0, L21N | 0 | B12 | XC2S600E | All | I/O, VREF Bank 0 | I/O, VREF Bank 0, L21N_Y |
| I/O, L20P | 0 | D12 | XC2S600E | - | I/O, L20P | I/O, L20P_Y |
| I/O, L20N | 0 | E12 | XC2S600E | - | I/O, L20N | I/O, L20N_Y |
| I/O | 0 | F12 | - | - | - | I/O |
| I/O, L19P_YY | 0 | G12 | All | - | I/O, L19P_YY | I/O, L19P_YY |
| I/O, L19N_YY | 0 | H12 | All | - | I/O, L19N_YY | I/O, L19N_YY |
| I/O | 0 | J12 | - | - | - | I/O |
| I/O, L18P_YY | 0 | A11 | All | - | I/O, L18P_YY | I/O, L18P_YY |
| I/O, VREF Bank 0, L18N_YY | 0 | B11 | All | All | I/O, VREF Bank 0, L18N_YY | I/O, VREF Bank 0, L18N_YY |
| I/O, L17P_YY | 0 | E11 | All | - | I/O, L17P_YY | I/O, L17P_YY |
| I/O, L17N_YY | 0 | F11 | All | - | I/O, L17N_YY | I/O, L17N_YY |
| I/O | 0 | C11 | - | - | - | I/O |
| I/O, L16P | 0 | G11 | - | - | I/O, L16P | I/O, L16P |
| I/O, L16N | 0 | H11 | - | - | I/O, L16N | I/O, L16N |
| I/O | 0 | C10 | - | - | - | I/O |
| I/O, L15P_YY | 0 | A10 | All | - | I/O, L15P_YY | I/O, L15P_YY |
| I/O, L15N_YY | 0 | B10 | All | - | I/O, L15N_YY | I/O, L15N_YY |
| I/O, L14P_YY | 0 | D10 | All | - | I/O, L14P_YY | I/O, L14P_YY |