AMD Xilinx - XC2S300E-6FTG256C Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1536
Number of Logic Elements/Cells	6912
Total RAM Bits	65536
Number of I/O	182
Number of Gates	300000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s300e-6ftg256c

Architectural Description

Spartan-IIE FPGA Array

The Spartan®-IIE user-programmable gate array, shown in Figure 3, is composed of five major configurable elements:

- IOBs provide the interface between the package pins and the internal logic
- CLBs provide the functional elements for constructing most logic
- Dedicated block RAM memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- Versatile multi-level interconnect structure

As can be seen in Figure 3, the CLBs form the central logic structure with easy access to all support and routing structures. The IOBs are located around all the logic and memory elements for easy and quick routing of signals on and off the chip.

Values stored in static memory cells control all the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

Each of these elements will be discussed in detail in the following sections.

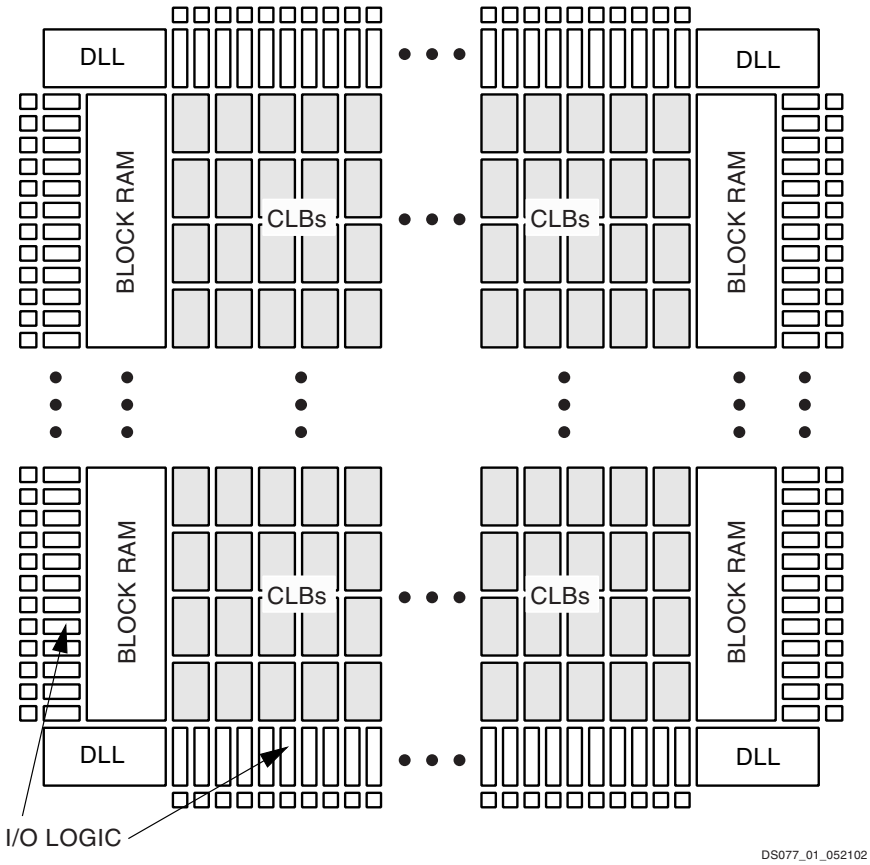

Figure 3: **Basic Spartan-IIE Family FPGA Block Diagram**

Optional pull-up and pull-down resistors and an optional weak-keeper circuit are attached to each user I/O pad. Prior to configuration all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but inputs may optionally be pulled up. The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins will float. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. After configuration, clamping diodes are connected to V_{CCO} for LVTTL, PCI, HSTL, SSTL, CTT, and AGP standards.

All Spartan-IIE FPGA IOBs support IEEE 1149.1-compatible boundary scan testing.

Input Path

A buffer in the IOB input path routes the input signal directly to internal logic and through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can used in close proximity to each other. See I/O Banking.

There are optional pull-up and pull-down resistors at each input for use after configuration.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. Each output buffer can source up to 24 mA and sink up to 48 mA. Drive strength and slew rate controls minimize bus transients. The default output driver is LVTTL with 12 mA drive strength and slow slew rate.

In most signaling standards, the output high voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See I/O Banking.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way helps eliminate bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signaling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks (see Figure 5). The pinout tables show the bank affiliation of each I/O (see Pinout Tables, page 53). Each bank has multiple V_{CCO} pins which must be connected to the same voltage. Voltage requirements are determined by the output standards in use.

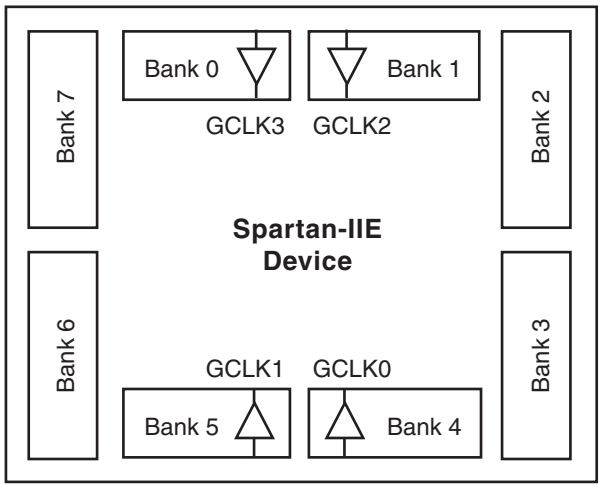

Figure 5: **Spartan-IIE I/O Banks**

In the TQ144 and PQ208 packages, the eight banks have V_{CCO} connected together. Thus, only one V_{CCO} level is allowed in these packages, although different V_{REF} values are allowed in each of the eight banks.

Within a bank, standards may be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 4. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO}. Note that V_{CCO}

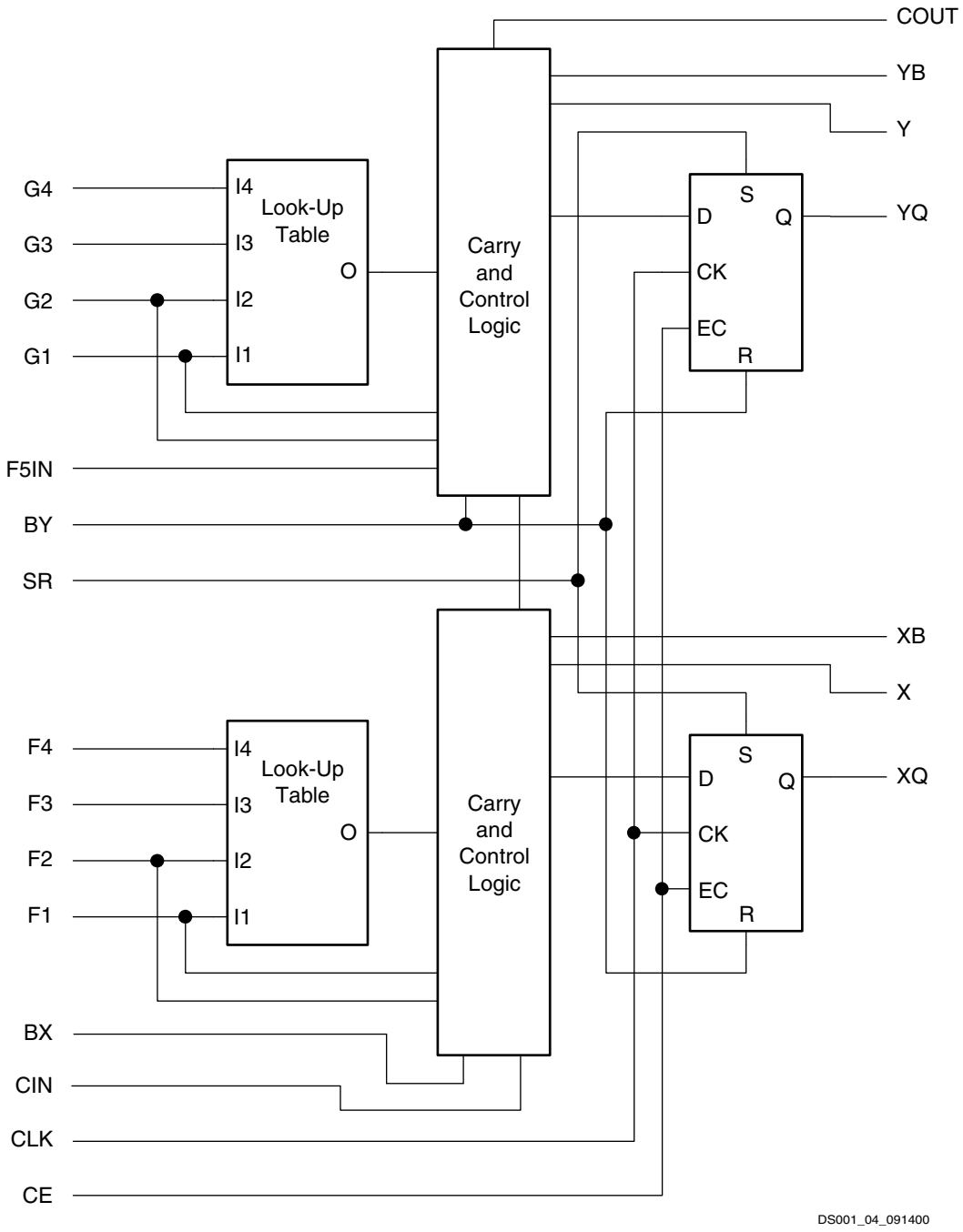

Figure 6: **Spartan-IIE CLB Slice** (two identical slices in each CLB)

Additional Logic

The F5 multiplexer in each slice combines the function generator outputs (Figure 7). This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the two F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

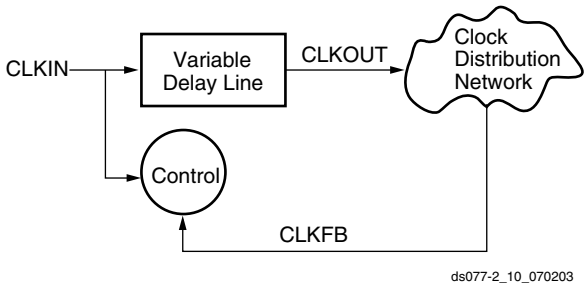

Figure 12: **Delay-Locked Loop Block Diagram**

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16. The phase-shifted output have optional duty-cycle correction (Figure 13).

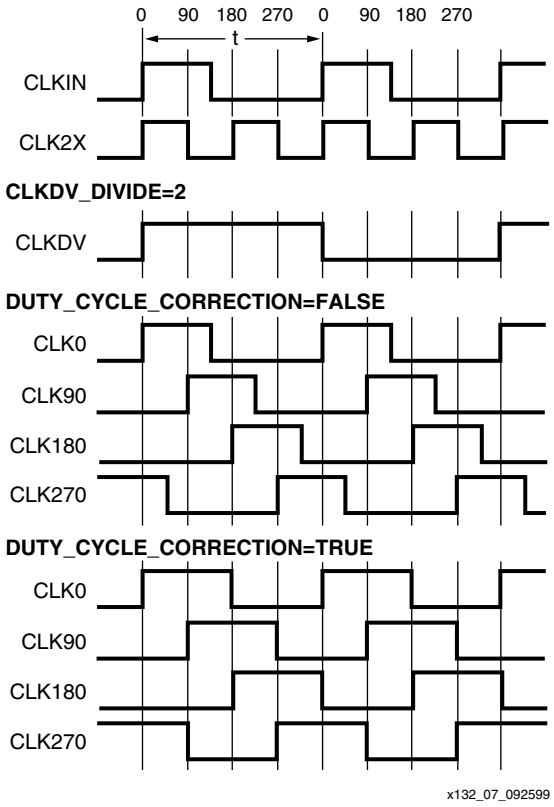

Figure 13: **DLL Output Characteristics**

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to deskew a board level clock among multiple Spartan-IIE devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock. If the DLL uses external feedback, apply a reset after startup to ensure consistent locking to the external signal. See Xilinx Application Note XAPP174 for more information on DLLs.

Boundary Scan

Spartan-IIE devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, and HIGHZ instructions. The TAP also supports two USERCODE instructions, internal scan chains, and configuration/readback of the device.

The TAP uses dedicated package pins that always operate using LVTTL. For TDO to operate using LVTTL, the V_{CCO} for Bank 2 must be 3.3V. Otherwise, TDO switches rail-to-rail between ground and V_{CCO}. The boundary-scan input pins (TDI, TMS, TCK) do not have a V_{CCO} requirement and operate with either 2.5V or 3.3V input signaling levels. TDI, TMS, and TCK hava a default internal weak pull-up resistor, and TDO has no default resistor. Bitstream options allow setting any of the four TAP pins to have an internal pull-up, pull-down, or neither.

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including unbonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections.

Table 8 lists the boundary-scan instructions supported in Spartan-IIE FPGAs. Internal signals can be captured during EXTEST by connecting them to unbonded or unused IOBs. They may also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Table 8: **Boundary-Scan Instructions**

Boundary-Scan Command	Binary Code[4:0]	Description
EXTEST	00000	Enables boundary-scan EXTEST operation
SAMPLE/ PRELOAD	00001	Enables boundary-scan SAMPLE/PRELOAD operation
USER1	00010	Access user-defined register 1
USER2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for Readback
CFG_IN	00101	Access the configuration bus for Configuration

Bit Sequence

The bit sequence within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

From a cavity-up view of the chip (as shown in the FPGA Editor), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 15.

BSDL (Boundary Scan Description Language) files for Spartan-IIE family devices are available on the Xilinx web site.

Spartan-IIE FPGA boundary scan IDCODE values are shown in Table 9.

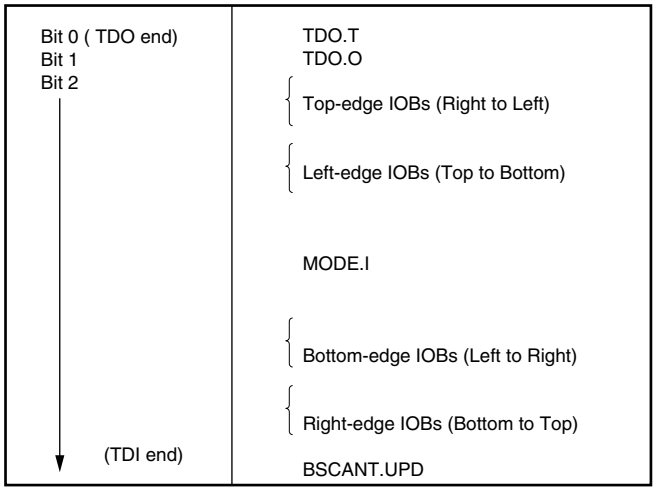

Figure 15: **Boundary Scan Bit Sequence**

Table 9: **Spartan-IIE IDCODE Values**

Device	IDCODE				
	Version	Family	Array Size	Manufacturer	Required
XC2S50E	XXXX	0000 101	0 0001 0000	0000 1001 001	1
XC2S100E	XXXX	0000 101	0 0001 0100	0000 1001 001	1
XC2S150E	XXXX	0000 101	0 0001 1000	0000 1001 001	1
XC2S200E	XXXX	0000 101	0 0001 1100	0000 1001 001	1
XC2S300E	XXXX	0000 101	0 0010 0000	0000 1001 001	1
XC2S400E	XXXX	0000 101	0 0010 1000	0000 1001 001	1
XC2S600E	XXXX	0000 101	0 0011 0000	0000 1001 001	1

Development System

Spartan-IIE FPGAs are supported by the Xilinx ISE® CAE tools. The basic methodology for Spartan-IIE FPGA design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for design entry and simulation, while Xilinx provides proprietary architecture-specific tools for implementation.

The Xilinx development system is integrated under the Xilinx Project Navigator software, providing designers with a common user interface regardless of their choice of entry and verification tools. The software simplifies the selection of implementation options with pull-down menus and on-line help.

Several advanced software features facilitate Spartan-IIE FPGA design. CORE Generator™ tool functions, for example, include macros with relative location constraints to guide their placement. They help ensure optimal implementation of common functions.

For HDL design entry, the Xilinx FPGA development system provides interfaces to several synthesis design environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Spartan-IIE FPGAs are supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The design environment supports hierarchical design entry, with high-level designs that comprise major functional blocks, while lower-level designs define the logic in these blocks. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical

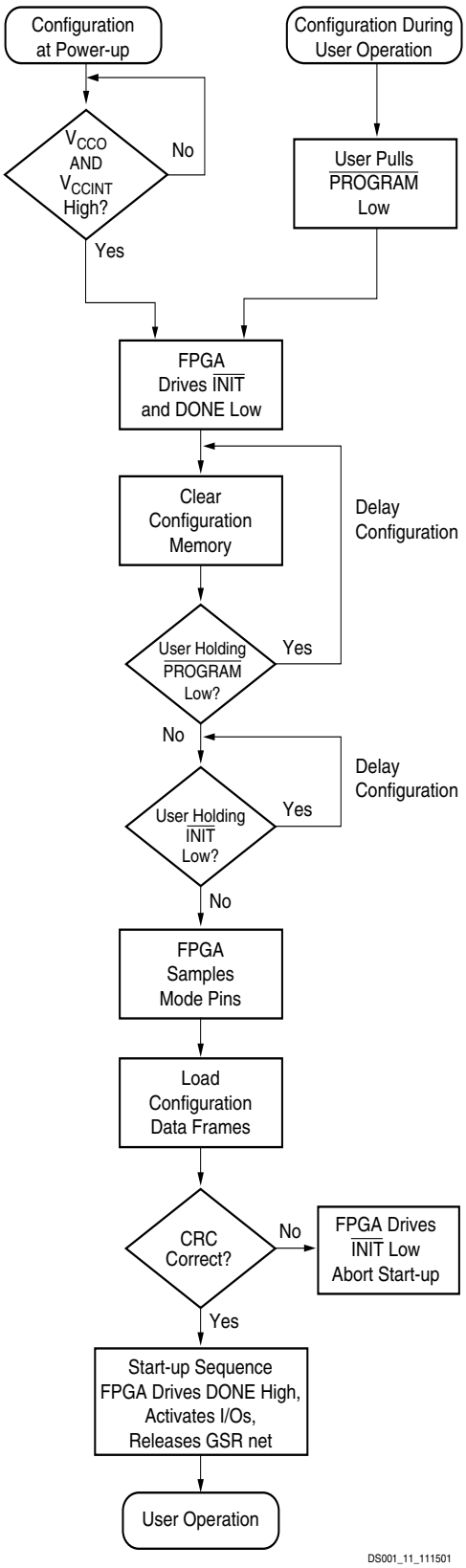

Figure 16: **Configuration Flow Diagram**

Clearing Configuration Memory

The device indicates that clearing the configuration memory is in progress by driving $\overline{\text{INIT}}$ Low.

Delaying Configuration

At this time, the user can delay configuration by holding either $\overline{\text{PROGRAM}}$ or $\overline{\text{INIT}}$ Low, which causes the device to remain in the memory clearing phase. Note that the bidirectional $\overline{\text{INIT}}$ line is driving a Low logic level during memory clearing. Thus, to avoid contention, use an open-drain driver to keep $\overline{\text{INIT}}$ Low.

With no delay in force, the device indicates that the memory is completely clear by driving $\overline{\text{INIT}}$ High. The FPGA samples its mode pins on this Low-to-High transition.

Loading Configuration Data

Once $\overline{\text{INIT}}$ is High, the user can begin loading configuration data frames into the device. The details of loading the configuration data are discussed in the sections treating the configuration modes individually. The sequence of operations necessary to load configuration data using the serial modes is shown in Figure 18. Loading data using the Slave Parallel mode is shown in Figure 21, page 28.

CRC Error Checking

After the loading of configuration data, a CRC value embedded in the configuration file is checked against a CRC value calculated within the FPGA. If the CRC values do not match, the FPGA drives $\overline{\text{INIT}}$ Low to indicate that an error has occurred and configuration is aborted. Note that attempting to load an incorrect bitstream causes configuration to fail and can damage the device.

To reconfigure the device, the $\overline{\text{PROGRAM}}$ pin should be asserted to reset the configuration logic. Recycling power also resets the FPGA for configuration. See Clearing Configuration Memory.

Start-up

The start-up sequence oversees the transition of the FPGA from the configuration state to full user operation. A match of CRC values, indicating a successful loading of the configuration data, initiates the sequence.

During start-up, the device performs four operations:

1. The assertion of DONE. The failure of DONE to go High may indicate the unsuccessful loading of configuration data.
2. The release of the Global Three State (GTS). This activates all the I/Os to which signals are assigned. The remaining I/Os stay in a high-impedance state with internal weak pull-up resistors present.
3. The release of the Global Set Reset (GSR). This allows all flip-flops to change state.
4. The assertion of Global Write Enable (GWE). This allows all RAMs and flip-flops to change state.

By default, these operations are synchronized to CCLK. The entire start-up sequence lasts eight cycles, called C0-C7, after which the loaded design is fully functional. The four operations can be selected to switch on any CCLK cycle C1-C6 through settings in the Xilinx Development Software. The default timing for start-up is shown in the top half of Figure 17; heavy lines show default settings.

The default Start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The bottom half of Figure 17 shows another commonly used version of the start-up timing known as Sync-to-DONE. This version makes the GTS, GSR, and GWE events conditional upon the DONE pin going High. This timing is important for a daisy chain of multiple FPGAs in serial mode, since it ensures that all FPGAs go through start-up together, after all their DONE pins have gone High.

Sync-to-DONE timing is selected by setting the GTS, GSR, and GWE cycles to a value of DONE in the configuration options. This causes these signals to transition one clock cycle after DONE externally transitions High.

The sequence can also be paused at any stage until lock has been achieved on any or all DLLs.

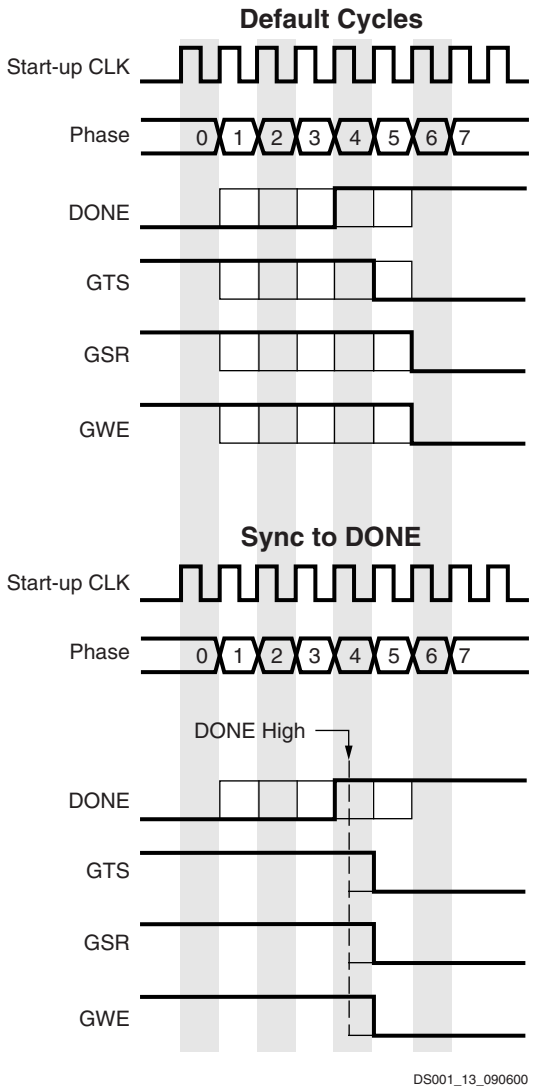

Figure 17: **Start-Up Waveforms**

Serial Modes

There are two serial configuration modes. In Master Serial mode, the FPGA controls the configuration process by driving CCLK as an output. In Slave Serial mode, the FPGA passively receives CCLK as an input from an external agent (e.g., a microprocessor, CPLD, or second FPGA in master mode) that is controlling the configuration process. In both modes, the FPGA is configured by loading one bit per CCLK cycle. The MSB of each configuration data byte is always written to the DIN pin first.

See Figure 18 for the sequence for loading data into the Spartan-IIE FPGA serially. This is an expansion of the "Load Configuration Data Frames" block in Figure 16, page 23. Note that $\overline{CS}$ and $\overline{WRITE}$ are not normally used during serial configuration. To ensure successful loading of the FPGA, do not toggle $\overline{WRITE}$ with $\overline{CS}$ Low during serial configuration.

Master Serial Mode

In Master Serial mode, the CCLK output of the FPGA drives a Xilinx PROM, which feeds a serial stream of configuration data to the FPGA's DIN input. Figure 19 shows a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-IIE device in Master Serial mode should be connected as shown for the device on the left side. Master Serial mode is selected by a <00x> on the mode pins (M0, M1, M2). The PROM RESET pin is driven by $\overline{\text{INIT}}$, and the CE input is driven by DONE. For more information on serial PROMs, see the Xilinx Configuration PROM data sheets at www.xilinx.com.

The interface is identical to the slave serial mode except that an oscillator internal to the FPGA is used to generate the configuration clock (CCLK). Any of a number of different frequencies ranging from 4 to 60 MHz can be set using the ConfigRate option in the Xilinx development software. When selecting a CCLK frequency, ensure that the serial PROM and any daisy-chained FPGAs are fast enough to support the clock rate. On power-up, while the first 60 bytes of the configuration data are being loaded, the CCLK frequency is always 2.5 MHz. This frequency is used until the ConfigRate bits, part of the configuration file, have been loaded into the FPGA, at which point the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz. The frequency of the CCLK signal created by the internal oscillator has a variance of +45%, –30% from the specified value.

The FPGA accepts one bit of configuration data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge. The timing for Master Serial mode is shown in Figure 25, page 49.

Slave Parallel Mode (SelectMAP)

The Slave Parallel mode, also known as SelectMAP, is the fastest configuration option. Byte-wide data is written into the FPGA on the D0-D7 pins. Note that D0 is the MSB of each byte for configuration. A BUSY flag is provided for controlling the flow of data at a clock frequency above 50 MHz.

Figure 20, page 27 shows the connections for two Spartan-IIE devices using the Slave Parallel mode. Slave Parallel mode is selected by a <011> on the mode pins (M0, M1, M2).

The agent controlling configuration is not shown. Typically, a processor, a microcontroller, or CPLD controls the Slave Parallel interface. The controlling agent provides byte-wide configuration data, CCLK, a Chip Select ($\overline{\text{CS}}$) signal and a Write signal ($\overline{\text{WRITE}}$). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

After configuration, the pins of the Slave Parallel port (D0-D7) can be used as additional user I/O. Alternatively, the port may be retained to permit high-speed 8-bit readback. Then data can be read by deasserting $\overline{\text{WRITE}}$. If retention is selected, prohibit the D0-D7 pins from being used as user I/O. See Readback, page 28.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
T_J	Junction temperature	Commercial	0	85	°C
		Industrial	–40	100	°C
V_{CCINT}	Supply voltage relative to GND(1)	Commercial	1.8 – 5%	1.8 + 5%	V
		Industrial	1.8 – 5%	1.8 + 5%	V
V_{CCO}	Supply voltage relative to GND(2)	Commercial	1.2	3.6	V
		Industrial	1.2	3.6	V
T_{IN}	Input signal transition time(3)		-	250	ns

Notes:
1. Functional operation is guaranteed down to a minimum V_{CCINT} of 1.62V (Nominal V_{CCINT} –10%). For every 50 mV reduction in V_{CCINT} below 1.71V (nominal V_{CCINT} –5%), all delay parameters increase by approximately 3%.
2. Minimum and maximum values for V_{CCO} vary according to the I/O standard selected.
3. Input and output measurement threshold is ~50% of V_{CCO}. See Delay Measurement Methodology, page 41 for specific details.

DC Characteristics Over Operating Conditions

Symbol	Description			Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data may be lost)			1.5	-	-	V
V_{DRIO}	Data retention V_{CCO} voltage (below which configuration data may be lost)			1.2	-	-	V
I_{CCINTQ}	Quiescent V_{CCINT} supply current(1)	XC2S50E	Commercial	-	10	200	mA
			Industrial	-	10	200	mA
		XC2S100E	Commercial	-	10	200	mA
			Industrial	-	10	200	mA
		XC2S150E	Commercial	-	10	300	mA
			Industrial	-	10	300	mA
		XC2S200E	Commercial	-	10	300	mA
			Industrial	-	10	300	mA
		XC2S300E	Commercial	-	12	300	mA
			Industrial	-	12	300	mA
		XC2S400E	Commercial	-	15	300	mA
			Industrial	-	15	300	mA
		XC2S600E	Commercial	-	15	400	mA
			Industrial	-	15	400	mA
I_{CCOQ}	Quiescent V_{CCO} supply current(1)			-	-	2	mA
I_{REF}	V_{REF} current per V_{REF} pin			-	-	20	µA
I_L	Input or output leakage current per pin			–10	-	+10	µA
C_{IN}	Input capacitance (sample tested)	TQ, PQ, FG, FT packages		-	-	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V (sample tested)(2)			-	-	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.6V (sample tested)(2)			-	-	0.25	mA

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not provide valid logic levels when input pins are connected to other circuits.

Power-On Requirements

Spartan®-IIE FPGAs require that a minimum supply current I_{CCPO} be provided to the V_{CCINT} lines for a successful power-on. If more current is available, the FPGA can consume more than I_{CCPO} min., though this cannot adversely affect reliability.

A maximum limit for I_{CCPO} is not specified. Be careful when using foldback/crowbar supplies and fuses. It is possible to control the magnitude of I_{CCPO} by limiting the supply current available to the FPGA. A current limit below the trip level will avoid inadvertently activating over-current protection circuits.

Symbol	Description				Min(1)	Typ	Max	Units
I_{CCPO}	Total V_{CCINT} supply current required during power-on	Commercial	XC2S50E - XC2S300E	After PCN(2)	300	-	-	mA
				Before PCN(2)	500	-	-	mA
			XC2S400E - XC2S600E		500	-	-	mA
		Industrial	XC2S50E - XC2S300E	After PCN(2)	500	-	-	mA
				Before PCN(2)	2	-	-	A
			XC2S400E - XC2S600E		700	-	-	mA
T_{CCPO}	V_{CCINT}(3,4) ramp time		After PCN(2)		500	-	-	µs
			Before PCN(2)		2	-	50	ms
I_{HSPO}	AC current per pin during power-on in hot-swap applications when $V_{IN} > V_{CCO} + 0.4V$; duration < 10ns		After PCN(2)		-	±60	-	µA

Notes:
1. The I_{CCPO} requirement applies for a brief time (commonly only a few milliseconds) when V_{CCINT} ramps from 0 to 1.8V.
2. Devices built after the Product Change Notice PCN 2002-05 (see http://www.xilinx.com/support/documentation/customer_notices/pcn2002-05.pdf) have improved power-on requirements. Devices after the PCN have a 'T' preceding the date code as referenced in the PCN. Note that the XC2S150E, XC2S400E, and XC2S600E always have this mark. Devices before the PCN have an 'S' preceding the date code. Note that devices before the PCN are measured with V_{CCINT} and V_{CCO} powering up simultaneously.
3. The ramp time is measured from GND to 1.8V on a fully loaded board.
4. V_{CCINT} must not dip in the negative direction during power on.
5. I/Os are not guaranteed to be disabled until V_{CCINT} is applied.
6. For more information on designing to meet the power-on specifications, refer to the application note XAPP450 "Power-On Current Requirements for the Spartan-II and Spartan-IIE Families".

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for V_{OL} and V_{OH} are guaranteed output voltages over the recommended operating conditions. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective I_{OL} and I_{OH} currents shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL(1)	–0.5	0.8	2.0	3.6	0.4	2.4	24	–24
LVCMOS2	–0.5	0.7	1.7	2.7	0.4	1.9	12	–12
LVCMOS18	–0.5	35% V_{CCO}	65% V_{CCO}	1.95	0.4	V_{CCO} – 0.4	8	–8
PCI, 3.3V	–0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note (2)	Note (2)
GTL	–0.5	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	-	40	-
GTL+	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	-	36	-

TQ144 Pinouts (XC2S50E and XC2S100E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O (DLL), L17P	4	P56	-	-
I/O	4	P57	-	-
I/O, VREF Bank 4	4	P58	-	All
I/O, L16N_YY	4	P59	All	-
I/O, L16P_YY	4	P60	All	-
VCCINT	-	P61	-	-
GND	-	P62	-	-
I/O, L15N_YY	4	P63	All	-
I/O, L15P_YY	4	P64	All	XC2S100E
I/O	4	P65	-	-
I/O, VREF Bank 4	4	P66	-	All
I/O	4	P67	-	-
I/O, L14N_YY	4	P68	All	-
I/O, L14P_YY	4	P69	All	-
GND	-	P70	-	-
DONE	3	P71	-	-
VCCO	-	P72	-	-
$\overline{\text{PROGRAM}}$	-	P73	-	-
I/O ($\overline{\text{INIT}}$), L13N_YY	3	P74	All	-
I/O (D7), L13P_YY	3	P75	All	-
I/O	3	P76	-	-
I/O, VREF Bank 3	3	P77	-	All
I/O	3	P78	-	-
I/O, L12N	3	P79	XC2S50E	XC2S100E
I/O (D6), L12P	3	P80	XC2S50E	-
GND	-	P81	-	-
I/O (D5), L11N_YY	3	P82	All	-
I/O, L11P_YY	3	P83	All	-
I/O	3	P84	-	-

TQ144 Pinouts (XC2S50E and XC2S100E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 3, L10N	3	P85	XC2S50E	All
I/O (D4), L10P	3	P86	XC2S50E	-
I/O	3	P87	-	-
VCCINT	-	P88	-	-
I/O (TRDY)	3	P89	-	-
VCCO	-	P90	-	-
GND	-	P91	-	-
I/O (IRDY)	2	P92	-	-
I/O	2	P93	-	-
I/O (D3), L9N	2	P94	XC2S50E	-
I/O, VREF Bank 2, L9P	2	P95	XC2S50E	All
I/O	2	P96	-	-
I/O, L8N_YY	2	P97	All	-
I/O (D2), L8P_YY	2	P98	All	-
GND	-	P99	-	-
I/O (D1), L7N	2	P100	XC2S50E	-
I/O, L7P	2	P101	XC2S50E	XC2S100E
I/O	2	P102	-	-
I/O, VREF Bank 2	2	P103	-	All
I/O	2	P104	-	-
I/O (DIN, D0), L6N_YY	2	P105	All	-
I/O (DOUT, BUSY), L6P_YY	2	P106	All	-
CCLK	2	P107	-	-
VCCO	-	P108	-	-
TDO	2	P109	-	-
GND	-	P110	-	-
TDI	-	P111	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 1, L6P	1	P178	XC2S50E, 200E, 300E	All
I/O, L6N	1	P179	XC2S50E, 200E, 300E	-
I/O	1	P180	-	-
I/O (DLL), L5P	1	P181	-	-
GCK2, I	1	P182	-	-
GND	-	P183	-	-
VCCO	-	P184	-	-
GCK3, I	0	P185	-	-
VCCINT	-	P186	-	-
I/O (DLL), L5N	0	P187	-	-
I/O, L4P	0	P188	XC2S50E, 200E, 300E	-
I/O, VREF Bank 0, L4N	0	P189	XC2S50E, 200E, 300E	All
GND	-	P190	-	-
I/O, L3P	0	P191	XC2S50E, 200E, 300E	-
I/O, L3N	0	P192	XC2S50E, 200E, 300E	-
I/O, L2P	0	P193	XC2S50E, 100E, 200E, 300E	-
I/O, L2N	0	P194	XC2S50E, 100E, 200E, 300E	-
VCCINT	-	P195	-	-
VCCO	-	P196	-	-
GND	-	P197	-	-
I/O, L1P	0	P198	XC2S50E, 100E, 200E, 300E	-
I/O, L1N	0	P199	XC2S50E, 100E, 200E, 300E	XC2S100E, 150E, 200E, 300E
I/O	0	P200	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O	0	P201	-	-
I/O, L0P_YY	0	P202	All	-
I/O, VREF Bank 0, L0N_YY	0	P203	All	All
I/O	0	P204	-	-
I/O	0	P205	-	XC2S200E, 300E
I/O	0	P206	-	-
TCK	-	P207	-	-
VCCO	-	P208	-	-

PQ208 Differential Clock Pins

Clock	Bank	P		N	
		Pin	Name	Pin	Name
GCK0	4	P80	GCK0, I	P81	I/O (DLL), L31P
GCK1	5	P77	GCK1, I	P75	I/O (DLL), L31N
GCK2	1	P182	GCK2, I	P181	I/O (DLL), L5P
GCK3	0	P185	GCK3, I	P187	I/O (DLL), L5N

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L65P	6	L4	XC2S50E, 150E, 200E, 300E, 400E	-
I/O, VREF Bank 6, L65N	6	L5	XC2S50E, 150E, 200E, 300E, 400E	All
I/O, L64P_YY	6	M3	All	-
I/O, L64N_YY	6	M4	All	-
I/O, L63P	6	N2	XC2S100E, 200E, 300E	-
I/O, L63N	6	N3	XC2S100E, 200E, 300E	XC2S200E, 300E, 400E
I/O, L62P_YY	6	P1	All	-
I/O, L62N_YY	6	P2	All	-
M1	-	R1	-	-
M0	-	T2	-	-
M2	-	R3	-	-
I/O, L61N_YY	5	P4	All	-
I/O, L61P_YY	5	R4	All	-
I/O, L60N	5	T3	XC2S50E, 100E, 200E, 300E, 400E	XC2S200E, 300E, 400E
I/O, L60P	5	T4	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L59N_YY	5	N5	All	-
I/O, L59P_YY	5	P5	All	-
I/O, VREF Bank 5, L58N_YY	5	R5	All	All
I/O, L58P_YY	5	T5	All	-
I/O, L57N	5	N6	XC2S50E, 100E, 150E, 300E	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L57P	5	P6	XC2S50E, 100E, 150E, 300E	-
I/O, L56N	5	R6	XC2S50E, 100E, 200E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L56P	5	T6	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L55N	5	M6	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L55P	5	N7	XC2S50E, 100E, 200E, 300E, 400E	-
I/O	5	P7	-	-
I/O, L54N	5	R7	XC2S50E, 200E, 300E, 400E	-
I/O, L54P	5	T7	XC2S50E, 200E, 300E, 400E	-
I/O, VREF Bank 5, L53N	5	M7	XC2S50E, 200E, 300E, 400E	All
I/O, L53P	5	N8	XC2S50E, 200E, 300E, 400E	-
I/O	5	P8	-	XC2S400E
I/O (DLL), L52N	5	R8	-	-
GCK1, I	5	T8	-	-
GCK0, I	4	T9	-	-
I/O (DLL), L52P	4	R9	-	-
I/O, L51N	4	P9	XC2S50E, 150E, 200E, 400E	XC2S400E

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L51P	4	N9	XC2S50E, 150E, 200E, 400E	-
I/O, L50N	4	T10	XC2S50E, 200E, 300E, 400E	-
I/O, VREF Bank 4, L50P	4	R10	XC2S50E, 200E, 300E, 400E	All
I/O, L49N	4	P10	XC2S50E, 200E, 300E, 400E	-
I/O, L49P	4	R11	XC2S50E, 200E, 300E, 400E	-
I/O	4	T11	-	-
I/O, L48N	4	N10	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L48P	4	M10	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L47N	4	P11	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L47P	4	R12	XC2S50E, 100E, 200E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L46N	4	T12	XC2S50E, 100E, 150E, 300E	-
I/O, L46P	4	T13	XC2S50E, 100E, 150E, 300E	-
I/O, L45N_YY	4	N11	All	-
I/O, VREF Bank 4, L45P_YY	4	M11	All	All
I/O, L44N_YY	4	P12	All	-
I/O, L44P_YY	4	N12	All	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L43N	4	R13	XC2S50E, 150E	XC2S200E, 300E, 400E
I/O, L43P	4	P13	XC2S50E, 150E	-
I/O, L42N_YY	4	T14	All	-
I/O, L42P_YY	4	R14	All	-
DONE	3	T15	-	-
$\overline{\text{PROGRAM}}$	-	R16	-	-
I/O ($\overline{\text{INIT}}$), L41N_YY	3	P15	All	-
I/O (D7), L41P_YY	3	P16	All	-
I/O, L40N	3	N15	XC2S100E, 150E, 400E	-
I/O, L40P	3	N16	XC2S100E, 150E, 400E	XC2S200E, 300E, 400E
I/O, L39N	3	N14	XC2S50E, 100E, 150E, 200E, 300E(1)	-
I/O, L39P	3	M14	XC2S50E, 100E, 150E, 200E, 300E(1)	-
I/O, VREF Bank 3, L38N	3	M15	XC2S50E, 150E, 200E, 300E, 400E	All
I/O, L38P	3	M16	XC2S50E, 150E, 200E, 300E, 400E	-
I/O(2)	3	M13	-	-
I/O(2)	3	L14	-	-
I/O, L36N	3	L15	XC2S50E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O (D6), L36P	3	L16	XC2S50E, 300E, 400E	-

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
M0	-	AA1	-	-	M0	M0	M0	M0	M0	M0
M2	-	AB2	-	-	M2	M2	M2	M2	M2	M2
I/O, L#N_Y	5	AA3	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L84N_Y	I/O, L89N_Y	I/O, L89N_Y	I/O, L89N_Y	I/O, L89N_Y
I/O, L#P_Y	5	AB3	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L84P_Y	I/O, L89P_Y	I/O, L89P_Y	I/O, L89P_Y	I/O, L89P_Y
I/O	5	AB4	-	-	-	-	-	I/O	I/O	I/O
I/O	5	AA5	XC2S100E, 150E	-	I/O, L63N_Y	I/O, L83N_Y	I/O	I/O	I/O	I/O
I/O, L#N_Y	5	W5	XC2S100E, 150E, 200E, 300E, 400E, 600E	-	I/O, L63P_Y	I/O, L83P_Y	I/O, L88N_Y	I/O, L88N_Y	I/O, L88N_Y	I/O, L88N_Y
I/O, L#P_Y	5	Y5	XC2S200E, 300E, 400E, 600E	-	I/O	I/O	I/O, L88P_Y	I/O, L88P_Y	I/O, L88P_Y	I/O, L88P_Y
I/O, L#N_Y	5	AB5	XC2S100E, 200E, 300E, 400E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L62N_Y	I/O, L82N	I/O, VREF Bank 5, L87N_Y	I/O, VREF Bank 5, L87N_Y	I/O, VREF Bank 5, L87N_Y	I/O, VREF Bank 5, L87N_Y
I/O, L#P_Y	5	AB6	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L62P_Y	I/O, L82P	I/O, L87P_Y	I/O, L87P_Y	I/O, L87P_Y	I/O, L87P_Y
I/O	5	Y6	-	-	-	-	-	I/O	I/O	I/O
I/O	5	AA6	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N_YY	5	V6	All	-	I/O, L61N_YY	I/O, L81N_YY	I/O, L86N_YY	I/O, L86N_YY	I/O, L86N_YY	I/O, L86N_YY
I/O, L#P_YY	5	W6	All	-	I/O, L61P_YY	I/O, L81P_YY	I/O, L86P_YY	I/O, L86P_YY	I/O, L86P_YY	I/O, L86P_YY
I/O, VREF Bank 5, L#N_YY	5	AB7	All	All	I/O, VREF Bank 5, L60N_YY	I/O, VREF Bank 5, L80N_YY	I/O, VREF Bank 5, L85N_YY	I/O, VREF Bank 5, L85N_YY	I/O, VREF Bank 5, L85N_YY	I/O, VREF Bank 5, L85N_YY
I/O, L#P_YY	5	AA7	All	-	I/O, L60P_YY	I/O, L80P_YY	I/O, L85P_YY	I/O, L85P_YY	I/O, L85P_YY	I/O, L85P_YY
I/O	5	Y7	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N_Y	5	V7	XC2S300E, 600E	-	-	I/O, L79N	I/O, L84N	I/O, L84N_Y	I/O, L84N	I/O, L84N_Y
I/O, L#P_Y	5	W7	XC2S300E, 600E	-	I/O	I/O, L79P	I/O, L84P	I/O, L84P_Y	I/O, L84P	I/O, L84P_Y
I/O, L#N_Y	5	AB8	XC2S100E, 300E, 600E	XC2S600E	I/O, L59N_Y	I/O, L78N	I/O, L83N	I/O, L83N_Y	I/O, L83N	I/O, VREF Bank 5, L83N_Y
I/O, L#P_Y	5	AA8	XC2S100E, 300E, 600E	-	I/O, L59P_Y	I/O, L78P	I/O, L83P	I/O, L83P_Y	I/O, L83P	I/O, L83P_Y
I/O	5	Y8	-	-	-	-	-	I/O	I/O	I/O

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O, L#N	3	V19	XC2S150E, 200E, 300E, 400E	-	-	I/O, L54N_Y	I/O, L58N_Y	I/O, L58N_Y	I/O, L58N_Y	I/O, L58N
I/O, L#P	3	V20	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L54P_Y	I/O, L58P_Y	I/O, L58P_Y	I/O, L58P_Y	I/O, L58P
I/O, L#N	3	V22	XC2S100E, 200E, 300E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L40N_Y	I/O, L53N	I/O, VREF Bank 3, L57N_Y	I/O, VREF Bank 3, L57N_Y	I/O, VREF Bank 3, L57N	I/O, VREF Bank 3, L57N_Y
I/O, L#P	3	U22	XC2S100E, 200E, 300E, 600E	-	I/O, L40P_Y	I/O, L53P	I/O, L57P_Y	I/O, L57P_Y	I/O, L57P	I/O, L57P_Y
I/O	3	U21	-	-	-	-	-	I/O	I/O	I/O
I/O	3	U20	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N	3	U18	XC2S100E, 200E, 300E, 600E	-	I/O, L39N_Y	I/O, L52N	I/O, L56N_Y	I/O, L56N_Y	I/O, L56N	I/O, L56N_Y
I/O, L#P	3	U19	XC2S100E, 200E, 300E, 600E	-	I/O, L39P_Y	I/O, L52P	I/O, L56P_Y	I/O, L56P_Y	I/O, L56P	I/O, L56P_Y
I/O, VREF Bank 3, L#N	3	T21	XC2S150E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 3, L38N	I/O, VREF Bank 3, L51N_Y	I/O, VREF Bank 3, L55N_Y	I/O, VREF Bank 3, L55N_Y	I/O, VREF Bank 3, L55N_Y	I/O, VREF Bank 3, L55N_Y
I/O, L#P	3	T22	XC2S150E, 200E, 300E, 400E, 600E	-	I/O, L38P	I/O, L51P_Y	I/O, L55P_Y	I/O, L55P_Y	I/O, L55P_Y	I/O, L55P_Y
I/O	3	T20	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N	3	T18	XC2S150E, 200E, 300E, 400E	-	-	I/O, L50N_Y	I/O, L54N_Y	I/O, L54N_Y	I/O, L54N_Y	I/O, L54N
I/O, L#P	3	T19	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L50P_Y	I/O, L54P_Y	I/O, L54P_Y	I/O, L54P_Y	I/O, L54P
I/O, L#N	3	R21	XC2S100E, 150E, 300E, 600E	XC2S600E	I/O, L37N_Y	I/O, L49N_Y	I/O, L53N	I/O, L53N_Y	I/O, L53N	I/O, VREF Bank 3, L53N_Y
I/O, L#P	3	R22	XC2S100E, 150E, 300E, 600E	-	I/O, L37P_Y	I/O, L49P_Y	I/O, L53P	I/O, L53P_Y	I/O, L53P	I/O, L53P_Y
I/O	3	R20	-	-	-	-	-	I/O	I/O	I/O
I/O, VREF Bank 3, L#N	3	R18	XC2S300E, 400E, 600E	All	I/O, VREF Bank 3, L36N	I/O, VREF Bank 3, L48N	I/O, VREF Bank 3, L52N	I/O, VREF Bank 3, L52N_Y	I/O, VREF Bank 3, L52N_Y	I/O, VREF Bank 3, L52N_Y
I/O (D6), L#P	3	R19	XC2S300E, 400E, 600E	-	I/O (D6), L36P	I/O (D6), L48P	I/O (D6), L52P	I/O (D6), L52P_Y	I/O (D6), L52P_Y	I/O (D6), L52P_Y
I/O (D5), L#N_YY	3	P22	All	-	I/O (D5), L35N_YY	I/O (D5), L47N_YY	I/O (D5), L51N_YY	I/O (D5), L51N_YY	I/O (D5) L51N_YY	I/O (D5), L51N_YY
I/O, L#P_YY	3	P21	All	-	I/O, L35P_YY	I/O, L47P_YY	I/O, L51P_YY	I/O, L51P_YY	I/O, L51P_YY	I/O, L51P_YY

Additional FG456 Package Pins *(Continued)*

VCCO Bank 1 Pins								
F15	F16	G13	G14	-	-	-	-	-
VCCO Bank 2 Pins								
G17	H17	J16	K16	-	-	-	-	-
VCCO Bank 3 Pins								
N16	P16	R17	T17	-	-	-	-	-
VCCO Bank 4 Pins								
T13	T14	U15	U16	-	-	-	-	-
VCCO Bank 5 Pins								
T9	T10	U7	U8	-	-	-	-	-
VCCO Bank 6 Pins								
N7	P7	R6	T6	-	-	-	-	-
VCCO Bank 7 Pins								
G6	H6	J7	K7	-	-	-	-	-
GND Pins								
A1	A2(2)	A22	B1(2)	B2	B21	C3	C20	G11
G12	J9	J10	J11	J12	J13	J14	K9	K10
K11	K12	K13	K14	L7	L9	L10	L11	L12
L13	L14	L16	M7	M9	M10	M11	M12	M13
M14	M16	N9	N10	N11	N12	N13	N14	P9
P10	P11	P12	P13	P14	T11	T12	Y20	Y3
Y4(2)	AA2	AA4(2)	AA21	AA22(2)	AB1	AB22	-	-
Not Connected Pins								
A2(2)	B1(2)	D4(1)	D19(1)	W4(1)	W19(1)	Y4(2)	AA4(2)	AA22(2)

Notes:
1. VCCINT connections in XC2S400E and XC2S600E. No Connects (no internal connection) in XC2S100E, XC2S150E, XC2S200E, and XC2S300E.
2. GND connections in XC2S400E and XC2S600E. No Connects (no internal connection) in XC2S100E, XC2S150E, XC2S200E, and XC2S300E

FG676 Pinouts (XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
TMS	-	B1	-	-	TMS	TMS
I/O	7	D3	-	-	I/O	I/O
I/O, L204P	7	C2	-	-	-	I/O, L204P
I/O, L204N	7	C1	-	-	-	I/O, L204N
I/O, L203P	7	D2	XC2S600E	-	-	I/O, L203P_Y
I/O, L203N	7	D1	XC2S600E	-	I/O	I/O, L203N_Y
I/O, L202P_YY	7	E2	All	-	I/O, L202P_YY	I/O, L202P_YY
I/O, L202N_YY	7	E1	All	-	I/O, L202N_YY	I/O, L202N_YY

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L164N	6	W2	XC2S600E	XC2S600E	I/O, L164N	I/O, VREF Bank 6, L164N_Y
I/O, L163P	6	W5	XC2S400E	-	I/O, L163P_Y	I/O, L163P
I/O, L163N	6	W6	XC2S400E	-	I/O, L163N_Y	I/O, L163N
I/O	6	W7	-	-	I/O	I/O
I/O, L162P_YY	6	Y1	All	-	I/O, L162P_YY	I/O, L162P_YY
I/O, L162N_YY	6	Y2	All	-	I/O, L162N_YY	I/O, L162N_YY
I/O	6	Y3	-	-	-	I/O
I/O, L161P_YY	6	Y4	All	-	I/O, L161P_YY	I/O, L161P_YY
I/O, VREF Bank 6, L161N_YY	6	Y5	All	All	I/O, VREF Bank 6, L161N_YY	I/O, VREF Bank 6, L161N_YY
I/O	6	Y6	-	-	I/O	I/O
I/O, L160P_YY	6	AA1	All	-	I/O, L160P_YY	I/O, L160P_YY
I/O, L160N_YY	6	AA2	All	-	I/O, L160N_YY	I/O, L160N_YY
I/O, L159P	6	AA3	XC2S600E	-	I/O, L159P	I/O, L159P_Y
I/O, L159N	6	AA4	XC2S600E	-	I/O, L159N	I/O, L159N_Y
I/O	6	Y7	-	-	-	I/O
I/O, L158P	6	AA5	XC2S600E	-	I/O, L158P	I/O, L158P_Y
I/O, VREF Bank 6, L158N	6	AB5	XC2S600E	All	I/O, VREF Bank 6, L158N	I/O, VREF Bank 6, L158N_Y
I/O, L157P	6	AB1	XC2S400E	-	I/O, L157P_Y	I/O, L157P
I/O, L157N	6	AB2	XC2S400E	-	I/O, L157N_Y	I/O, L157N
I/O, L156P	6	AC1	XC2S600E	-	-	I/O, L156P_Y
I/O, L156N	6	AC2	XC2S600E	-	I/O	I/O, L156N_Y
I/O, L155P_YY	6	AC3	All	-	I/O, L155P_YY	I/O, L155P_YY
I/O, L155N_YY	6	AB4	All	-	I/O, L155N_YY	I/O, L155N_YY
I/O, L154P	6	AD1	-	-	-	I/O, L154P
I/O, L154N	6	AD2	-	-	-	I/O, L154N
I/O, L153P_YY	6	AE1	All	-	I/O, L153P_YY	I/O, L153P_YY
I/O, L153N_YY	6	AF2	All	-	I/O, L153N_YY	I/O, L153N_YY
M1	-	AE3	-	-	M1	M1
M0	-	AF3	-	-	M0	M0
M2	-	AD4	-	-	M2	M2

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, VREF Bank 1, L25P	1	D14	XC2S600E	All	I/O, VREF Bank 1, L25P	I/O, VREF Bank 1, L25P_Y
I/O, L25N	1	C14	XC2S600E	-	I/O, L25N	I/O, L25N_Y
I/O	1	J13	-	-	-	I/O
I/O, L24P	1	C13	-	-	I/O, L24P	I/O, L24P
I/O, L24N	1	D13	-	-	I/O, L24N	I/O, L24N
I/O	1	H13	-	-	-	I/O
I/O (DLL), L23P	1	B14	-	-	I/O (DLL), L23P	I/O (DLL), L23P
GCK2, I	1	A14	-	-	GCK2, I	GCK2, I
GCK3, I	0	A13	-	-	GCK3, I	GCK3, I
I/O (DLL), L23N	0	B13	-	-	I/O (DLL), L23N	I/O (DLL), L23N
I/O	0	E13	-	-	-	I/O
I/O, L22P_YY	0	F13	All	-	I/O, L22P_YY	I/O, L22P_YY
I/O, L22N_YY	0	G13	All	-	I/O, L22N_YY	I/O, L22N_YY
I/O, L21P	0	A12	XC2S600E	-	-	I/O, L21P_Y
I/O, VREF Bank 0, L21N	0	B12	XC2S600E	All	I/O, VREF Bank 0	I/O, VREF Bank 0, L21N_Y
I/O, L20P	0	D12	XC2S600E	-	I/O, L20P	I/O, L20P_Y
I/O, L20N	0	E12	XC2S600E	-	I/O, L20N	I/O, L20N_Y
I/O	0	F12	-	-	-	I/O
I/O, L19P_YY	0	G12	All	-	I/O, L19P_YY	I/O, L19P_YY
I/O, L19N_YY	0	H12	All	-	I/O, L19N_YY	I/O, L19N_YY
I/O	0	J12	-	-	-	I/O
I/O, L18P_YY	0	A11	All	-	I/O, L18P_YY	I/O, L18P_YY
I/O, VREF Bank 0, L18N_YY	0	B11	All	All	I/O, VREF Bank 0, L18N_YY	I/O, VREF Bank 0, L18N_YY
I/O, L17P_YY	0	E11	All	-	I/O, L17P_YY	I/O, L17P_YY
I/O, L17N_YY	0	F11	All	-	I/O, L17N_YY	I/O, L17N_YY
I/O	0	C11	-	-	-	I/O
I/O, L16P	0	G11	-	-	I/O, L16P	I/O, L16P
I/O, L16N	0	H11	-	-	I/O, L16N	I/O, L16N
I/O	0	C10	-	-	-	I/O
I/O, L15P_YY	0	A10	All	-	I/O, L15P_YY	I/O, L15P_YY
I/O, L15N_YY	0	B10	All	-	I/O, L15N_YY	I/O, L15N_YY
I/O, L14P_YY	0	D10	All	-	I/O, L14P_YY	I/O, L14P_YY