# AMD Xilinx - XC2S300E-6PQ208C Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 1536 |
| Number of Logic Elements/Cells | 6912 |
| Total RAM Bits | 65536 |
| Number of I/O | 146 |
| Number of Gates | 300000 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2s300e-6pq208c |

## Revision History

| Date | Version | Description |
|---|---|---|
| 06/27/2002 | 1.1 | Updated -7 availability. |
| 11/18/2002 | 2.0 | Added XC2S400E and XC2S600E. Corrected XC2S150E max I/O count and XC2S50E differential I/O count and updated availability. |
| 07/09/2003 | 2.1 | Noted hot-swap capability. Updated Table 2 to show that all products are available. Clarified device part marking. |
| 07/28/2004 | 2.2 | Added information on Pb-free packaging options. |
| 06/18/2008 | 2.3 | Added dual mark information in Device Part Marking. Updated all modules for continuous page, figure, and table numbering. Updated links. Synchronized all modules to v2.3. |
| 08/09/2013 | 3.0 | This product is obsolete/discontinued per XCN12026. |

Table 7 shows the depth and width aspect ratios for the block RAM.

*Table 7:* **Block RAM Port Aspect Ratios**

| Width | Depth | ADDR Bus | Data Bus |
|---|---|---|---|
| 1 | 4096 | ADDR<11:0> | DATA<0> |
| 2 | 2048 | ADDR<10:0> | DATA<1:0> |
| 4 | 1024 | ADDR<9:0> | DATA<3:0> |
| 8 | 512 | ADDR<8:0> | DATA<7:0> |
| 16 | 256 | ADDR<7:0> | DATA<15:0> |

The Spartan-IIE FPGA block RAM also includes dedicated routing to provide an efficient interface with both CLBs and other block RAMs. See Xilinx Application Note XAPP173 for more information on block RAM.

## Programmable Routing

It is the longest delay path that limits the speed of any design. Consequently, the Spartan-IIE FPGA routing architecture and its place-and-route software were defined jointly to minimize long-path delays and yield the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

The software automatically uses the best available routing based on user timing requirements. The details are provided here for reference.

### *Local Routing*

The local routing resources, as shown in Figure 9, provide the following three types of connections:

- Interconnections among the LUTs, flip-flops, and General Routing Matrix (GRM), described below.
- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM

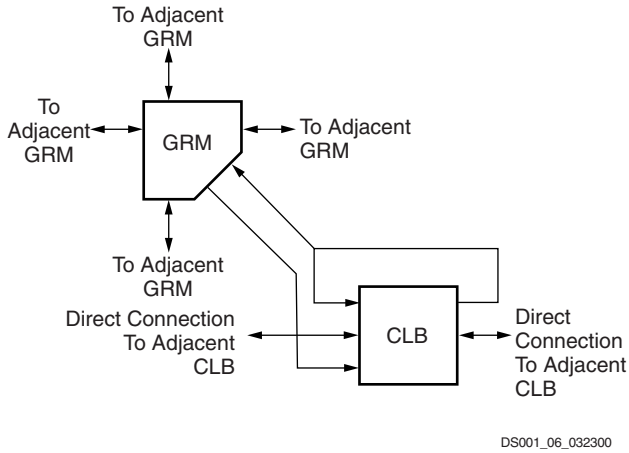



*Figure 9:* **Spartan-IIE Local Routing**

### *General Purpose Routing*

Most Spartan-IIE FPGA signals are routed on the general purpose routing, and consequently, the majority of interconnect resources are associated with this level of the routing hierarchy. The general routing resources are located in horizontal and vertical routing channels associated with the rows and columns of CLBs. The general-purpose routing resources are listed below.

- Adjacent to each CLB is a General Routing Matrix (GRM). The GRM is the switch matrix through which horizontal and vertical routing resources connect, and is also the means by which the CLB gains access to the general purpose routing.
- 24 single-length lines route GRM signals to adjacent GRMs in each of the four directions.
- 96 buffered Hex lines route GRM signals to other GRMs six blocks away in each one of the four directions. Organized in a staggered pattern, Hex lines may be driven only at their endpoints. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source). One third of the Hex lines are bidirectional, while the remaining ones are unidirectional.
- 12 Longlines are buffered, bidirectional wires that distribute signals across the device quickly and efficiently. Vertical Longlines span the full height of the device, and horizontal ones span the full width of the device.

### *I/O Routing*

Spartan-IIE devices have additional routing resources around their periphery that form an interface between the CLB array and the IOBs. This additional routing, called the VersaRing™ routing, facilitates pin-swapping and pin-locking, such that logic redesigns can adapt to existing PCB layouts. Time-to-market is reduced, since PCBs and other system components can be manufactured while the logic design is still in progress.

## Definition of Terms

In this document, some specifications may be designated as Advance or Preliminary. These designations are based on the more detailed timing information used by the development system and reported in the output files. These terms are defined as follows:

**Advance:** Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

**Preliminary:** Based on characterization. Further changes are not expected.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. All specifications are subject to change without notice.

## DC Specifications

### Absolute Maximum Ratings(1)

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage relative to GND | –0.5 | 2.0 | V |
| $V_{CCO}$ | Supply voltage relative to GND | –0.5 | 4.0 | V |
| $V_{REF}$ | Input reference voltage | –0.5 | 4.0 | V |
| $V_{IN}$ | Input voltage relative to GND(2,3) | –0.5 | 4.0 | V |
| $V_{TS}$ | Voltage applied to 3-state output(3) | –0.5 | 4.0 | V |
| $T_{STG}$ | Storage temperature (ambient) | –65 | +150 | °C |
| $T_J$ | Junction temperature | - | +125 | °C |

**Notes:**
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. $V_{IN}$ should not exceed $V_{CCO}$ by more than 3.6V over extended periods of time (e.g., longer than a day).
3. Maximum DC overshoot must be limited to either $V_{CCO}$ + 0.5V or 10 mA, and undershoot must be limited to –0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to –2.0V or overshoot to $V_{CCO}$ + 2.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
4. For soldering guidelines, see the Packaging Information on the Xilinx® website.

## Power-On Requirements

Spartan®-IIE FPGAs require that a minimum supply current $I_{CCPO}$ be provided to the $V_{CCINT}$ lines for a successful power-on. If more current is available, the FPGA can consume more than $I_{CCPO}$ min., though this cannot adversely affect reliability.

A maximum limit for $I_{CCPO}$ is not specified. Be careful when using foldback/crowbar supplies and fuses. It is possible to control the magnitude of $I_{CCPO}$ by limiting the supply current available to the FPGA. A current limit below the trip level will avoid inadvertently activating over-current protection circuits.

| Symbol | Description | | | | Min(1) | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $I_{CCPO}$ | Total $V_{CCINT}$ supply current required during power-on | Commercial | XC2S50E - XC2S300E | After PCN(2) | 300 | - | - | mA |
| | | | | Before PCN(2) | 500 | - | - | mA |
| | | | XC2S400E - XC2S600E | | 500 | - | - | mA |
| | | Industrial | XC2S50E - XC2S300E | After PCN(2) | 500 | - | - | mA |
| | | | | Before PCN(2) | 2 | - | - | A |
| | | | XC2S400E - XC2S600E | | 700 | - | - | mA |
| $T_{CCPO}$ | $V_{CCINT}$(3,4) ramp time | | After PCN(2) | | 500 | - | - | µs |
| | | | Before PCN(2) | | 2 | - | 50 | ms |
| $I_{HSPO}$ | AC current per pin during power-on in hot-swap applications when $V_{IN} > V_{CCO} + 0.4V$; duration < 10ns | | After PCN(2) | | - | ±60 | - | µA |

**Notes:**
1. The $I_{CCPO}$ requirement applies for a brief time (commonly only a few milliseconds) when $V_{CCINT}$ ramps from 0 to 1.8V.
2. Devices built after the Product Change Notice PCN 2002-05 (see http://www.xilinx.com/support/documentation/customer_notices/pcn2002-05.pdf) have improved power-on requirements. Devices after the PCN have a 'T' preceding the date code as referenced in the PCN. Note that the XC2S150E, XC2S400E, and XC2S600E always have this mark. Devices before the PCN have an 'S' preceding the date code. Note that devices before the PCN are measured with $V_{CCINT}$ and $V_{CCO}$ powering up simultaneously.
3. The ramp time is measured from GND to 1.8V on a fully loaded board.
4. $V_{CCINT}$ must not dip in the negative direction during power on.
5. I/Os are not guaranteed to be disabled until $V_{CCINT}$ is applied.
6. For more information on designing to meet the power-on specifications, refer to the application note XAPP450 "Power-On Current Requirements for the Spartan-II and Spartan-IIE Families".

## DC Input and Output Levels

Values for $V_{IL}$ and $V_{IH}$ are recommended input voltages. Values for $V_{OL}$ and $V_{OH}$ are guaranteed output voltages over the recommended operating conditions. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum $V_{CCO}$ with the respective $I_{OL}$ and $I_{OH}$ currents shown. Other standards are sample tested.

| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| LVTTL(1) | –0.5 | 0.8 | 2.0 | 3.6 | 0.4 | 2.4 | 24 | –24 |
| LVCMOS2 | –0.5 | 0.7 | 1.7 | 2.7 | 0.4 | 1.9 | 12 | –12 |
| LVCMOS18 | –0.5 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | 1.95 | 0.4 | $V_{CCO}$ – 0.4 | 8 | –8 |
| PCI, 3.3V | –0.5 | 30% $V_{CCO}$ | 50% $V_{CCO}$ | $V_{CCO}$ + 0.5 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | Note (2) | Note (2) |
| GTL | –0.5 | $V_{REF}$ – 0.05 | $V_{REF}$ + 0.05 | 3.6 | 0.4 | - | 40 | - |
| GTL+ | –0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.6 | - | 36 | - |

## IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in IOB Output Delay Adjustments for Different Standards(1), page 40.

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -7 | | -6 | | |
| | | Min | Max | Min | Max | |
| **Propagation Delays** | | | | | | |
| $T_{IOOP}$ | O input to pad | 1.0 | 2.7 | 1.0 | 2.9 | ns |
| $T_{IOOLP}$ | O input to pad via transparent latch | 1.2 | 3.1 | 1.2 | 3.4 | ns |
| **3-state Delays** | | | | | | |
| $T_{IOTHZ}$ | T input to pad high impedance(1) | 0.7 | 1.7 | 0.7 | 1.9 | ns |
| $T_{IOTON}$ | T input to valid data on pad | 1.1 | 2.9 | 1.1 | 3.1 | ns |
| $T_{IOTLPHZ}$ | T input to pad high impedance via transparent latch(1) | 0.8 | 2.0 | 0.8 | 2.2 | ns |
| $T_{IOTLPON}$ | T input to valid data on pad via transparent latch | 1.2 | 3.2 | 1.2 | 3.4 | ns |
| $T_{GTS}$ | GTS to pad high impedance(1) | 1.9 | 4.6 | 1.9 | 4.9 | ns |
| **Sequential Delays** | | | | | | |
| $T_{IOCKP}$ | Clock CLK to pad | 0.9 | 2.8 | 0.9 | 2.9 | ns |
| $T_{IOCKHZ}$ | Clock CLK to pad high impedance (synchronous)(1) | 0.7 | 2.0 | 0.7 | 2.2 | ns |
| $T_{IOCKON}$ | Clock CLK to valid data on pad (synchronous) | 1.1 | 3.2 | 1.1 | 3.4 | ns |
| **Setup/Hold Times with Respect to Clock CLK** | | | | | | |
| $T_{IOOCK}$ / $T_{IOCKO}$ | O input | 1.0 / 0 | - | 1.1 / 0 | - | ns |
| $T_{IOOCECK}$ / $T_{IOCKOCE}$ | OCE input | 0.7 / 0 | - | 0.7 / 0 | - | ns |
| $T_{IOSRCKO}$ / $T_{IOCKOSR}$ | SR input (OFF) | 0.9 / 0 | - | 1.0 / 0 | - | ns |
| $T_{IOTCK}$ / $T_{IOCKT}$ | 3-state setup times, T input | 0.6 / 0 | - | 0.7 / 0 | - | ns |
| $T_{IOTCECK}$ / $T_{IOCKTCE}$ | 3-state setup times, TCE input | 0.6 / 0 | - | 0.8 / 0 | - | ns |
| $T_{IOSRCKT}$ / $T_{IOCKTSR}$ | 3-state setup times, SR input (TFF) | 0.9 / 0 | - | 1.0 / 0 | - | ns |
| **Set/Reset Delays** | | | | | | |
| $T_{IOSRP}$ | SR input to pad (asynchronous) | 1.2 | 3.3 | 1.2 | 3.5 | ns |
| $T_{IOSRHZ}$ | SR input to pad high impedance (asynchronous)(1) | 1.0 | 2.4 | 1.0 | 2.7 | ns |
| $T_{IOSRON}$ | SR input to valid data on pad (asynchronous) | 1.4 | 3.7 | 1.4 | 3.9 | ns |
| $T_{IOGSRQ}$ | GSR to pad | 3.8 | 8.5 | 3.8 | 9.7 | ns |

**Notes:**
1. Three-state turn-off delays should not be adjusted.

## Calculation of $T_{IOOP}$ as a Function of Capacitance

$T_{IOOP}$ is the propagation delay from the O Input of the IOB to the pad. The values for $T_{IOOP}$ are based on the standard capacitive load ($C_{SL}$) for each I/O standard as listed in the table Constants for Calculating $T_{IOOP}$, below.

For other capacitive loads, use the formulas below to calculate an adjusted propagation delay, $T_{IOOP1}$.

$$T_{IOOP1} = T_{IOOP} + Adj + (C_{LOAD} - C_{SL}) * F_L$$

Where:

- Adj — is selected from IOB Output Delay Adjustments for Different Standards(1), page 40, according to the I/O standard used
- $C_{LOAD}$ — is the capacitive load for the design
- $F_L$ — is the capacitance scaling factor

## Delay Measurement Methodology

| Standard | $V_L$(1) | $V_H$(1) | Meas. Point | $V_{REF}$ Typ(2) |
|---|---|---|---|---|
| LVTTL | 0 | 3 | 1.4 | - |
| LVCMOS2 | 0 | 2.5 | 1.125 | - |
| PCI33_3 | Per PCI Spec | | | - |
| PCI66_3 | Per PCI Spec | | | - |
| GTL | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | $V_{REF}$ | 0.80 |
| GTL+ | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | $V_{REF}$ | 1.0 |
| HSTL Class I | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.75 |
| HSTL Class III | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.90 |
| HSTL Class IV | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.90 |
| SSTL3 I and II | $V_{REF}$ – 1.0 | $V_{REF}$ + 1.0 | $V_{REF}$ | 1.5 |
| SSTL2 I and II | $V_{REF}$ – 0.75 | $V_{REF}$ + 0.75 | $V_{REF}$ | 1.25 |
| CTT | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | $V_{REF}$ | 1.5 |
| AGP | $V_{REF}$ – (0.2x$V_{CCO}$) | $V_{REF}$ + (0.2x$V_{CCO}$) | $V_{REF}$ | Per AGP Spec |
| LVDS | 1.2 – 0.125 | 1.2 + 0.125 | 1.2 | |
| LVPECL | 1.6 – 0.3 | 1.6 + 0.3 | 1.6 | |

**Notes:**

1. Input waveform switches between $V_L$ and $V_H$.
2. Measurements are made at $V_{REF}$ Typ, Maximum, and Minimum. Worst-case values are reported.
3. I/O parameter measurements are made with the capacitance values shown in the following table, Constants for Calculating $T_{IOOP}$. Refer to Application Note XAPP179 for appropriate terminations.
4. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

## Constants for Calculating $T_{IOOP}$

| Standard | $C_{SL}$(1) (pF) | $F_L$ (ns/pF) |
|---|---|---|
| LVTTL Fast Slew Rate, 2 mA drive | 35 | 0.41 |
| LVTTL Fast Slew Rate, 4 mA drive | 35 | 0.20 |
| LVTTL Fast Slew Rate, 6 mA drive | 35 | 0.13 |
| LVTTL Fast Slew Rate, 8 mA drive | 35 | 0.079 |
| LVTTL Fast Slew Rate, 12 mA drive | 35 | 0.044 |
| LVTTL Fast Slew Rate, 16 mA drive | 35 | 0.043 |
| LVTTL Fast Slew Rate, 24 mA drive | 35 | 0.033 |
| LVTTL Slow Slew Rate, 2 mA drive | 35 | 0.41 |
| LVTTL Slow Slew Rate, 4 mA drive | 35 | 0.20 |
| LVTTL Slow Slew Rate, 6 mA drive | 35 | 0.100 |
| LVTTL Slow Slew Rate, 8 mA drive | 35 | 0.086 |
| LVTTL Slow Slew Rate, 12 mA drive | 35 | 0.058 |
| LVTTL Slow Slew Rate, 16 mA drive | 35 | 0.050 |
| LVTTL Slow Slew Rate, 24 mA drive | 35 | 0.048 |
| LVCMOS2 | 35 | 0.041 |
| LVCMOS18 | 35 | 0.050 |
| PCI 33 MHz 3.3V | 10 | 0.050 |
| PCI 66 MHz 3.3V | 10 | 0.033 |
| GTL | 0 | 0.014 |
| GTL+ | 0 | 0.017 |
| HSTL Class I | 20 | 0.022 |
| HSTL Class III | 20 | 0.016 |
| HSTL Class IV | 20 | 0.014 |
| SSTL2 Class I | 30 | 0.028 |
| SSTL2 Class II | 30 | 0.016 |
| SSTL3 Class I | 30 | 0.029 |
| SSTL3 Class II | 30 | 0.016 |
| CTT | 20 | 0.035 |
| AGP | 10 | 0.037 |

**Notes:**

1. I/O parameter measurements are made with the capacitance values shown above. Refer to Application Note XAPP179 for appropriate terminations.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

## DLL Timing Parameters

Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

| Symbol | Description | $F_{CLKIN}$ | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -7 | | -6 | | |
| | | | Min | Max | Min | Max | |
| $F_{CLKINHF}$ | Input clock frequency (CLKDLLHF) | - | 60 | 320 | 60 | 275 | MHz |
| $F_{CLKINLF}$ | Input clock frequency (CLKDLL) | - | 25 | 160 | 25 | 135 | MHz |
| $T_{DLLPW}$ | Input clock pulse width | ≥25 MHz | 5.0 | - | 5.0 | - | ns |
| | | ≥50 MHz | 3.0 | - | 3.0 | - | ns |
| | | ≥100 MHz | 2.4 | - | 2.4 | - | ns |
| | | ≥150 MHz | 2.0 | - | 2.0 | - | ns |
| | | ≥200 MHz | 1.8 | - | 1.8 | - | ns |
| | | ≥250 MHz | 1.5 | - | 1.5 | - | ns |
| | | ≥300 MHz | 1.3 | - | NA | - | |

## DLL Clock Tolerance, Jitter, and Phase Information

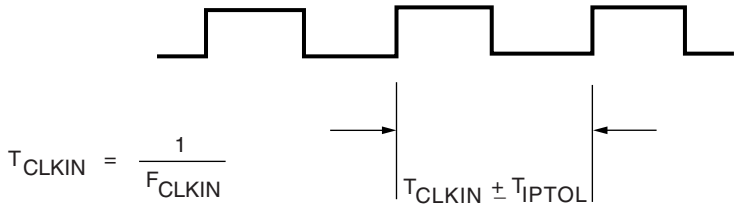
All DLL output jitter and phase specifications were determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers. Figure 22, page 44, provides definitions for various parameters in the table below.

| Symbol | Description | $F_{CLKIN}$ | CLKDLLHF | | CLKDLL | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $T_{IPTOL}$ | Input clock period tolerance | | - | 1.0 | - | 1.0 | ns |
| $T_{IJITCC}$ | Input clock jitter tolerance (cycle-to-cycle) | | - | ±150 | - | ±300 | ps |
| $T_{LOCK}$ | Time required for DLL to acquire lock(1) | > 60 MHz | - | 20 | - | 20 | µs |
| | | 50-60 MHz | - | - | - | 25 | µs |
| | | 40-50 MHz | - | - | - | 50 | µs |
| | | 30-40 MHz | - | - | - | 90 | µs |
| | | 25-30 MHz | - | - | - | 120 | µs |
| $T_{OJITCC}$ | Output jitter (cycle-to-cycle) for any DLL clock output(2) | | - | ±60 | - | ±60 | ps |
| $T_{PHIO}$ | Phase offset between CLKIN and CLKO(3) | | - | ±100 | - | ±100 | ps |
| $T_{PHOO}$ | Phase offset between clock outputs on the DLL(4) | | - | ±140 | - | ±140 | ps |
| $T_{PHIOM}$ | Phase difference between CLKIN and CLKO(5) | | - | ±160 | - | ±160 | ps |
| $T_{PHOOM}$ | Phase difference between clock outputs on the DLL(6) | | - | ±200 | - | ±200 | ps |

**Notes:**

1. Commercial operating conditions. Add 30% for Industrial operating conditions.
2. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
3. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* output jitter and input clock jitter.
4. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* output jitter and input clock jitter.
5. **Maximum Phase Difference between CLKIN and CLKO** is the sum of output jitter and phase offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
6. **Maximum Phase Difference between Clock Outputs on the DLL** is the sum of output jitter and phase offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).

***Period Tolerance:*** the allowed input clock period change in nanoseconds.




***Output Jitter:*** the difference between an ideal reference clock edge and the actual design.

***Phase Offset and Maximum Phase Difference***

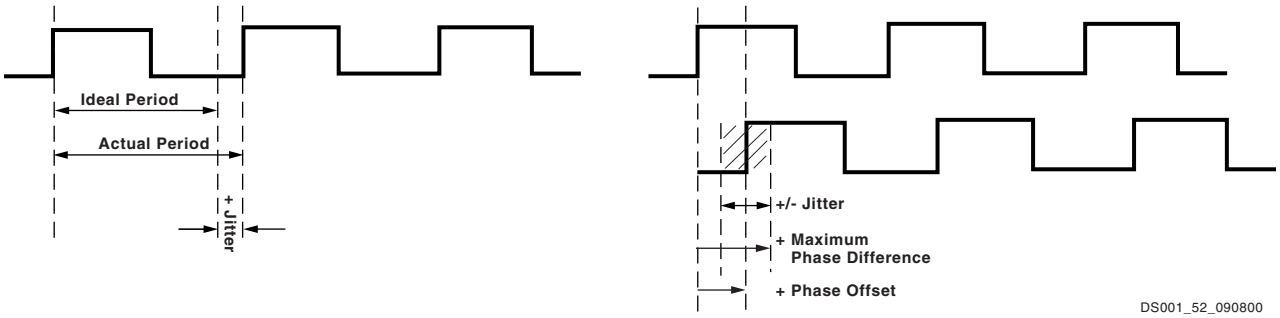



*Figure 22:* **Period Tolerance and Clock Jitter**

## Pin Definitions *(Continued)*

| Pad Name | Dedicated Pin | Direction | Description |
|---|---|---|---|
| D0/DIN, D1, D2, D3, D4, D5, D6, D7 | No | Input or Output | In Slave Parallel mode, D0-D7 are configuration data input pins. During readback, D0-D7 are output pins. These pins become user I/Os after configuration unless the Slave Parallel port is retained.<br>In serial modes, DIN is the single data input. This pin becomes a user I/O after configuration. |
| $\overline{WRITE}$ | No | Input | In Slave Parallel mode, the active-low Write Enable signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained. |
| $\overline{CS}$ | No | Input | In Slave Parallel mode, the active-low Chip Select signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained. |
| TDI, TDO, TMS, TCK | Yes | Mixed | Boundary Scan Test Access Port pins (IEEE 1149.1). |
| $V_{CCINT}$ | Yes | Input | 1.8V power supply pins for the internal core logic. |
| $V_{CCO}$ | Yes | Input | Power supply pins for output drivers (1.5V, 1.8V, 2.5V, or 3.3V subject to banking rules in the Functional Description module. |
| $V_{REF}$ | No | Input | Input threshold reference voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules in the Functional Description module. |
| GND | Yes | Input | Ground. All must be connected. |
| IRDY, TRDY | No | See PCI core documentation | These signals can only be accessed when using Xilinx PCI cores. If the cores are not used, these pins are available as user I/Os. |
| L#[P/N]<br>(e.g., L0P) | No | Bidirectional | Differential I/O with synchronous output. P = positive, N = negative. The number (#) is used to associate the two pins of a differential pair. Becomes a general user I/O when not needed for differential signals. |
| L#[P/N]_Y<br>(e.g., L0P_Y) | No | Bidirectional | Differential I/O with asynchronous or synchronous output (asynchronous output not compatible for all densities in a package). P = positive, N = negative. The number (#) is used to associate the two pins of a differential pair. Becomes a general user I/O when not needed for differential signals. |
| L#[P/N]_YY<br>(e.g., L0P_YY) | No | Bidirectional | Differential I/O with asynchronous or synchronous output (compatible for all densities in a package). P = positive, N = negative. The number (#) is used to associate the two pins of a differential pair. Becomes a general user I/O when not needed for differential signals. |
| I/O | No | Bidirectional | These pins can be configured to be input and/or output after configuration is completed. Unused I/Os are disabled with a weak pull-down resistor. After power-on and before configuration is completed, these pins are either pulled up or left floating according to the Mode pin values. See the DC and Switching Characteristics module for power-on characteristics. |

# Pinout Tables

The following device-specific pinout tables include all packages available for each Spartan-IIE device. They follow the pad locations around the die. In the TQ144 package, all VCCO pins must be connected to the same voltage.

## TQ144 Pinouts (XC2S50E and XC2S100E)

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| GND | - | P1 | - | - |
| TMS | - | P2 | - | - |
| I/O | 7 | P3 | - | - |
| I/O | 7 | P4 | - | - |
| I/O, VREF Bank 7 | 7 | P5 | - | All |
| I/O | 7 | P6 | - | - |
| I/O, L27P | 7 | P7 | XC2S50E | XC2S100E |
| I/O, L27N | 7 | P8 | XC2S50E | - |
| GND | - | P9 | - | - |
| I/O, L26P_YY | 7 | P10 | All | - |
| I/O, L26N_YY | 7 | P11 | All | - |
| I/O, VREF Bank 7, L25P | 7 | P12 | XC2S50E | All |
| I/O, L25N | 7 | P13 | XC2S50E | - |
| I/O | 7 | P14 | - | - |
| I/O (IRDY) | 7 | P15 | - | - |
| GND | - | P16 | - | - |
| VCCO | - | P17 | - | - |
| | | | | |
| I/O (TRDY) | 6 | P18 | - | - |
| VCCINT | - | P19 | - | - |
| I/O | 6 | P20 | - | - |
| I/O, L24P | 6 | P21 | XC2S50E | - |
| I/O, VREF Bank 6, L24N | 6 | P22 | XC2S50E | All |
| I/O, L23P_YY | 6 | P23 | All | - |
| I/O, L23N_YY | 6 | P24 | All | - |
| GND | - | P25 | - | - |
| I/O, L22P | 6 | P26 | XC2S50E | - |

## TQ144 Pinouts (XC2S50E and XC2S100E) *(Continued)*

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| I/O, L22N | 6 | P27 | XC2S50E | XC2S100E |
| I/O | 6 | P28 | - | - |
| I/O, VREF Bank 6 | 6 | P29 | - | All |
| I/O | 6 | P30 | - | - |
| I/O, L21P_YY | 6 | P31 | All | - |
| I/O, L21N_YY | 6 | P32 | All | - |
| M1 | - | P33 | - | - |
| GND | - | P34 | - | - |
| M0 | - | P35 | - | - |
| VCCO | - | P36 | - | - |
| M2 | - | P37 | - | - |
| | | | | |
| I/O, L20N_YY | 5 | P38 | All | - |
| I/O, L20P_YY | 5 | P39 | All | - |
| I/O | 5 | P40 | - | - |
| I/O, VREF Bank 5 | 5 | P41 | - | All |
| I/O | 5 | P42 | - | - |
| I/O, L19N_YY | 5 | P43 | All | XC2S100E |
| I/O, L19P_YY | 5 | P44 | All | - |
| GND | - | P45 | - | - |
| VCCINT | - | P46 | - | - |
| I/O, L18N_YY | 5 | P47 | All | - |
| I/O, L18P_YY | 5 | P48 | All | - |
| I/O, VREF Bank 5 | 5 | P49 | - | All |
| I/O (DLL), L17N | 5 | P50 | - | - |
| VCCINT | - | P51 | - | - |
| GCK1, I | 5 | P52 | - | - |
| VCCO | 5 | P53 | - | - |
| GND | - | P54 | - | - |
| | | | | |
| GCK0, I | 4 | P55 | - | - |

In the PQ208 package, all VCCO pins must be connected to the same voltage.

## PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| GND | - | P1 | - | - |
| TMS | - | P2 | - | - |
| I/O | 7 | P3 | - | - |
| I/O | 7 | P4 | - | XC2S200E, 300E |
| I/O | 7 | P5 | - | - |
| I/O, VREF Bank 7, L49P | 7 | P6 | XC2S50E, 150E, 200E, 300E | All |
| I/O, L49N | 7 | P7 | XC2S50E, 150E, 200E, 300E | - |
| I/O | 7 | P8 | - | - |
| I/O | 7 | P9 | - | - |
| I/O, L48P | 7 | P10 | XC2S50E, 300E | XC2S100E, 150E, 200E, 300E |
| I/O, L48N | 7 | P11 | XC2S50E, 300E | - |
| GND | - | P12 | - | - |
| VCCO | - | P13 | - | - |
| VCCINT | - | P14 | - | - |
| I/O, L47P_YY | 7 | P15 | All | - |
| I/O, L47N_YY | 7 | P16 | All | - |
| I/O, L46P_YY | 7 | P17 | All | - |
| I/O, L46N_YY | 7 | P18 | All | - |
| GND | - | P19 | - | - |
| I/O, VREF Bank 7, L45P | 7 | P20 | XC2S50E, 300E | All |
| I/O, L45N | 7 | P21 | XC2S50E, 300E | - |

## PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| I/O | 7 | P22 | - | - |
| I/O, L44P_YY | 7 | P23 | All | - |
| I/O (IRDY), L44N_YY | 7 | P24 | All | - |
| GND | - | P25 | - | - |
| VCCO | - | P26 | - | - |
| | | | | |
| I/O (TRDY) | 6 | P27 | - | - |
| VCCINT | - | P28 | - | - |
| I/O | 6 | P29 | - | - |
| I/O, L43P | 6 | P30 | XC2S50E, 300E | - |
| I/O, VREF Bank 6, L43N | 6 | P31 | XC2S50E, 300E | All |
| GND | - | P32 | - | - |
| I/O, L42P_YY | 6 | P33 | All | - |
| I/O, L42N_YY | 6 | P34 | All | - |
| I/O, L41P_YY | 6 | P35 | All | - |
| I/O, L41N_YY | 6 | P36 | All | - |
| VCCINT | - | P37 | - | - |
| VCCO | - | P38 | - | - |
| GND | - | P39 | - | - |
| I/O, L40P | 6 | P40 | XC2S50E, 300E | - |
| I/O, L40N | 6 | P41 | XC2S50E, 300E | XC2S100E, 150E, 200E, 300E |
| I/O | 6 | P42 | - | - |
| I/O | 6 | P43 | - | - |
| I/O | 6 | P44 | - | - |

## PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| I/O, L28P | 4 | P89 | XC2S50E, 100E, 200E, 300E | - |
| VCCINT | - | P90 | - | - |
| VCCO | - | P91 | - | - |
| GND | - | P92 | - | - |
| I/O, L27N | 4 | P93 | XC2S50E, 100E, 200E, 300E | - |
| I/O, L27P | 4 | P94 | XC2S50E, 100E, 200E, 300E | XC2S100E, 150E, 200E, 300E |
| I/O | 4 | P95 | - | - |
| I/O | 4 | P96 | - | - |
| I/O, L26N_YY | 4 | P97 | All | - |
| I/O, VREF Bank 4, L26P_YY | 4 | P98 | All | All |
| I/O | 4 | P99 | - | - |
| I/O | 4 | P100 | - | XC2S200E, 300E |
| I/O, L25N_YY | 4 | P101 | All | - |
| I/O, L25P_YY | 4 | P102 | All | - |
| GND | - | P103 | - | - |
| | | | | |
| DONE | 3 | P104 | - | - |
| VCCO | - | P105 | - | - |
| $\overline{\text{PROGRAM}}$ | - | P106 | - | - |
| I/O ($\overline{\text{INIT}}$), L24N_YY | 3 | P107 | All | - |
| I/O (D7), L24P_YY | 3 | P108 | All | - |
| I/O | 3 | P109 | - | XC2S200E, 300E |
| I/O | 3 | P110 | - | - |

## PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| I/O, VREF Bank 3, L23N | 3 | P111 | XC2S50E, 150E, 200E, 300E | All |
| I/O, L23P | 3 | P112 | XC2S50E, 150E, 200E, 300E | - |
| I/O | 3 | P113 | - | - |
| I/O | 3 | P114 | - | - |
| I/O, L22N | 3 | P115 | XC2S50E, 300E | XC2S100E, 150E, 200E, 300E |
| I/O (D6), L22P | 3 | P116 | XC2S50E, 300E | - |
| GND | - | P117 | - | - |
| VCCO | - | P118 | - | - |
| VCCINT | - | P119 | - | - |
| I/O (D5), L21N_YY | 3 | P120 | All | - |
| I/O, L21P_YY | 3 | P121 | All | - |
| I/O, L20N_YY | 3 | P122 | All | - |
| I/O, L20P_YY | 3 | P123 | All | - |
| GND | - | P124 | - | - |
| I/O, VREF Bank 3, L19N | 3 | P125 | XC2S50E, 300E | All |
| I/O (D4), L19P | 3 | P126 | XC2S50E, 300E | - |
| I/O | 3 | P127 | - | - |
| VCCINT | - | P128 | - | - |
| I/O (TRDY) | 3 | P129 | - | - |
| VCCO | - | P130 | - | - |
| GND | - | P131 | - | - |
| | | | | |
| I/O (IRDY), L18N_YY | 2 | P132 | All | - |
| I/O, L18P_YY | 2 | P133 | All | - |

## FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option | Device-Specific Pinouts: XC2S | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Function | Bank | | | | 100E | 150E | 200E | 300E | 400E | 600E |
| TMS | - | E4 | - | - | TMS | TMS | TMS | TMS | TMS | TMS |
| I/O | 7 | D3 | XC2S150E | - | I/O | I/O, L113P_Y | I/O | I/O | I/O | I/O |
| I/O | 7 | C2 | - | - | - | - | - | I/O | I/O | I/O |
| I/O | 7 | C1 | XC2S150E | - | - | I/O, L113N_Y | I/O | I/O | I/O | I/O |
| I/O, L#P_Y | 7 | D2 | XC2S150E, 200E, 300E, 400E | - | - | I/O, L112P_Y | I/O, L119P_Y | I/O, L119P_Y | I/O, L119P_Y | I/O, L119P |
| I/O, L#N_Y | 7 | D1 | XC2S150E, 200E, 300E, 400E | - | I/O | I/O, L112N_Y | I/O, L119N_Y | I/O, L119N_Y | I/O, L119N_Y | I/O, L119N |
| I/O, L#P_Y | 7 | E2 | XC2S100E, 200E, 300E, 600E | XC2S200E, 300E, 400E, 600E | I/O, L85P_Y | I/O, L111P | I/O, VREF Bank 7, L118P_Y | I/O, VREF Bank 7, L118P_Y | I/O, VREF Bank 7, L118P | I/O, VREF Bank 7, L118P_Y |
| I/O, L#N_Y | 7 | E3 | XC2S100E, 200E, 300E, 600E | - | I/O, L85N_Y | I/O, L111N | I/O, L118N_Y | I/O, L118N_Y | I/O, L118N | I/O, L118N_Y |
| I/O | 7 | E1 | - | - | - | - | - | I/O | I/O | I/O |
| I/O | 7 | F5 | - | - | - | I/O | I/O | I/O | I/O | I/O |
| I/O, L#P_Y | 7 | F4 | XC2S100E, 200E, 300E, 600E | - | I/O, L84P_Y | I/O, L110P | I/O, L117P_Y | I/O, L117P_Y | I/O, L117P | I/O, L117P_Y |
| I/O, L#N_Y | 7 | F3 | XC2S100E, 200E, 300E, 600E | - | I/O, L84N_Y | I/O, L110N | I/O, L117N_Y | I/O, L117N_Y | I/O, L117N | I/O, L117N_Y |
| I/O, VREF Bank 7, L#P_Y | 7 | F2 | XC2S150E, 200E, 300E, 400E, 600E | All | I/O, VREF Bank 7, L83P | I/O, VREF Bank 7, L109P_Y | I/O, VREF Bank 7, L116P_Y | I/O, VREF Bank 7, L116P_Y | I/O, VREF Bank 7, L116P_Y | I/O, VREF Bank 7, L116P_Y |
| I/O, L#N_Y | 7 | F1 | XC2S150E, 200E, 300E, 400E, 600E | - | I/O, L83N | I/O, L109N_Y | I/O, L116N_Y | I/O, L116N_Y | I/O, L116N_Y | I/O, L116N_Y |
| I/O | 7 | G5 | - | - | - | I/O | I/O | I/O | I/O | I/O |
| I/O, L#P_Y | 7 | G4 | XC2S150E, 200E, 300E, 400E | - | - | I/O, L108P_Y | I/O, L115P_Y | I/O, L115P_Y | I/O, L115P_Y | I/O, L115P |
| I/O, L#N_Y | 7 | G3 | XC2S150E, 200E, 300E, 400E | - | I/O | I/O, L108N_Y | I/O, L115N_Y | I/O, L115N_Y | I/O, L115N_Y | I/O, L115N |
| I/O, L#P_Y | 7 | G2 | XC2S100E, 150E, 300E, 600E | XC2S600E | I/O, L82P_Y | I/O, L107P_Y | I/O, L114P | I/O, L114P_Y | I/O, L114P | I/O, VREF Bank 7, L114P_Y |
| I/O, L#N_Y | 7 | G1 | XC2S100E, 150E, 300E, 600E | - | I/O, L82N_Y | I/O, L107N_Y | I/O, L114N | I/O, L114N_Y | I/O, L114N | I/O, L114N_Y |

## FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

| Pad Name | | | LVDS Async. Output Option | $V_{REF}$ Option | Device-Specific Pinouts: XC2S | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Function | Bank | Pin | | | 100E | 150E | 200E | 300E | 400E | 600E |
| I/O (WRITE), L#N_YY | 1 | A20 | All | - | I/O (WRITE), L20N_YY | I/O (WRITE), L26N_YY | I/O (WRITE), L28N_YY | I/O (WRITE), L28N_YY | I/O (WRITE), L28N_YY | I/O (WRITE), L28N_YY |
| I/O | 1 | D18 | - | - | - | - | - | I/O | I/O | I/O |
| I/O | 1 | C18 | - | - | - | I/O | I/O | I/O | I/O | I/O |
| I/O, L#P | 1 | B19 | XC2S200E, 300E, 400E, 600E | - | - | I/O, L25P | I/O, L27P_Y | I/O, L27P_Y | I/O, L27P_Y | I/O, L27P_Y |
| I/O, L#N | 1 | A19 | XC2S200E, 300E, 400E, 600E | - | I/O | I/O, L25N | I/O, L27N_Y | I/O, L27N_Y | I/O, L27N_Y | I/O, L27N_Y |
| I/O, L#P | 1 | B18 | XC2S100E, 200E, 300E, 400E, 600E | XC2S200E, 300E, 400E, 600E | I/O, L19P_Y | I/O, L24P | I/O, VREF Bank 1, L26P_Y | I/O, VREF Bank 1, L26P_Y | I/O, VREF Bank 1, L26P_Y | I/O, VREF Bank 1, L26P_Y |
| I/O, L#N | 1 | A18 | XC2S100E, 200E, 300E, 400E, 600E | - | I/O, L19N_Y | I/O, L24N | I/O, L26N_Y | I/O, L26N_Y | I/O, L26N_Y | I/O, L26N_Y |
| I/O | 1 | D17 | - | - | - | - | - | I/O | I/O | I/O |
| I/O | 1 | C17 | - | - | - | I/O | I/O | I/O | I/O | I/O |
| I/O, L#P_YY | 1 | B17 | All | - | I/O, L18P_YY | I/O, L23P_YY | I/O, L25P_YY | I/O, L25P_YY | I/O, L25P_YY | I/O, L25P_YY |
| I/O, L#N_YY | 1 | A17 | All | - | I/O, L18N_YY | I/O, L23N_YY | I/O, L25N_YY | I/O, L25N_YY | I/O, L25N_YY | I/O, L25N_YY |
| I/O, VREF Bank 1, L#P_YY | 1 | E16 | All | All | I/O, VREF Bank 1, L17P_YY | I/O, VREF Bank 1, L22P_YY | I/O, VREF Bank 1, L24P_YY | I/O, VREF Bank 1, L24P_YY | I/O, VREF Bank 1, L24P_YY | I/O, VREF Bank 1, L24P_YY |
| I/O, L#N_YY | 1 | E17 | All | - | I/O, L17N_YY | I/O, L22N_YY | I/O, L24N_YY | I/O, L24N_YY | I/O, L24N_YY | I/O, L24N_YY |
| I/O | 1 | E15 | - | - | - | I/O | I/O | I/O | I/O | I/O |
| I/O, L#P | 1 | D16 | XC2S300E, 600E | - | - | I/O, L21P | I/O, L23P | I/O, L23P_Y | I/O, L23P | I/O, L23P_Y |
| I/O, L#N | 1 | C16 | XC2S300E, 600E | - | I/O | I/O, L21N | I/O, L23N | I/O, L23N_Y | I/O, L23N | I/O, L23N_Y |
| I/O, L#P | 1 | B16 | XC2S100E, 300E, 600E | XC2S600E | I/O, L16P_Y | I/O, L20P | I/O, L22P | I/O, L22P_Y | I/O, L22P | I/O, VREF Bank 1, L22P_Y |
| I/O, L#N | 1 | A16 | XC2S100E, 300E, 600E | - | I/O, L16N_Y | I/O, L20N | I/O, L22N | I/O, L22N_Y | I/O, L22N | I/O, L22N_Y |
| I/O | 1 | F14 | - | - | - | - | - | I/O | I/O | I/O |
| I/O, VREF Bank 1, L#P | 1 | D15 | XC2S100E, 200E, 300E, 400E, 600E | All | I/O, VREF Bank 1, L15P_Y | I/O, VREF Bank 1, L19P | I/O, VREF Bank 1, L21P_Y | I/O, VREF Bank 1, L21P_Y | I/O, VREF Bank 1, L21P_Y | I/O, VREF Bank 1, L21P_Y |
| I/O, L#N | 1 | C15 | XC2S100E, 200E, 300E, 400E, 600E | - | I/O, L15N_Y | I/O, L19N | I/O, L21N_Y | I/O, L21N_Y | I/O, L21N_Y | I/O, L21N_Y |
| I/O, L#P | 1 | B15 | XC2S100E, 200E, 300E, 400E, 600E | - | I/O, L14P_Y | I/O, L18P | I/O, L20P_Y | I/O, L20P_Y | I/O, L20P_Y | I/O, L20P_Y |

## FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

| Pad Name | | Pin | LVDS Async. Output Option | VREF Option | Device-Specific Pinouts | |
|---|---|---|---|---|---|---|
| Function | Bank | | | | XC2S400E | XC2S600E |
| I/O, L201P | 7 | E4 | XC2S400E | - | I/O, L201P_Y | I/O, L201P |
| I/O, L201N | 7 | F5 | XC2S400E | - | I/O, L201N_Y | I/O, L201N |
| I/O, VREF Bank 7, L200P | 7 | F4 | XC2S600E | All | I/O, VREF Bank 7, L200P | I/O, VREF Bank 7, L200P_Y |
| I/O, L200N | 7 | F3 | XC2S600E | - | I/O, L200N | I/O, L200N_Y |
| I/O, L199P | 7 | F2 | XC2S600E | - | - | I/O, L199P_Y |
| I/O, L199N | 7 | F1 | XC2S600E | - | I/O | I/O, L199N_Y |
| I/O, L198P | 7 | G6 | XC2S400E | - | I/O, L198P_Y | I/O, L198P |
| I/O, L198N | 7 | G5 | XC2S400E | - | I/O, L198N_Y | I/O, L198N |
| I/O, L197P | 7 | G4 | XC2S600E | - | I/O, L197P | I/O, L197P_Y |
| I/O, L197N | 7 | G3 | XC2S600E | - | I/O, L197N | I/O, L197N_Y |
| I/O, VREF Bank 7, L196P_YY | 7 | G2 | All | All | I/O, VREF Bank 7, L196P_YY | I/O, VREF Bank 7, L196P_YY |
| I/O, L196N_YY | 7 | G1 | All | - | I/O, L196N_YY | I/O, L196N_YY |
| I/O | 7 | H7 | - | - | I/O | I/O |
| I/O, L195P_YY | 7 | H6 | All | - | I/O, L195P_YY | I/O, L195P_YY |
| I/O, L195N_YY | 7 | H5 | All | - | I/O, L195N_YY | I/O, L195N_YY |
| I/O | 7 | J8 | - | - | - | I/O |
| I/O, L194P | 7 | H2 | XC2S400E | - | I/O, L194P_Y | I/O, L194P |
| I/O, L194N | 7 | H1 | XC2S400E | - | I/O, L194N_Y | I/O, L194N |
| I/O, L193P | 7 | J7 | XC2S600E | XC2S600E | I/O | I/O, VREF Bank 7, L193P_Y |
| I/O, L193N | 7 | J6 | XC2S600E | - | - | I/O, L193N_Y |
| I/O | 7 | J5 | - | - | I/O | I/O |
| I/O, L192P_YY | 7 | J4 | All | - | I/O, L192P_YY | I/O, L192P_YY |
| I/O, L192N_YY | 7 | J3 | All | - | I/O, L192N_YY | I/O, L192N_YY |
| I/O | 7 | K5 | - | - | I/O | I/O |
| I/O, VREF Bank 7, L191P_YY | 7 | J2 | All | All | I/O, VREF Bank 7, L191P_YY | I/O, VREF Bank 7, L191P_YY |
| I/O, L191N_YY | 7 | J1 | All | - | I/O, L191N_YY | I/O, L191N_YY |
| I/O, L190P_YY | 7 | K8 | All | - | I/O, L190P_YY | I/O, L190P_YY |
| I/O, L190N_YY | 7 | K7 | All | - | I/O, L190N_YY | I/O, L190N_YY |
| I/O | 7 | K4 | - | - | - | I/O |
| I/O, L189P_YY | 7 | K3 | All | - | I/O, L189P_YY | I/O, L189P_YY |
| I/O, L189N_YY | 7 | K2 | All | - | I/O, L189N_YY | I/O, L189N_YY |
| I/O | 7 | K1 | - | - | - | I/O |

## FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

| Pad Name | | Pin | LVDS Async. Output Option | VREF Option | Device-Specific Pinouts | |
|---|---|---|---|---|---|---|
| Function | Bank | | | | XC2S400E | XC2S600E |
| | | | | | | |
| I/O | 5 | AC5 | - | - | I/O | I/O |
| I/O, L152N | 5 | AE4 | - | - | I/O | I/O, L152N |
| I/O, L152P | 5 | AF4 | - | - | - | I/O, L152P |
| I/O, L151N | 5 | AE5 | - | - | - | I/O, L151N |
| I/O, L151P | 5 | AF5 | - | - | I/O | I/O, L151P |
| I/O, L150N | 5 | AA6 | XC2S400E | - | I/O, L150N_Y | I/O, L150N |
| I/O, L150P | 5 | AB6 | XC2S400E | - | I/O, L150P_Y | I/O, L150P |
| I/O, L149N_YY | 5 | AC6 | All | - | I/O, L149N_YY | I/O, L149N_YY |
| I/O, L149P_YY | 5 | AD6 | All | - | I/O, L149P_YY | I/O, L149P_YY |
| I/O, VREF Bank 5, L148N_YY | 5 | AE6 | All | All | I/O, VREF Bank 5, L148N_YY | I/O, VREF Bank 5, L148N_YY |
| I/O, L148P_YY | 5 | AF6 | All | - | I/O, L148P_YY | I/O, L148P_YY |
| I/O, L147N | 5 | AA7 | XC2S600E | - | - | I/O, L147N_Y |
| I/O, L147P | 5 | AB7 | XC2S600E | - | I/O | I/O, L147P_Y |
| I/O, L146N_YY | 5 | AC7 | All | - | I/O, L146N_YY | I/O, L146N_YY |
| I/O, L146P_YY | 5 | AD7 | All | - | I/O, L146P_YY | I/O, L146P_YY |
| I/O, L145N_YY | 5 | AE7 | All | - | I/O, L145N_YY | I/O, L145N_YY |
| I/O, L145P_YY | 5 | AF7 | All | - | I/O, L145P_YY | I/O, L145P_YY |
| I/O, VREF Bank 5, L144N_YY | 5 | Y8 | All | All | I/O, VREF Bank 5, L144N_YY | I/O, VREF Bank 5, L144N_YY |
| I/O, L144P_YY | 5 | AA8 | All | - | I/O, L144P_YY | I/O, L144P_YY |
| I/O, L143N_YY | 5 | AE8 | All | - | I/O, L143N_YY | I/O, L143N_YY |
| I/O, L143P_YY | 5 | AF8 | All | - | I/O, L143P_YY | I/O, L143P_YY |
| I/O | 5 | AB8 | - | - | I/O | I/O |
| I/O, L142N | 5 | W9 | XC2S600E | - | I/O, L142N | I/O, L142N_Y |
| I/O, L142P | 5 | Y9 | XC2S600E | - | I/O, L142P | I/O, L142P_Y |
| I/O, L141N | 5 | AA9 | XC2S600E | XC2S600E | - | I/O, VREF Bank 5, L141N_Y |
| I/O, L141P | 5 | AB9 | XC2S600E | - | I/O | I/O, L141P_Y |
| I/O, L140N_YY | 5 | AC9 | All | - | I/O, L140N_YY | I/O, L140N_YY |
| I/O, L140P_YY | 5 | AD9 | All | - | I/O, L140P_YY | I/O, L140P_YY |
| I/O, L139N_YY | 5 | AE9 | All | - | I/O, L139N_YY | I/O, L139N_YY |
| I/O, L139P_YY | 5 | AF9 | All | - | I/O, L139P_YY | I/O, L139P_YY |
| I/O, VREF Bank 5, L138N_YY | 5 | W10 | All | All | I/O, VREF Bank 5, L138N_YY | I/O, VREF Bank 5, L138N_YY |

## FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

| Pad Name | | Pin | LVDS Async. Output Option | VREF Option | Device-Specific Pinouts | |
|---|---|---|---|---|---|---|
| Function | Bank | | | | XC2S400E | XC2S600E |
| I/O, L88P_YY | 3 | V25 | All | - | I/O, L88P_YY | I/O, L88P_YY |
| I/O | 3 | V26 | - | - | I/O | I/O |
| I/O, VREF Bank 3, L87N_YY | 3 | U19 | All | All | I/O, VREF Bank 3, L87N_YY | I/O, VREF Bank 3, L87N_YY |
| I/O (D6), L87P_YY | 3 | U20 | All | - | I/O (D6), L87P_YY | I/O (D6), L87P_YY |
| I/O (D5), L86N_YY | 3 | U22 | All | - | I/O (D5), L86N_YY | I/O (D5), L86N_YY |
| I/O, L86P_YY | 3 | U23 | All | - | I/O, L86P_YY | I/O, L86P_YY |
| I/O | 3 | U24 | - | - | - | I/O |
| I/O, L85N | 3 | U25 | XC2S600E | - | - | I/O, L85N_Y |
| I/O, L85P | 3 | U26 | XC2S600E | - | I/O | I/O, L85P_Y |
| I/O | 3 | R18 | - | - | I/O | I/O |
| I/O, L84N | 3 | T19 | XC2S400E | - | I/O, L84N_Y | I/O, L84N |
| I/O, L84P | 3 | T20 | XC2S400E | - | I/O, L84P_Y | I/O, L84P |
| I/O, L83N | 3 | T21 | XC2S600E | - | I/O, L83N | I/O, L83N_Y |
| I/O, L83P | 3 | T22 | XC2S600E | - | I/O, L83P | I/O, L83P_Y |
| I/O | 3 | T24 | - | - | - | I/O |
| I/O, L82N | 3 | T25 | XC2S600E | - | I/O, L82N | I/O, L82N_Y |
| I/O, L82P | 3 | T26 | XC2S600E | - | I/O, L82P | I/O, L82P_Y |
| I/O | 3 | R19 | - | - | - | I/O |
| I/O, L81N | 3 | R20 | XC2S600E | - | I/O, L81N | I/O, L81N_Y |
| I/O, L81P | 3 | R21 | XC2S600E | - | I/O, L81P | I/O, L81P_Y |
| I/O, VREF Bank 3, L80N_YY | 3 | R22 | All | All | I/O, VREF Bank 3, L80N_YY | I/O, VREF Bank 3, L80N_YY |
| I/O (D4), L80P_YY | 3 | R23 | All | - | I/O (D4), L80P_YY | I/O (D4), L80P_YY |
| I/O | 3 | P18 | - | - | - | I/O |
| I/O, L79N_YY | 3 | R25 | All | - | I/O, L79N_YY | I/O, L79N_YY |
| I/O, L79P_YY | 3 | R26 | All | - | I/O, L79P_YY | I/O, L79P_YY |
| I/O | 3 | P19 | - | - | - | I/O |
| I/O, L78N | 3 | P20 | XC2S400E | - | I/O, L78N_Y | I/O, L78N |
| I/O, L78P | 3 | P21 | XC2S400E | - | I/O, L78P_Y | I/O, L78P |
| I/O, VREF Bank 3, L77N | 3 | P22 | XC2S600E | All | I/O, VREF Bank 3, L77N | I/O, VREF Bank 3, L77N_Y |
| I/O, L77P | 3 | P23 | XC2S600E | - | I/O, L77P | I/O, L77P_Y |
| I/O | 3 | P24 | - | - | - | I/O |
| I/O, L76N_YY | 3 | P25 | All | - | I/O, L76N_YY | I/O, L76N_YY |
| I/O, L76P_YY | 3 | P26 | All | - | I/O, L76P_YY | I/O, L76P_YY |

## Revision History

| Date | Version | Description |
|---|---|---|
| 11/15/2001 | 1.0 | Initial Xilinx release. |
| 12/20/2001 | 1.1 | Corrected differential pin pair designations. |
| 11/18/2002 | 2.0 | Added XC2S400E and XC2S600E and FG676. Removed L37 designation from FT256 pinouts. Minor corrections and clarifications to pinout definitions. Removed Preliminary designation. |
| 02/14/2003 | 2.1 | Added differential pairs table on page 57, fixed 3 P/N designation typos introduced in v2.0. Clarified that XC2S50E has two VREF pins per bank. |
| 06/18/2008 | 2.3 | Added Package Overview section. Updated all modules for continuous page, figure, and table numbering. Updated links. Synchronized all modules to v2.3. |
| 08/09/2013 | 3.0 | This product is obsolete/discontinued per XCN12026. |