AMD Xilinx - XC2S300E-6PQG208C Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

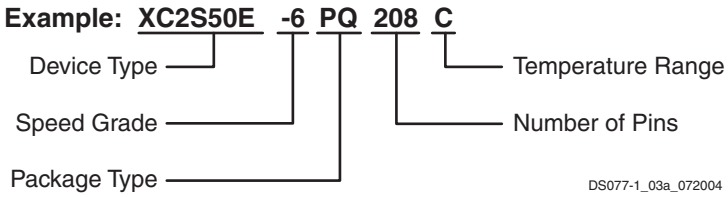
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1536
Number of Logic Elements/Cells	6912
Total RAM Bits	65536
Number of I/O	146
Number of Gates	300000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s300e-6pqg208c

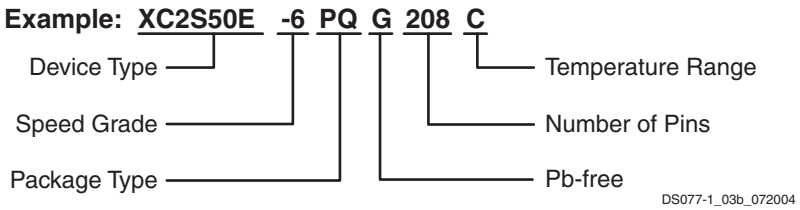
Ordering Information

Spartan-IIE devices are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a special "G" character in the ordering code.

Standard Packaging



Pb-Free Packaging



Device Ordering Options

Device
XC2S50E
XC2S100E
XC2S150E
XC2S200E
XC2S300E
XC2S400E
XC2S600E

Speed Grade	
-6	Standard Performance
-7	Higher Performance(1)

Package Type / Number of Pins	
TQ(G)144	144-pin Plastic Thin QFP
PQ(G)208	208-pin Plastic QFP
FT(G)256	256-ball Fine Pitch BGA
FG(G)456	456-ball Fine Pitch BGA
FG(G)676	676-ball Fine Pitch BGA

Temperature Range (T_J)(2)	
C = Commercial	0°C to +85°C
I = Industrial	–40°C to +100°C

Notes:
1. The -7 speed grade is exclusively available in the Commercial temperature range.
2. See www.xilinx.com for information on automotive temperature range devices.

Device Part Marking

Figure 2 is a top marking example for Spartan-IIE FPGAs in the quad-flat packages. The markings for BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator.

The "7C" and "6I" Speed Grade/Temperature Range part combinations may be dual marked as "7C/6I". Devices with the dual mark can be used as either -7C or -6I devices. Devices with a single mark are only guaranteed for the marked speed grade and temperature range.

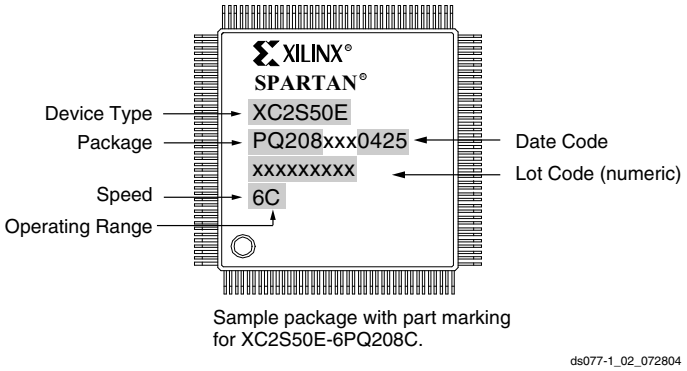


Figure 2: **Spartan-IIE QFP Marking Example**

Optional pull-up and pull-down resistors and an optional weak-keeper circuit are attached to each user I/O pad. Prior to configuration all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but inputs may optionally be pulled up. The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins will float. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. After configuration, clamping diodes are connected to V_{CCO} for LVTTL, PCI, HSTL, SSTL, CTT, and AGP standards.

All Spartan-IIE FPGA IOBs support IEEE 1149.1-compatible boundary scan testing.

Input Path

A buffer in the IOB input path routes the input signal directly to internal logic and through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can used in close proximity to each other. See I/O Banking.

There are optional pull-up and pull-down resistors at each input for use after configuration.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. Each output buffer can source up to 24 mA and sink up to 48 mA. Drive strength and slew rate controls minimize bus transients. The default output driver is LVTTL with 12 mA drive strength and slow slew rate.

In most signaling standards, the output high voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See I/O Banking.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way helps eliminate bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signaling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks (see Figure 5). The pinout tables show the bank affiliation of each I/O (see Pinout Tables, page 53). Each bank has multiple V_{CCO} pins which must be connected to the same voltage. Voltage requirements are determined by the output standards in use.

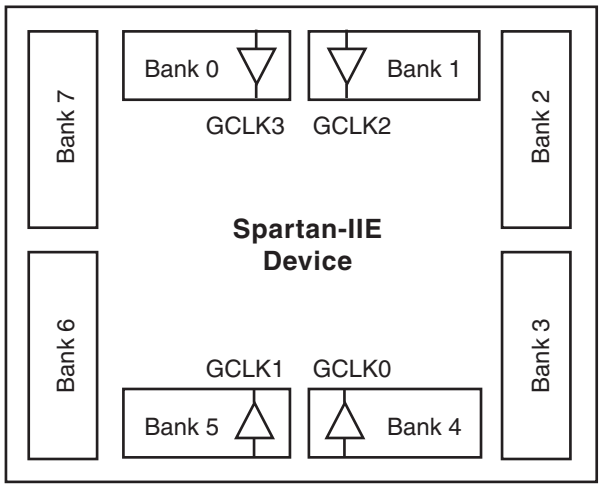


Figure 5: **Spartan-IIE I/O Banks**

In the TQ144 and PQ208 packages, the eight banks have V_{CCO} connected together. Thus, only one V_{CCO} level is allowed in these packages, although different V_{REF} values are allowed in each of the eight banks.

Within a bank, standards may be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 4. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO}. Note that V_{CCO}

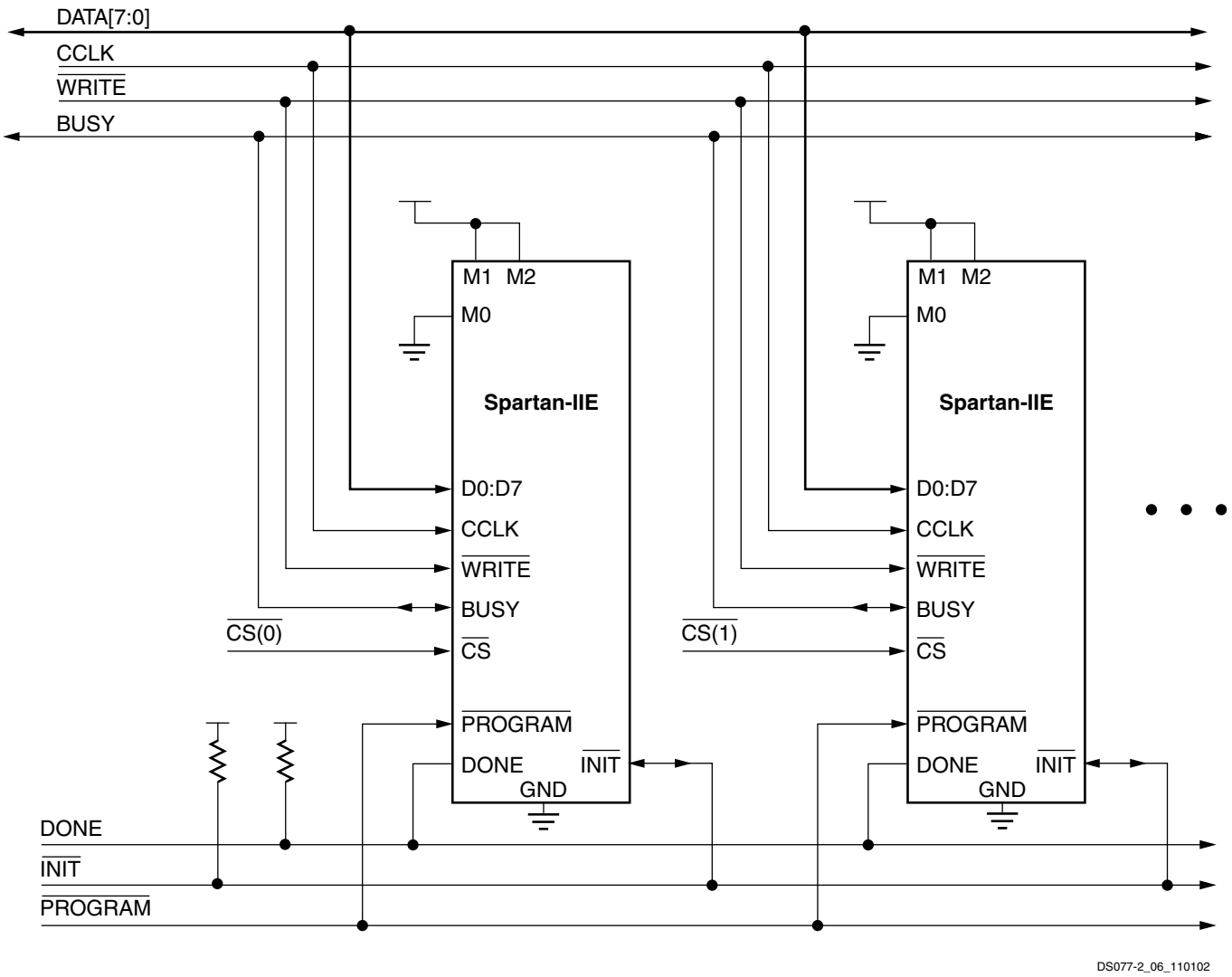


Figure 20: **Slave Parallel Configuration Circuit Diagram**

Multiple Spartan-IIE FPGAs can be configured using the Slave Parallel mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, $\overline{\text{WRITE}}$, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the $\overline{\text{CS}}$ pin of each device in turn and writing the appropriate data. Sync-to-DONE start-up timing is used to ensure that the start-up sequence does not begin until all the FPGAs have been loaded. See Start-up, page 23.

Write

When using the Slave Parallel Mode, write operations send packets of byte-wide configuration data into the FPGA. Figure 21, page 28 shows a flowchart of the write sequence used to load data into the Spartan-IIE FPGA. This is an expansion of the "Load Configuration Data Frames" block in Figure 16, page 23.

The timing for Slave Parallel mode is shown in Figure 26, page 50.

For the present example, the user holds $\overline{\text{WRITE}}$ and $\overline{\text{CS}}$ Low throughout the sequence of write operations. Note that when $\overline{\text{CS}}$ is asserted on successive CCLKs, $\overline{\text{WRITE}}$ must remain either asserted or deasserted. Otherwise an abort will be initiated, as in the next section.

1. Drive data onto D0-D7. Note that to avoid contention, the data source should not be enabled while $\overline{\text{CS}}$ is Low and $\overline{\text{WRITE}}$ is High. Similarly, while $\overline{\text{WRITE}}$ is High, no more than one device's $\overline{\text{CS}}$ should be asserted.
2. On the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this happens.
3. Repeat steps 1 and 2 until all the data has been sent.
4. Deassert $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL I	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	8	–8
HSTL III	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	24	–8
HSTL IV	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	48	–8
SSTL3 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	–8
SSTL3 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	–16
SSTL2 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.61	V_{REF} + 0.61	7.6	–7.6
SSTL2 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	15.2	–15.2
CTT	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.4	V_{REF} + 0.4	8	–8
AGP	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	Note (2)	Note (2)

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested.
2. Tested according to the relevant specifications.

LVDS DC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		2.375	2.5	2.625	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	1.25	1.425	1.6	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	0.9	1.075	1.25	V
V_{ODIFF}	Differential output voltage (Q – $\overline{Q}$), Q = High or ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	250	350	450	mV
V_{OCM}	Output common-mode voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.125	1.25	1.375	V
V_{IDIFF}	Differential input voltage (Q – $\overline{Q}$), Q = High or ($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25 V	100	350	-	mV
V_{ICM}	Input common-mode voltage	Differential input voltage = ±350 mV	0.2	1.25	2.2	V

LVPECL DC Specifications

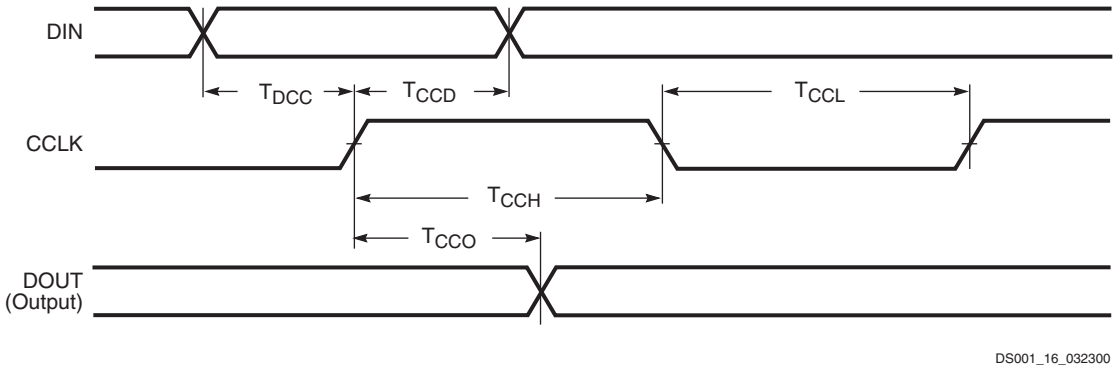
These values are valid at the output of the source termination pack shown under LVPECL, with a 100Ω differential load only. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. The following table summarizes the DC output specifications of LVPECL.

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential input voltage	0.3	-	0.3	-	0.3	-	V

IOB Input Delay Adjustments for Different Standards

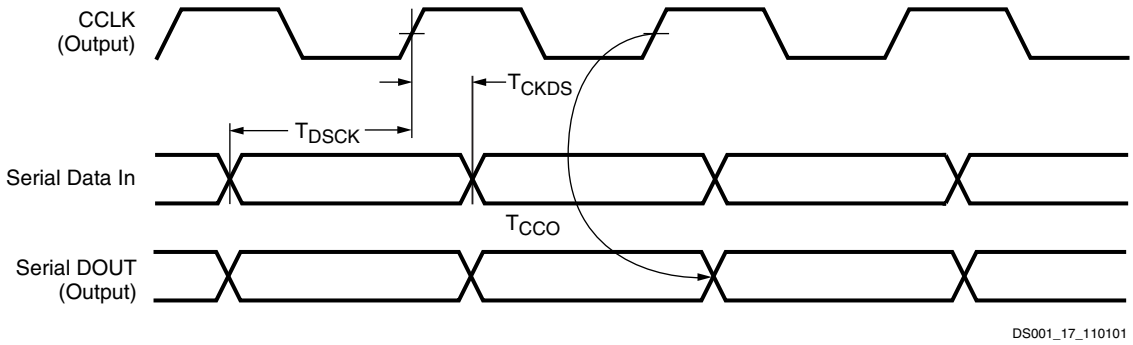
Input delays associated with the pad are specified for LVTTL. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade		Units
			-7	-6	
Data Input Delay Adjustments					
T_{ILVTTL}	Standard-specific data input delay adjustments	LVTTL	0	0	ns
$T_{ILVCMOS2}$		LVCMOS2	0	0	ns
$T_{ILVCMOS18}$		LVCMOS18	0.20	0.20	ns
T_{ILVDS}		LVDS	0.15	0.15	ns
$T_{ILVPECL}$		LVPECL	0.15	0.15	ns
T_{IPCI33_3}		PCI, 33 MHz, 3.3V	0.08	0.08	ns
T_{IPCI66_3}		PCI, 66 MHz, 3.3V	–0.11	–0.11	ns
T_{IGTL}		GTL	0.14	0.14	ns
T_{IGTLP}		GTL+	0.14	0.14	ns
T_{IHSTL}		HSTL	0.04	0.04	ns
T_{ISSTL2}		SSTL2	0.04	0.04	ns
T_{ISSTL3}		SSTL3	0.04	0.04	ns
T_{ICTT}		CTT	0.10	0.10	ns
T_{IAGP}		AGP	0.04	0.04	ns



Symbol		Description	All Devices		Units
			Min	Max	
T_{DCC} / T_{CCD}	CCLK	DIN setup/hold	5 / 0	-	ns
T_{CCO}		DOUT	-	12	ns
T_{CCH}		High time	5	-	ns
T_{CCL}		Low time	5	-	ns
F_{CC}		Maximum frequency	-	66	MHz

Figure 24: **Slave Serial Mode Timing**



Symbol		Description	All Devices		Units
			Min	Max	
T_{DSCK} / T_{CKDS}	CCLK	DIN setup/hold	5 / 0	-	ns
T_{CCO}		DOUT	-	12	ns
F_{CC}		Frequency tolerance with respect to nominal	–30%	+45%	-

Figure 25: **Master Serial Mode Timing**

Revision History

Date	Version	Description
11/15/2001	1.0	Initial Xilinx release.
06/28/2002	1.1	Added -7 speed grade and extended DLL specs to Industrial.
11/18/2002	2.0	Added XC2S400E and XC2S600E. Added minimum specifications. Added reference to XAPP450 for Power-On Requirements. Removed Preliminary designation.
07/09/2003	2.1	Added I_{CCINTQ} typical values. Reduced ICCPO power-on current requirements. Relaxed TCCPO power-on ramp requirements. Added IHSPO to describe current in hot-swap applications. Updated TPSFD / TPHFD description to indicate use of delay element.
06/18/2008	2.3	Updated I/O measurement thresholds. Updated all modules for continuous page, figure, and table numbering. Updated links. Synchronized all modules to v2.3.
08/09/2013	3.0	This product is obsolete/discontinued per XCN12026.

Pin Definitions *(Continued)*

Pad Name	Dedicated Pin	Direction	Description
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In Slave Parallel mode, D0-D7 are configuration data input pins. During readback, D0-D7 are output pins. These pins become user I/Os after configuration unless the Slave Parallel port is retained. In serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
$\overline{WRITE}$	No	Input	In Slave Parallel mode, the active-low Write Enable signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
$\overline{CS}$	No	Input	In Slave Parallel mode, the active-low Chip Select signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary Scan Test Access Port pins (IEEE 1149.1).
V_{CCINT}	Yes	Input	1.8V power supply pins for the internal core logic.
V_{CCO}	Yes	Input	Power supply pins for output drivers (1.5V, 1.8V, 2.5V, or 3.3V subject to banking rules in the Functional Description module.
V_{REF}	No	Input	Input threshold reference voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules in the Functional Description module.
GND	Yes	Input	Ground. All must be connected.
IRDY, TRDY	No	See PCI core documentation	These signals can only be accessed when using Xilinx PCI cores. If the cores are not used, these pins are available as user I/Os.
L#[P/N] (e.g., L0P)	No	Bidirectional	Differential I/O with synchronous output. P = positive, N = negative. The number (#) is used to associate the two pins of a differential pair. Becomes a general user I/O when not needed for differential signals.
L#[P/N]_Y (e.g., L0P_Y)	No	Bidirectional	Differential I/O with asynchronous or synchronous output (asynchronous output not compatible for all densities in a package). P = positive, N = negative. The number (#) is used to associate the two pins of a differential pair. Becomes a general user I/O when not needed for differential signals.
L#[P/N]_YY (e.g., L0P_YY)	No	Bidirectional	Differential I/O with asynchronous or synchronous output (compatible for all densities in a package). P = positive, N = negative. The number (#) is used to associate the two pins of a differential pair. Becomes a general user I/O when not needed for differential signals.
I/O	No	Bidirectional	These pins can be configured to be input and/or output after configuration is completed. Unused I/Os are disabled with a weak pull-down resistor. After power-on and before configuration is completed, these pins are either pulled up or left floating according to the Mode pin values. See the DC and Switching Characteristics module for power-on characteristics.

Package Thermal Characteristics

Table 14 provides the thermal characteristics for the various Spartan-II FPGA package offerings. This information is also available using the Thermal Query tool on xilinx.com (www.xilinx.com/cgi-bin/thermal/thermal.pl).

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board (θ_{JB}) value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The "Still Air (0 LFM)" column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 14: **Spartan-IIE Package Thermal Characteristics**

Package	Device	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
TQ144 TQG144	XC2S50E	5.8	N/A	32.3	25.1	21.5	20.1	°C/Watt
	XC2S100E	5.3	N/A	31.4	24.4	20.8	19.6	°C/Watt
PQ208 PQG208	XC2S50E	7.1	N/A	35.1	25.9	22.9	21.2	°C/Watt
	XC2S100E	6.1	N/A	34.2	25.2	22.3	20.7	°C/Watt
	XC2S150E	6.0	N/A	34.1	25.2	22.2	20.6	°C/Watt
	XC2S200E	4.6	N/A	32.4	23.9	21.2	19.6	°C/Watt
	XC2S300E	4.0	N/A	31.6	23.3	20.6	19.1	°C/Watt
FT256 FTG256	XC2S50E	7.3	17.8	27.4	21.6	20.4	20.0	°C/Watt
	XC2S100E	5.8	15.1	25.0	19.5	18.2	17.8	°C/Watt
	XC2S150E	5.7	14.8	24.8	19.3	18.0	17.6	°C/Watt
	XC2S200E	3.9	11.4	21.9	16.6	15.2	14.7	°C/Watt
	XC2S300E	3.2	10.1	20.8	15.6	14.2	13.7	°C/Watt
	XC2S400E	2.5	8.8	19.7	14.5	13.2	12.6	°C/Watt
FG456 FGG456	XC2S100E	8.4	14.9	24.3	19.2	18.1	17.4	°C/Watt
	XC2S150E	8.2	14.6	24.1	19.0	17.9	17.1	°C/Watt
	XC2S200E	6.3	11.6	21.0	16.1	15.0	14.3	°C/Watt
	XC2S300E	5.6	10.4	19.9	15.1	13.9	13.2	°C/Watt
	XC2S400E	3.6	6.5	17.7	11.7	10.5	10.0	°C/Watt
	XC2S600E	2.7	5.0	17.3	11.2	10.0	9.5	°C/Watt
FG676 FGG676	XC2S400E	4.1	7.9	15.6	11.1	9.8	9.2	°C/Watt
	XC2S600E	3.4	6.9	14.5	9.9	8.6	7.9	°C/Watt

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 1, L6P	1	P178	XC2S50E, 200E, 300E	All
I/O, L6N	1	P179	XC2S50E, 200E, 300E	-
I/O	1	P180	-	-
I/O (DLL), L5P	1	P181	-	-
GCK2, I	1	P182	-	-
GND	-	P183	-	-
VCCO	-	P184	-	-
GCK3, I	0	P185	-	-
VCCINT	-	P186	-	-
I/O (DLL), L5N	0	P187	-	-
I/O, L4P	0	P188	XC2S50E, 200E, 300E	-
I/O, VREF Bank 0, L4N	0	P189	XC2S50E, 200E, 300E	All
GND	-	P190	-	-
I/O, L3P	0	P191	XC2S50E, 200E, 300E	-
I/O, L3N	0	P192	XC2S50E, 200E, 300E	-
I/O, L2P	0	P193	XC2S50E, 100E, 200E, 300E	-
I/O, L2N	0	P194	XC2S50E, 100E, 200E, 300E	-
VCCINT	-	P195	-	-
VCCO	-	P196	-	-
GND	-	P197	-	-
I/O, L1P	0	P198	XC2S50E, 100E, 200E, 300E	-
I/O, L1N	0	P199	XC2S50E, 100E, 200E, 300E	XC2S100E, 150E, 200E, 300E
I/O	0	P200	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O	0	P201	-	-
I/O, L0P_YY	0	P202	All	-
I/O, VREF Bank 0, L0N_YY	0	P203	All	All
I/O	0	P204	-	-
I/O	0	P205	-	XC2S200E, 300E
I/O	0	P206	-	-
TCK	-	P207	-	-
VCCO	-	P208	-	-

PQ208 Differential Clock Pins

Clock	Bank	P		N	
		Pin	Name	Pin	Name
GCK0	4	P80	GCK0, I	P81	I/O (DLL), L31P
GCK1	5	P77	GCK1, I	P75	I/O (DLL), L31N
GCK2	1	P182	GCK2, I	P181	I/O (DLL), L5P
GCK3	0	P185	GCK3, I	P187	I/O (DLL), L5N

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
TMS	-	E4	-	-	TMS	TMS	TMS	TMS	TMS	TMS
I/O	7	D3	XC2S150E	-	I/O	I/O, L113P_Y	I/O	I/O	I/O	I/O
I/O	7	C2	-	-	-	-	-	I/O	I/O	I/O
I/O	7	C1	XC2S150E	-	-	I/O, L113N_Y	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	D2	XC2S150E, 200E, 300E, 400E	-	-	I/O, L112P_Y	I/O, L119P_Y	I/O, L119P_Y	I/O, L119P_Y	I/O, L119P
I/O, L#N_Y	7	D1	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L112N_Y	I/O, L119N_Y	I/O, L119N_Y	I/O, L119N_Y	I/O, L119N
I/O, L#P_Y	7	E2	XC2S100E, 200E, 300E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L85P_Y	I/O, L111P	I/O, VREF Bank 7, L118P_Y	I/O, VREF Bank 7, L118P_Y	I/O, VREF Bank 7, L118P	I/O, VREF Bank 7, L118P_Y
I/O, L#N_Y	7	E3	XC2S100E, 200E, 300E, 600E	-	I/O, L85N_Y	I/O, L111N	I/O, L118N_Y	I/O, L118N_Y	I/O, L118N	I/O, L118N_Y
I/O	7	E1	-	-	-	-	-	I/O	I/O	I/O
I/O	7	F5	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	F4	XC2S100E, 200E, 300E, 600E	-	I/O, L84P_Y	I/O, L110P	I/O, L117P_Y	I/O, L117P_Y	I/O, L117P	I/O, L117P_Y
I/O, L#N_Y	7	F3	XC2S100E, 200E, 300E, 600E	-	I/O, L84N_Y	I/O, L110N	I/O, L117N_Y	I/O, L117N_Y	I/O, L117N	I/O, L117N_Y
I/O, VREF Bank 7, L#P_Y	7	F2	XC2S150E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 7, L83P	I/O, VREF Bank 7, L109P_Y	I/O, VREF Bank 7, L116P_Y	I/O, VREF Bank 7, L116P_Y	I/O, VREF Bank 7, L116P_Y	I/O, VREF Bank 7, L116P_Y
I/O, L#N_Y	7	F1	XC2S150E, 200E, 300E, 400E, 600E	-	I/O, L83N	I/O, L109N_Y	I/O, L116N_Y	I/O, L116N_Y	I/O, L116N_Y	I/O, L116N_Y
I/O	7	G5	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	G4	XC2S150E, 200E, 300E, 400E	-	-	I/O, L108P_Y	I/O, L115P_Y	I/O, L115P_Y	I/O, L115P_Y	I/O, L115P
I/O, L#N_Y	7	G3	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L108N_Y	I/O, L115N_Y	I/O, L115N_Y	I/O, L115N_Y	I/O, L115N
I/O, L#P_Y	7	G2	XC2S100E, 150E, 300E, 600E	XC2S600E	I/O, L82P_Y	I/O, L107P_Y	I/O, L114P	I/O, L114P_Y	I/O, L114P	I/O, VREF Bank 7, L114P_Y
I/O, L#N_Y	7	G1	XC2S100E, 150E, 300E, 600E	-	I/O, L82N_Y	I/O, L107N_Y	I/O, L114N	I/O, L114N_Y	I/O, L114N	I/O, L114N_Y

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
M0	-	AA1	-	-	M0	M0	M0	M0	M0	M0
M2	-	AB2	-	-	M2	M2	M2	M2	M2	M2
I/O, L#N_Y	5	AA3	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L84N_Y	I/O, L89N_Y	I/O, L89N_Y	I/O, L89N_Y	I/O, L89N_Y
I/O, L#P_Y	5	AB3	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L84P_Y	I/O, L89P_Y	I/O, L89P_Y	I/O, L89P_Y	I/O, L89P_Y
I/O	5	AB4	-	-	-	-	-	I/O	I/O	I/O
I/O	5	AA5	XC2S100E, 150E	-	I/O, L63N_Y	I/O, L83N_Y	I/O	I/O	I/O	I/O
I/O, L#N_Y	5	W5	XC2S100E, 150E, 200E, 300E, 400E, 600E	-	I/O, L63P_Y	I/O, L83P_Y	I/O, L88N_Y	I/O, L88N_Y	I/O, L88N_Y	I/O, L88N_Y
I/O, L#P_Y	5	Y5	XC2S200E, 300E, 400E, 600E	-	I/O	I/O	I/O, L88P_Y	I/O, L88P_Y	I/O, L88P_Y	I/O, L88P_Y
I/O, L#N_Y	5	AB5	XC2S100E, 200E, 300E, 400E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L62N_Y	I/O, L82N	I/O, VREF Bank 5, L87N_Y	I/O, VREF Bank 5, L87N_Y	I/O, VREF Bank 5, L87N_Y	I/O, VREF Bank 5, L87N_Y
I/O, L#P_Y	5	AB6	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L62P_Y	I/O, L82P	I/O, L87P_Y	I/O, L87P_Y	I/O, L87P_Y	I/O, L87P_Y
I/O	5	Y6	-	-	-	-	-	I/O	I/O	I/O
I/O	5	AA6	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N_YY	5	V6	All	-	I/O, L61N_YY	I/O, L81N_YY	I/O, L86N_YY	I/O, L86N_YY	I/O, L86N_YY	I/O, L86N_YY
I/O, L#P_YY	5	W6	All	-	I/O, L61P_YY	I/O, L81P_YY	I/O, L86P_YY	I/O, L86P_YY	I/O, L86P_YY	I/O, L86P_YY
I/O, VREF Bank 5, L#N_YY	5	AB7	All	All	I/O, VREF Bank 5, L60N_YY	I/O, VREF Bank 5, L80N_YY	I/O, VREF Bank 5, L85N_YY	I/O, VREF Bank 5, L85N_YY	I/O, VREF Bank 5, L85N_YY	I/O, VREF Bank 5, L85N_YY
I/O, L#P_YY	5	AA7	All	-	I/O, L60P_YY	I/O, L80P_YY	I/O, L85P_YY	I/O, L85P_YY	I/O, L85P_YY	I/O, L85P_YY
I/O	5	Y7	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N_Y	5	V7	XC2S300E, 600E	-	-	I/O, L79N	I/O, L84N	I/O, L84N_Y	I/O, L84N	I/O, L84N_Y
I/O, L#P_Y	5	W7	XC2S300E, 600E	-	I/O	I/O, L79P	I/O, L84P	I/O, L84P_Y	I/O, L84P	I/O, L84P_Y
I/O, L#N_Y	5	AB8	XC2S100E, 300E, 600E	XC2S600E	I/O, L59N_Y	I/O, L78N	I/O, L83N	I/O, L83N_Y	I/O, L83N	I/O, VREF Bank 5, L83N_Y
I/O, L#P_Y	5	AA8	XC2S100E, 300E, 600E	-	I/O, L59P_Y	I/O, L78P	I/O, L83P	I/O, L83P_Y	I/O, L83P	I/O, L83P_Y
I/O	5	Y8	-	-	-	-	-	I/O	I/O	I/O

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O, VREF Bank 5, L#N_Y	5	V8	XC2S100E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 5, L58N_Y	I/O, VREF Bank 5, L77N	I/O, VREF Bank 5, L82N_Y	I/O, VREF Bank 5, L82N_Y	I/O, VREF Bank 5, L82N_Y	I/O, VREF Bank 5, L82N_Y
I/O, L#P_Y	5	W8	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L58P_Y	I/O, L77P	I/O, L82P_Y	I/O, L82P_Y	I/O, L82P_Y	I/O, L82P_Y
I/O, L#N_Y	5	AB9	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L57N_Y	I/O, L76N	I/O, L81N_Y	I/O, L81N_Y	I/O, L81N_Y	I/O, L81N_Y
I/O, L#P_Y	5	AA9	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L57P_Y	I/O, L76P	I/O, L81P_Y	I/O, L81P_Y	I/O, L81P_Y	I/O, L81P_Y
I/O	5	AB10	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#N_Y	5	W9	XC2S150E, 300E, 400E, 600E	-	-	I/O, L75N_Y	I/O, L80N	I/O, L80N_Y	I/O, L80N_Y	I/O, L80N_Y
I/O, L#P_Y	5	Y9	XC2S100E, 150E, 300E, 400E, 600E	-	I/O, L56N_Y	I/O, L75P_Y	I/O, L80P	I/O, L80P_Y	I/O, L80P_Y	I/O, L80P_Y
I/O, L#N_Y	5	V9	XC2S100E, 150E, 300E, 400E, 600E	-	I/O, L56P_Y	I/O, L74N_Y	I/O, L79N	I/O, L79N_Y	I/O, L79N_Y	I/O, L79N_Y
I/O, L#P_Y	5	U9	XC2S150E, 300E, 400E, 600E	-	-	I/O, L74P_Y	I/O, L79P	I/O, L79P_Y	I/O, L79P_Y	I/O, L79P_Y
I/O	5	AA10	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#N_Y	5	W10	XC2S200E, 300E, 400E, 600E	-	I/O, L55N	I/O, L73N	I/O, L78N_Y	I/O, L78N_Y	I/O, L78N_Y	I/O, L78N_Y
I/O, L#P_Y	5	Y10	XC2S200E, 300E, 400E, 600E	-	I/O, L55P	I/O, L73P	I/O, L78P_Y	I/O, L78P_Y	I/O, L78P_Y	I/O, L78P_Y
I/O, VREF Bank 5, L#N_Y	5	V10	XC2S200E, 300E, 400E, 600E	All	I/O, VREF Bank 5, L54N	I/O, VREF Bank 5, L72N	I/O, VREF Bank 5, L77N_Y	I/O, VREF Bank 5, L77N_Y	I/O, VREF Bank 5, L77N_Y	I/O, VREF Bank 5, L77N_Y
I/O, L#P_Y	5	U10	XC2S200E, 300E, 400E, 600E	-	I/O, L54P	I/O, L72P	I/O, L77P_Y	I/O, L77P_Y	I/O, L77P_Y	I/O, L77P_Y
I/O	5	U11	-	-	-	-	-	I/O	I/O	I/O
I/O	5	V11	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#N	5	W11	XC2S200E, 400E	-	I/O	I/O, L71N	I/O, L76N_Y	I/O, L76N	I/O, L76N_Y	I/O, L76N
I/O, L#P	5	Y11	XC2S200E, 400E	XC2S400E, 600E	-	I/O, L71P	I/O, L76P_Y	I/O, L76P	I/O, VREF Bank 5, L76P_Y	I/O, VREF Bank 5, L76P
I/O	5	AA11	-	-	-	-	-	I/O	I/O	I/O
I/O (DLL), L#N	5	AB11	-	-	I/O (DLL), L53N	I/O (DLL), L70N	I/O (DLL), L75N	I/O (DLL), L75N	I/O (DLL), L75N	I/O (DLL), L75N
GCK1, I	5	AB12	-	-	GCK1, I	GCK1, I	GCK1, I	GCK1, I	GCK1, I	GCK1, I

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
GCK0, I	4	AA12	-	-	GCK0, I	GCK0, I	GCK0, I	GCK0, I	GCK0, I	GCK0, I
I/O (DLL), L#P	4	Y12	-	-	I/O (DLL), L53P	I/O (DLL), L70P	I/O (DLL), L75P	I/O (DLL), L75P	I/O (DLL), L75P	I/O (DLL), L75P
I/O	4	W12	-	-	-	-	-	I/O	I/O	I/O
I/O, L#N	4	V12	XC2S150E, 300E, 600E	-	-	I/O, L69N_Y	I/O, L74N	I/O, L74N_Y	I/O, L74N	I/O, L74N_Y
I/O, L#P	4	U12	XC2S150E, 300E, 600E	XC2S400E, 600E	I/O, L52N	I/O, L69P_Y	I/O, L74P	I/O, L74P_Y	I/O, VREF Bank 4, L74P	I/O, VREF Bank 4, L74P_Y
I/O, L#N	4	AB13	XC2S300E, 600E	-	I/O, L52P	I/O	I/O, L73N	I/O, L73N_Y	I/O, L73N	I/O, L73N_Y
I/O, L#P	4	AA13	XC2S300E, 600E	-	-	-	I/O, L73P	I/O, L73P_Y	I/O, L73P	I/O, L73P_Y
I/O	4	Y13	-	-	-	-	-	I/O	I/O	I/O
I/O, L#N	4	W13	XC2S200E, 300E, 400E, 600E	-	I/O, L51N	I/O, L68N	I/O, L72N_Y	I/O, L72N_Y	I/O, L72N_Y	I/O, L72N_Y
I/O, VREF Bank 4, L#P	4	V13	XC2S200E, 300E, 400E, 600E	All	I/O, VREF Bank 4, L51P	I/O, VREF Bank 4, L68P	I/O, VREF Bank 4, L72P_Y	I/O, VREF Bank 4, L72P_Y	I/O, VREF Bank 4, L72P_Y	I/O, VREF Bank 4, L72P_Y
I/O	4	U13	-	-	I/O, L50N	I/O, L67N	I/O	I/O	I/O	I/O
I/O, L#N	4	AB14	-	-	I/O, L50P	I/O, L67P	I/O, L71N	I/O, L71N	I/O, L71N	I/O, L71N
I/O, L#P	4	AA14	-	-	-	-	I/O, L71P	I/O, L71P	I/O, L71P	I/O, L71P
I/O	4	AB15	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#N	4	Y14	XC2S100E, 150E, 200E	-	I/O, L49N_Y	I/O, L66N_Y	I/O, L70N_Y	I/O, L70N	I/O, L70N	I/O, L70N
I/O, L#P	4	W14	XC2S100E, 150E, 200E	-	I/O, L49P_Y	I/O, L66P_Y	I/O, L70P_Y	I/O, L70P	I/O, L70P	I/O, L70P
I/O, L#N	4	U14	XC2S150E, 200E	-	-	I/O, L65N_Y	I/O, L69N_Y	I/O, L69N	I/O, L69N	I/O, L69N
I/O, L#P	4	V14	XC2S150E, 200E	-	-	I/O, L65P_Y	I/O, L69P_Y	I/O, L69P	I/O, L69P	I/O, L69P
I/O, L#N	4	AA15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L48N_Y	I/O, L64N	I/O, L68N_Y	I/O, L68N_Y	I/O, L68N_Y	I/O, L68N_Y
I/O, L#P	4	Y15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L48P_Y	I/O, L64P	I/O, L68P_Y	I/O, L68P_Y	I/O, L68P_Y	I/O, L68P_Y
I/O, L#N	4	W15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L47N_Y	I/O, L63N	I/O, L67N_Y	I/O, L67N_Y	I/O, L67N_Y	I/O, L67N_Y
I/O, VREF Bank 4, L#P	4	V15	XC2S100E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 4, L47P_Y	I/O, VREF Bank 4, L63P	I/O, VREF Bank 4, L67P_Y	I/O, VREF Bank 4, L67P_Y	I/O, VREF Bank 4, L67P_Y	I/O, VREF Bank 4, L67P_Y
I/O	4	AB16	-	-	-	-	-	I/O	I/O	I/O
I/O	4	AB17	-	-	I/O	I/O	I/O	I/O	I/O	I/O

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O	0	F11	-	XC2S400E, 600E	-	-	I/O	I/O	I/O, VREF Bank 0	I/O, VREF Bank 0
I/O, L#P	0	A10	XC2S300E, 600E	-	I/O	I/O, L11P	I/O, L12P	I/O, L12P_Y	I/O, L12P	I/O,L12P_Y
I/O, L#N	0	B10	XC2S300E, 600E	-	-	I/O, L11N	I/O, L12N	I/O, L12N_Y	I/O, L12N	I/O, L12N_Y
I/O	0	E11	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P	0	C10	XC2S200E, 300E, 400E, 600E	-	I/O, L8P	I/O, L10P	I/O, L11P_Y	I/O, L11P_Y	I/O,L11P_Y	I/O,L11P_Y
I/O, VREF Bank 0, L#N	0	D10	XC2S200E, 300E, 400E, 600E	All	I/O, VREF Bank 0, L8N	I/O, VREF Bank 0, L10N	I/O, VREF Bank 0, L11N_Y	I/O, VREF Bank 0, L11N_Y	I/O, VREF Bank 0, L11N_Y	I/O, VREF Bank 0, L11N_Y
I/O	0	F10	-	-	I/O, L7P	I/O	I/O	I/O	I/O	I/O
I/O, L#P	0	A9	-	-	I/O, L7N	I/O	I/O, L10P	I/O, L10P	I/O, L10P	I/O, L10P
I/O, L#N	0	B9	-	-	-	-	I/O, L10N	I/O, L10N	I/O, L10N	I/O, L10N
I/O	0	E10	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#P	0	C9	XC2S100E, 150E, 200E	-	I/O, L6P_Y	I/O, L9P_Y	I/O, L9P_Y	I/O, L9P	I/O, L9P	I/O, L9P
I/O, L#N	0	D9	XC2S100E, 150E, 200E	-	I/O, L6N_Y	I/O, L9N_Y	I/O, L9N_Y	I/O, L9N	I/O, L9N	I/O, L9N
I/O, L#P	0	F9	XC2S150E, 200E	-	-	I/O, L8P_Y	I/O, L8P_Y	I/O, L8P	I/O, L8P	I/O, L8P
I/O, L#N	0	E9	XC2S150E, 200E	-	-	I/O, L8N_Y	I/O, L8N_Y	I/O, L8N	I/O, L8N	I/O, L8N
I/O, L#P	0	A8	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L5P_Y	I/O, L7P	I/O, L7P_Y	I/O, L7P_Y	I/O, L7P_Y	I/O, L7P_Y
I/O, L#N	0	B8	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L5N_Y	I/O, L7N	I/O, L7N_Y	I/O, L7N_Y	I/O, L7N_Y	I/O, L7N_Y
I/O, L#P	0	C8	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L4P_Y	I/O, L6P	I/O, L6P_Y	I/O, L6P_Y	I/O, L6P_Y	I/O, L6P_Y
I/O, VREF Bank 0, L#N	0	D8	XC2S100E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 0, L4N_Y	I/O, VREF Bank 0, L6N	I/O, VREF Bank 0, L6N_Y	I/O, VREF Bank 0, L6N_Y	I/O, VREF Bank 0, L6N_Y	I/O, VREF Bank 0, L6N_Y
I/O	0	A7	-	-	-	-	-	I/O	I/O	I/O
I/O	0	B7	-	-	I/O	I/O	I/O	I/O	I/O	I/O
I/O, L#P	0	C7	XC2S150E, 200E	XC2S600E	I/O, L3P	I/O, L5P_Y	I/O, L5P_Y	I/O, L5P	I/O, L5P	I/O, VREF Bank 0, L5P
I/O, L#N	0	D7	XC2S150E, 200E	-	I/O, L3N	I/O, L5N_Y	I/O, L5N_Y	I/O, L5N	I/O, L5N	I/O, L5N
I/O, L#P	0	E8	XC2S150E, 200E	-	-	I/O, L4P_Y	I/O, L4P_Y	I/O, L4P	I/O, L4P	I/O, L4P
I/O, L#N	0	E7	XC2S150E, 200E	-	-	I/O, L4N_Y	I/O, L4N_Y	I/O, L4N	I/O, L4N	I/O, L4N

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L201P	7	E4	XC2S400E	-	I/O, L201P_Y	I/O, L201P
I/O, L201N	7	F5	XC2S400E	-	I/O, L201N_Y	I/O, L201N
I/O, VREF Bank 7, L200P	7	F4	XC2S600E	All	I/O, VREF Bank 7, L200P	I/O, VREF Bank 7, L200P_Y
I/O, L200N	7	F3	XC2S600E	-	I/O, L200N	I/O, L200N_Y
I/O, L199P	7	F2	XC2S600E	-	-	I/O, L199P_Y
I/O, L199N	7	F1	XC2S600E	-	I/O	I/O, L199N_Y
I/O, L198P	7	G6	XC2S400E	-	I/O, L198P_Y	I/O, L198P
I/O, L198N	7	G5	XC2S400E	-	I/O, L198N_Y	I/O, L198N
I/O, L197P	7	G4	XC2S600E	-	I/O, L197P	I/O, L197P_Y
I/O, L197N	7	G3	XC2S600E	-	I/O, L197N	I/O, L197N_Y
I/O, VREF Bank 7, L196P_YY	7	G2	All	All	I/O, VREF Bank 7, L196P_YY	I/O, VREF Bank 7, L196P_YY
I/O, L196N_YY	7	G1	All	-	I/O, L196N_YY	I/O, L196N_YY
I/O	7	H7	-	-	I/O	I/O
I/O, L195P_YY	7	H6	All	-	I/O, L195P_YY	I/O, L195P_YY
I/O, L195N_YY	7	H5	All	-	I/O, L195N_YY	I/O, L195N_YY
I/O	7	J8	-	-	-	I/O
I/O, L194P	7	H2	XC2S400E	-	I/O, L194P_Y	I/O, L194P
I/O, L194N	7	H1	XC2S400E	-	I/O, L194N_Y	I/O, L194N
I/O, L193P	7	J7	XC2S600E	XC2S600E	I/O	I/O, VREF Bank 7, L193P_Y
I/O, L193N	7	J6	XC2S600E	-	-	I/O, L193N_Y
I/O	7	J5	-	-	I/O	I/O
I/O, L192P_YY	7	J4	All	-	I/O, L192P_YY	I/O, L192P_YY
I/O, L192N_YY	7	J3	All	-	I/O, L192N_YY	I/O, L192N_YY
I/O	7	K5	-	-	I/O	I/O
I/O, VREF Bank 7, L191P_YY	7	J2	All	All	I/O, VREF Bank 7, L191P_YY	I/O, VREF Bank 7, L191P_YY
I/O, L191N_YY	7	J1	All	-	I/O, L191N_YY	I/O, L191N_YY
I/O, L190P_YY	7	K8	All	-	I/O, L190P_YY	I/O, L190P_YY
I/O, L190N_YY	7	K7	All	-	I/O, L190N_YY	I/O, L190N_YY
I/O	7	K4	-	-	-	I/O
I/O, L189P_YY	7	K3	All	-	I/O, L189P_YY	I/O, L189P_YY
I/O, L189N_YY	7	K2	All	-	I/O, L189N_YY	I/O, L189N_YY
I/O	7	K1	-	-	-	I/O

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
GCK0, I	4	AF14	-	-	GCK0, I	GCK0, I
I/O (DLL), L126P	4	AE14	-	-	I/O (DLL), L126P	I/O (DLL), L126P
I/O	4	AD14	-	-	-	I/O
I/O, L125N	4	AC14	-	-	I/O, L125N	I/O, L125N
I/O, L125P	4	AB14	-	-	I/O, L125P	I/O, L125P
I/O	4	AC15	-	-	-	I/O
I/O, L124N	4	AA14	XC2S600E	-	I/O, L124N	I/O, L124N_Y
I/O, VREF Bank 4, L124P	4	Y14	XC2S600E	All	I/O, VREF Bank 4, L124P	I/O, VREF Bank 4, L124P_Y
I/O, L123N	4	AF15	XC2S600E	-	I/O, L123N	I/O, L123N_Y
I/O, L123P	4	AE15	XC2S600E	-	I/O, L123P	I/O, L123P_Y
I/O	4	AB15	-	-	-	I/O
I/O, L122N_YY	4	AA15	All	-	I/O, L122N_YY	I/O, L122N_YY
I/O, L122P_YY	4	Y15	All	-	I/O, L122P_YY	I/O, L122P_YY
I/O	4	AF16	-	-	-	I/O
I/O, L121N_YY	4	W15	All	-	I/O, L121N_YY	I/O, L121N_YY
I/O, VREF Bank 4, L121P_YY	4	V15	All	All	I/O, VREF Bank 4, L121P_YY	I/O, VREF Bank 4, L121P_YY
I/O, L120N_YY	4	AE16	All	-	I/O, L120N_YY	I/O, L120N_YY
I/O, L120P_YY	4	AD16	All	-	I/O, L120P_YY	I/O, L120P_YY
I/O	4	AB16	-	-	-	I/O
I/O, L119N	4	AA16	-	-	I/O, L119N	I/O, L119N
I/O, L119P	4	Y16	-	-	I/O, L119P	I/O, L119P
I/O	4	W16	-	-	-	I/O
I/O, L118N_YY	4	AF17	All	-	I/O, L118N_YY	I/O, L118N_YY
I/O, L118P_YY	4	AE17	All	-	I/O, L118P_YY	I/O, L118P_YY
I/O, L117N_YY	4	AD17	All	-	I/O, L117N_YY	I/O, L117N_YY
I/O, L117P_YY	4	AC17	All	-	I/O, L117P_YY	I/O, L117P_YY
I/O	4	AB17	-	-	-	I/O
I/O, L116N	4	Y17	XC2S600E	-	I/O, L116N	I/O, L116N_Y
I/O, L116P	4	W17	XC2S600E	-	I/O, L116P	I/O, L116P_Y
I/O	4	AF18	-	-	-	I/O
I/O, L115N_YY	4	AE18	All	-	I/O, L115N_YY	I/O, L115N_YY
I/O, L115P_YY	4	AD18	All	-	I/O, L115P_YY	I/O, L115P_YY

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O	4	AC18	-	-	I/O	I/O
I/O, VREF Bank 4, L114N	4	AB18	-	All	I/O, VREF Bank 4, L114N	I/O, VREF Bank 4, L114N
I/O, L114P	4	AA18	-	-	I/O, L114P	I/O, L114P
I/O, L113N	4	Y18	-	-	I/O, L113N	I/O, L113N
I/O, L113P	4	W18	-	-	I/O, L113P	I/O, L113P
I/O	4	AB19	-	-	I/O	I/O
I/O, L112N	4	AF19	XC2S600E	-	I/O	I/O, L112N_Y
I/O, L112P	4	AE19	XC2S600E	XC2S600E	-	I/O, VREF Bank 4, L112P_Y
I/O, L111N	4	AA19	XC2S600E	-	I/O, L111N	I/O, L111N_Y
I/O, L111P	4	Y19	XC2S600E	-	I/O, L111P	I/O, L111P_Y
I/O	4	AF20	-	-	-	I/O
I/O, L110N	4	AE20	XC2S600E	-	I/O, L110N	I/O, L110N_Y
I/O, L110P	4	AD20	XC2S600E	-	I/O, L110P	I/O, L110P_Y
I/O	4	AC20	-	-	I/O	I/O
I/O, L109N_YY	4	AB20	All	-	I/O, L109N_YY	I/O, L109N_YY
I/O, VREF Bank 4, L109P_YY	4	AA20	All	All	I/O, VREF Bank 4, L109P_YY	I/O, VREF Bank 4, L109P_YY
I/O	4	Y20	-	-	I/O	I/O
I/O, L108N	4	AF21	-	-	I/O, L108N	I/O, L108N
I/O, L108P	4	AE21	-	-	I/O, L108P	I/O, L108P
I/O, L107N	4	AD21	-	-	I/O, L107N	I/O, L107N
I/O, L107P	4	AC21	-	-	I/O, L107P	I/O, L107P
I/O	4	AC22	-	-	-	I/O
I/O, L106N_YY	4	AF22	All	-	I/O, L106N_YY	I/O, L106N_YY
I/O, VREF Bank 4, L106P_YY	4	AE22	All	All	I/O, VREF Bank 4, L106P_YY	I/O, VREF Bank 4, L106P_YY
I/O, L105N_YY	4	AB21	All	-	I/O, L105N_YY	I/O, L105N_YY
I/O, L105P_YY	4	AA21	All	-	I/O, L105P_YY	I/O, L105P_YY
I/O, L104N_YY	4	AF23	All	-	I/O, L104N_YY	I/O, L104N_YY
I/O, L104P_YY	4	AE23	All	-	I/O, L104P_YY	I/O, L104P_YY
I/O, L103N	4	AD23	XC2S600E	-	I/O	I/O, L103N_Y
I/O, L103P	4	AE24	XC2S600E	-	-	I/O, L103P_Y
I/O, L102N_YY	4	AF24	All	-	I/O, L102N_YY	I/O, L102N_YY
I/O, L102P_YY	4	AF25	All	-	I/O, L102P_YY	I/O, L102P_YY

Additional FG676 Package Pins *(Continued)*

GND Pins						
A1	A26	B2	B25	C3	C12	C15
C24	D4	D8	D19	D23	F10	F17
H4	H23	K6	K21	L11	L12	L13
L14	L15	L16	M3	M11	M12	M13
M14	M15	M16	M24	N11	N12	N13
N14	N15	N16	P11	P12	P13	P14
P15	P16	R3	R11	R12	R13	R14
R15	R16	R24	T11	T12	T13	T14
T15	T16	U6	U21	W4	W23	AA10
AA17	AC4	AC8	AC19	AC23	AD3	AD12
AD15	AD24	AE2	AE25	AF1	AF26	-
Not Connected Pins (XC2S400E Only)						
A12	A16	A23	B3	C1	C2	C10
C11	C25	D2	D15	D18	D24	D25
E7	E13	E19	F2	F6	F8	F12
F20	F22	G10	G14	G15	G16	G26
H10	H13	H16	H25	J6	J8	J12
J13	K1	K4	K22	K24	L3	L19
L22	L26	M4	M9	M22	N1	N4
N9	N18	N19	N23	P4	P5	P18
P19	P24	R4	R7	R19	T3	T24
U1	U4	U7	U24	U25	V8	V12
V13	V21	W12	W13	W14	W16	Y3
Y7	Y21	AA7	AA9	AA22	AB15	AB16
AB17	AB22	AC1	AC15	AC22	AC25	AC26
AD1	AD2	AD10	AD11	AD13	AD14	AE5
AE19	AE24	AF4	AF16	AF18	AF20	-