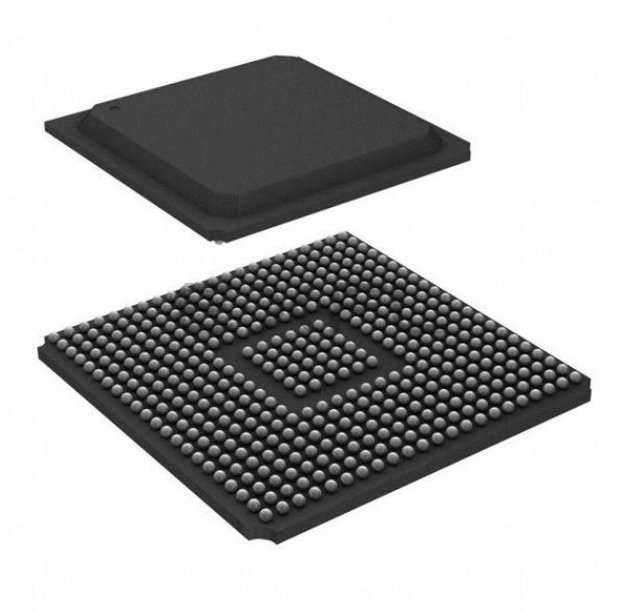
AMD Xilinx - XC2S400E-6FGG456C Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2400
Number of Logic Elements/Cells	10800
Total RAM Bits	163840
Number of I/O	329
Number of Gates	400000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s400e-6fgg456c

Spartan-IIE FPGA Family: Introduction and Ordering Information

DS077-1 (v3.0) August 9, 2013

Product Specification

Introduction

The Spartan®-IIE Field-Programmable Gate Array family gives users high performance, abundant logic resources, and a rich feature set, all at an exceptionally low price. The seven-member family offers densities ranging from 50,000 to 600,000 system gates, as shown in Table 1. System performance is supported beyond 200 MHz.

Features include block RAM (to 288K bits), distributed RAM (to 221,184 bits), 19 selectable I/O standards, and four DLLs (Delay-Locked Loops). Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

The Spartan-IIE family is a superior alternative to mask-programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary (impossible with ASICs).

Features

- Second generation ASIC replacement technology
  - Densities as high as 15,552 logic cells with up to 600,000 system gates
  - Streamlined features based on Virtex®-E FPGA architecture
  - Unlimited in-system reprogrammability
  - Very low cost
  - Cost-effective 0.15 micron technology
- System level features
  - SelectRAM™ hierarchical memory:
    - 16 bits/LUT distributed RAM
    - Configurable 4K-bit true dual-port block RAM
    - Fast interfaces to external RAM
  - Fully 3.3V PCI compliant to 64 bits at 66 MHz and CardBus compliant
  - Low-power segmented routing architecture
  - Dedicated carry logic for high-speed arithmetic
  - Efficient multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with enable, set, reset
  - Four dedicated DLLs for advanced clock control
    - Eliminate clock distribution delay
    - Multiply, divide, or phase shift
  - Four primary low-skew global clock distribution nets
  - IEEE 1149.1 compatible boundary scan logic
- Versatile I/O and packaging
  - Pb-free package options
  - Low-cost packages available in all densities
  - Family footprint compatibility in common packages
  - 19 high-performance interface standards
    - LVTTL, LVCMOS, HSTL, SSTL, AGP, CTT, GTL
    - LVDS and LVPECL differential I/O
  - Up to 205 differential I/O pairs that can be input, output, or bidirectional
  - Hot swap I/O (CompactPCI friendly)
- Core logic powered at 1.8V and I/Os powered at 1.5V, 2.5V, or 3.3V
- Fully supported by powerful Xilinx® ISE® development system
  - Fully automatic mapping, placement, and routing
  - Integrated with design entry and verification tools
  - Extensive IP library including DSP functions and soft processors

Table 1: **Spartan-IIE FPGA Family Members**

Device	Logic Cells	Typical System Gate Range (Logic and RAM)	CLB Array (R x C)	Total CLBs	Maximum Available User I/O(1)	Maximum Differential I/O Pairs	Distributed RAM Bits	Block RAM Bits
XC2S50E	1,728	23,000 - 50,000	16 x 24	384	182	83	24,576	32K
XC2S100E	2,700	37,000 - 100,000	20 x 30	600	202	86	38,400	40K
XC2S150E	3,888	52,000 - 150,000	24 x 36	864	265	114	55,296	48K
XC2S200E	5,292	71,000 - 200,000	28 x 42	1,176	289	120	75,264	56K
XC2S300E	6,912	93,000 - 300,000	32 x 48	1,536	329	120	98,304	64K
XC2S400E	10,800	145,000 - 400,000	40 x 60	2,400	410	172	153,600	160K
XC2S600E	15,552	210,000 - 600,000	48 x 72	3,456	514	205	221,184	288K

Notes:

1. User I/O counts include the four global clock/user input pins. See details in Table 2, page 5

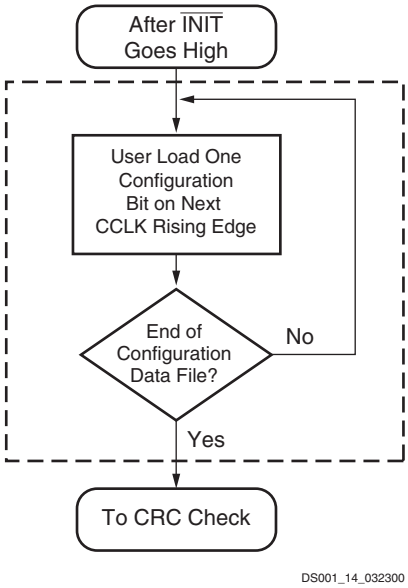


Figure 18: **Loading Serial Mode Configuration Data**

Slave Serial Mode

In Slave Serial mode, the FPGA's CCLK pin is driven by an external source, allowing the FPGA to be configured from other logic devices such as microprocessors or in a daisy-chain configuration. Figure 19 shows connections for a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-IIE device in slave serial mode should be connected as shown for the third device from the left. Slave Serial mode is selected by a <11x> on the mode pins (M0, M1, M2). The weak pull-ups on the mode pins make slave serial the default mode if the pins are left unconnected.

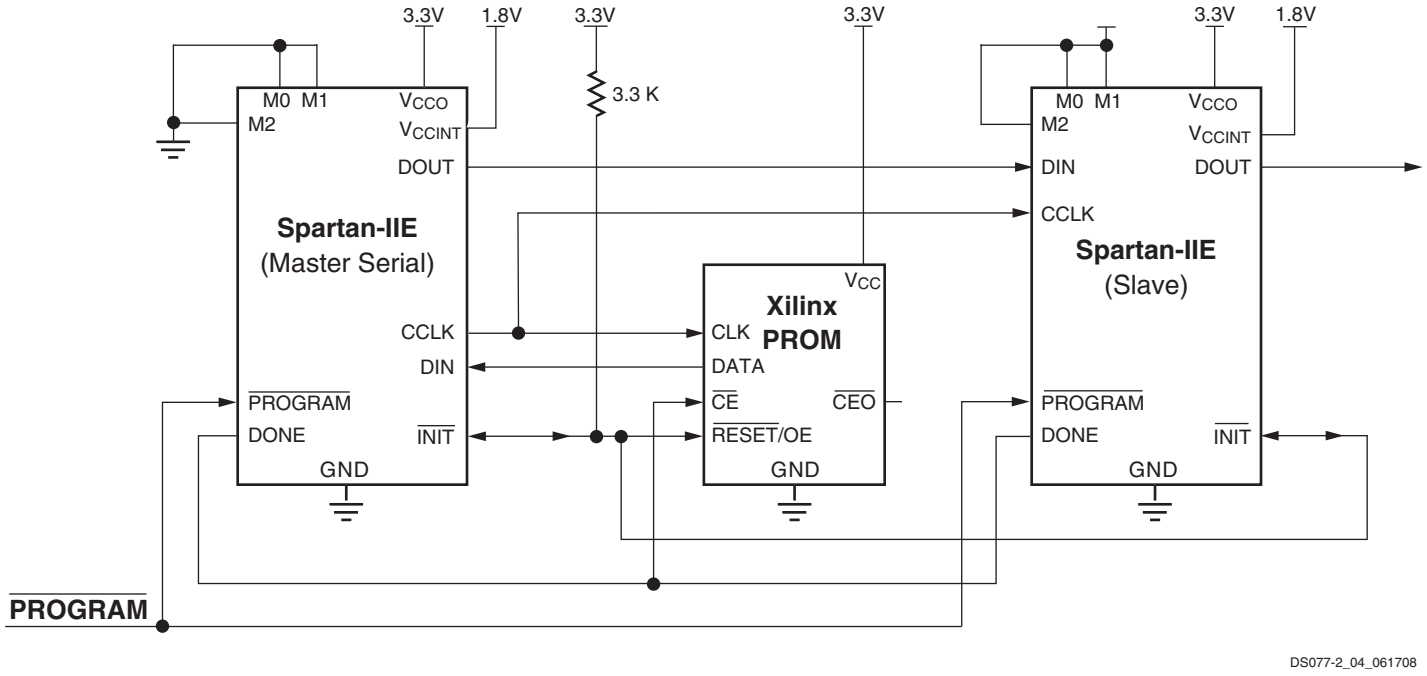
The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

Timing for Slave Serial mode is shown in Figure 24, page 49.

Daisy Chain

Multiple FPGAs in Slave Serial mode can be daisy-chained for configuration from a single source. After an FPGA is configured, data for the next device is sent to the DOUT pin. Data on the DOUT pin changes on the rising edge of CCLK. Note that DOUT changes on the falling edge of CCLK for some Xilinx families but mixed daisy chains are allowed. Configuration must be delayed until $\overline{\text{INIT}}$ pins of all daisy-chained FPGAs are High. For more information, see Start-up, page 23.

The maximum amount of data that can be sent to the DOUT pin for a serial daisy chain is 2^{20}-1 (1,048,575) 32-bit words, or 33,554,400 bits, which is approximately 8 XC2S600E bitstreams. The configuration bitstream of downstream devices is limited to this size.



Notes:
1. If the DriveDone configuration option is not active for any of the FPGAs, pull up DONE with a 330Ω resistor.

Figure 19: **Master/Slave Serial Configuration Circuit Diagram**

IOB Output Delay Adjustments for Different Standards(1)

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade		Units
			-7	-6	
Output Delay Adjustments (Adj)					
T_{OLVTTL_S2}	Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, C_{SL})	LVTTL, Slow, 2 mA	14.7	14.7	ns
T_{OLVTTL_S4}		4 mA	7.5	7.5	ns
T_{OLVTTL_S6}		6 mA	4.8	4.8	ns
T_{OLVTTL_S8}		8 mA	3.0	3.0	ns
T_{OLVTTL_S12}		12 mA	1.9	1.9	ns
T_{OLVTTL_S16}		16 mA	1.7	1.7	ns
T_{OLVTTL_S24}		24 mA	1.3	1.3	ns
T_{OLVTTL_F2}		LVTTL, Fast, 2 mA	13.1	13.1	ns
T_{OLVTTL_F4}		4 mA	5.3	5.3	ns
T_{OLVTTL_F6}		6 mA	3.1	3.1	ns
T_{OLVTTL_F8}		8 mA	1.0	1.0	ns
T_{OLVTTL_F12}		12 mA	0	0	ns
T_{OLVTTL_F16}		16 mA	–0.05	–0.05	ns
T_{OLVTTL_F24}		24 mA	–0.20	–0.20	ns
$T_{OLVCMOS2}$		LVCMOS2	0.09	0.09	ns
$T_{OLVCMOS18}$		LVCMOS18	0.7	0.7	ns
T_{OLVDS}		LVDS	–1.2	–1.2	ns
$T_{OLVPECL}$		LVPECL	–0.41	–0.41	ns
T_{OPCI33_3}		PCI, 33 MHz, 3.3V	2.3	2.3	ns
T_{OPCI66_3}		PCI, 66 MHz, 3.3V	–0.41	–0.41	ns
T_{OGTL}		GTL	0.49	0.49	ns
T_{OGTLP}		GTL+	0.8	0.8	ns
T_{OHSTL_I}		HSTL I	–0.51	–0.51	ns
T_{OHSTL_III}		HSTL III	–0.91	–0.91	ns
T_{OHSTL_IV}		HSTL IV	–1.01	–1.01	ns
T_{OSSTL2_I}		SSTL2 I	–0.51	–0.51	ns
T_{OSSLT2_II}		SSTL2 II	–0.91	–0.91	ns
T_{OSSTL3_I}		SSTL3 I	–0.51	–0.51	ns
T_{OSSTL3_II}		SSTL3 II	–1.01	–1.01	ns
T_{OCTT}		CTT	–0.61	–0.61	ns
T_{OAGP}		AGP	–0.91	–0.91	ns

Notes:

1. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see the tables Constants for Calculating T_{IOOP} and Delay Measurement Methodology, page 41.

Pin Definitions *(Continued)*

Pad Name	Dedicated Pin	Direction	Description
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In Slave Parallel mode, D0-D7 are configuration data input pins. During readback, D0-D7 are output pins. These pins become user I/Os after configuration unless the Slave Parallel port is retained. In serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
$\overline{WRITE}$	No	Input	In Slave Parallel mode, the active-low Write Enable signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
$\overline{CS}$	No	Input	In Slave Parallel mode, the active-low Chip Select signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary Scan Test Access Port pins (IEEE 1149.1).
V_{CCINT}	Yes	Input	1.8V power supply pins for the internal core logic.
V_{CCO}	Yes	Input	Power supply pins for output drivers (1.5V, 1.8V, 2.5V, or 3.3V subject to banking rules in the Functional Description module.
V_{REF}	No	Input	Input threshold reference voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules in the Functional Description module.
GND	Yes	Input	Ground. All must be connected.
IRDY, TRDY	No	See PCI core documentation	These signals can only be accessed when using Xilinx PCI cores. If the cores are not used, these pins are available as user I/Os.
L#[P/N] (e.g., L0P)	No	Bidirectional	Differential I/O with synchronous output. P = positive, N = negative. The number (#) is used to associate the two pins of a differential pair. Becomes a general user I/O when not needed for differential signals.
L#[P/N]_Y (e.g., L0P_Y)	No	Bidirectional	Differential I/O with asynchronous or synchronous output (asynchronous output not compatible for all densities in a package). P = positive, N = negative. The number (#) is used to associate the two pins of a differential pair. Becomes a general user I/O when not needed for differential signals.
L#[P/N]_YY (e.g., L0P_YY)	No	Bidirectional	Differential I/O with asynchronous or synchronous output (compatible for all densities in a package). P = positive, N = negative. The number (#) is used to associate the two pins of a differential pair. Becomes a general user I/O when not needed for differential signals.
I/O	No	Bidirectional	These pins can be configured to be input and/or output after configuration is completed. Unused I/Os are disabled with a weak pull-down resistor. After power-on and before configuration is completed, these pins are either pulled up or left floating according to the Mode pin values. See the DC and Switching Characteristics module for power-on characteristics.

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 6, L39P	6	P45	XC2S100E, 150E	All
I/O, L39N	6	P46	XC2S100E, 150E	-
I/O	6	P47	-	XC2S200E, 300E
I/O, L38P_YY	6	P48	All	-
I/O, L38N_YY	6	P49	All	-
M1	-	P50	-	-
GND	-	P51	-	-
M0	-	P52	-	-
VCCO	-	P53	-	-
M2	-	P54	-	-
I/O, L37N_YY	5	P55	All	-
I/O, L37P_YY	5	P56	All	-
I/O	5	P57	-	XC2S200E, 300E
I/O	5	P58	-	-
I/O, VREF Bank 5, L36N_YY	5	P59	All	All
I/O, L36P_YY	5	P60	All	-
I/O, L35N	5	P61	XC2S50E, 100E, 300E	-
I/O, L35P	5	P62	XC2S50E, 100E, 300E	-
I/O, L34N	5	P63	XC2S50E, 100E, 200E, 300E	XC2S100E, 150E, 200E, 300E
I/O, L34P	5	P64	XC2S50E, 100E, 200E, 300E	-
GND	-	P65	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
VCCO	-	P66	-	-
VCCINT	-	P67	-	-
I/O, L33N	5	P68	XC2S50E, 100E, 200E, 300E	-
I/O, L33P	5	P69	XC2S50E, 100E, 200E, 300E	-
I/O	5	P70	-	-
I/O, L32N	5	P71	XC2S100E, 150E	-
GND	-	P72	-	-
I/O, VREF Bank 5, L32P	5	P73	XC2S100E, 150E	All
I/O	5	P74	-	-
I/O (DLL), L31N	5	P75	-	-
VCCINT	-	P76	-	-
GCK1, I	5	P77	-	-
VCCO	-	P78	-	-
GND	-	P79	-	-
GCK0, I	4	P80	-	-
I/O (DLL), L31P	4	P81	-	-
I/O	4	P82	-	-
I/O, L30N	4	P83	XC2S50E, 200E, 300E	-
I/O, VREF Bank 4, L30P	4	P84	XC2S50E, 200E, 300E	All
GND	-	P85	-	-
I/O, L29N	4	P86	XC2S50E, 200E, 300E	-
I/O, L29P	4	P87	XC2S50E, 200E, 300E	-
I/O, L28N	4	P88	XC2S50E, 100E, 200E, 300E	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L28P	4	P89	XC2S50E, 100E, 200E, 300E	-
VCCINT	-	P90	-	-
VCCO	-	P91	-	-
GND	-	P92	-	-
I/O, L27N	4	P93	XC2S50E, 100E, 200E, 300E	-
I/O, L27P	4	P94	XC2S50E, 100E, 200E, 300E	XC2S100E, 150E, 200E, 300E
I/O	4	P95	-	-
I/O	4	P96	-	-
I/O, L26N_YY	4	P97	All	-
I/O, VREF Bank 4, L26P_YY	4	P98	All	All
I/O	4	P99	-	-
I/O	4	P100	-	XC2S200E, 300E
I/O, L25N_YY	4	P101	All	-
I/O, L25P_YY	4	P102	All	-
GND	-	P103	-	-
DONE	3	P104	-	-
VCCO	-	P105	-	-
$\overline{\text{PROGRAM}}$	-	P106	-	-
I/O ($\overline{\text{INIT}}$), L24N_YY	3	P107	All	-
I/O (D7), L24P_YY	3	P108	All	-
I/O	3	P109	-	XC2S200E, 300E
I/O	3	P110	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 3, L23N	3	P111	XC2S50E, 150E, 200E, 300E	All
I/O, L23P	3	P112	XC2S50E, 150E, 200E, 300E	-
I/O	3	P113	-	-
I/O	3	P114	-	-
I/O, L22N	3	P115	XC2S50E, 300E	XC2S100E, 150E, 200E, 300E
I/O (D6), L22P	3	P116	XC2S50E, 300E	-
GND	-	P117	-	-
VCCO	-	P118	-	-
VCCINT	-	P119	-	-
I/O (D5), L21N_YY	3	P120	All	-
I/O, L21P_YY	3	P121	All	-
I/O, L20N_YY	3	P122	All	-
I/O, L20P_YY	3	P123	All	-
GND	-	P124	-	-
I/O, VREF Bank 3, L19N	3	P125	XC2S50E, 300E	All
I/O (D4), L19P	3	P126	XC2S50E, 300E	-
I/O	3	P127	-	-
VCCINT	-	P128	-	-
I/O (TRDY)	3	P129	-	-
VCCO	-	P130	-	-
GND	-	P131	-	-
I/O (IRDY), L18N_YY	2	P132	All	-
I/O, L18P_YY	2	P133	All	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
TMS	-	B1	-	-
I/O	7	D3	-	-
I/O, L83P	7	C2	XC2S100E, 150E	-
I/O, L83N	7	C1	XC2S100E, 150E	XC2S200E, 300E, 400E
I/O, L82P_YY	7	D2	All	-
I/O, L82N_YY	7	D1	All	-
I/O, VREF Bank 7, L81P	7	E3	XC2S50E, 150E, 200E, 300E, 400E	All
I/O, L81N	7	E4	XC2S50E, 150E, 200E, 300E, 400E	-
I/O, L80P	7	E2	XC2S200E, 400E	-
I/O, L80N	7	E1	XC2S200E, 400E	-
I/O, L79P	7	F4	XC2S50E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L79N	7	F3	XC2S50E, 300E, 400E	-
I/O, L78P_YY	7	F2	All	-
I/O, L78N_YY	7	F1	All	-
I/O, L77P	7	F5	XC2S100E, 150E	-
I/O, L77N	7	G5	XC2S100E, 150E	-
I/O, L76P_YY	7	G3	All	-
I/O, L76N_YY	7	G4	All	-
I/O, VREF Bank 7, L75P	7	G2	XC2S50E, 300E, 400E	All
I/O, L75N	7	G1	XC2S50E, 300E, 400E	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L74P	7	H4	XC2S100E, 150E, 200E	-
I/O, L74N	7	H3	XC2S100E, 150E, 200E	XC2S400E
I/O, L73P_YY	7	H2	All	-
I/O (IRDY), L73N_YY	7	H1	All	-
I/O (TRDY)	6	J4	-	-
I/O, L72P	6	J2	XC2S100E, 150E, 200E, 400E	XC2S400E
I/O, L72N	6	J3	XC2S100E, 150E, 200E, 400E	-
I/O, L71P	6	J1	XC2S50E, 300E, 400E	-
I/O, VREF Bank 6, L71N	6	K1	XC2S50E, 300E, 400E	All
I/O, L70P_YY	6	K2	All	-
I/O, L70N_YY	6	K3	All	-
I/O, L69P	6	L1	XC2S100E, 150E, 400E	-
I/O, L69N	6	L2	XC2S100E, 150E, 400E	-
I/O, L68P_YY	6	K4	All	-
I/O, L68N_YY	6	K5	All	-
I/O, L67P	6	L3	XC2S50E, 300E, 400E	-
I/O, L67N	6	M2	XC2S50E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L66P	6	M1	XC2S150E, 200E, 400E	-
I/O, L66N	6	N1	XC2S150E, 200E, 400E	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L6P	0	C7	XC2S50E, 200E, 300E, 400E	-
I/O, L6N	0	B7	XC2S50E, 200E, 300E, 400E	-
I/O	0	A6	-	-
I/O, L5P	0	B6	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L5N	0	C6	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L4P	0	A5	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L4N	0	B5	XC2S50E, 100E, 200E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L3P	0	D6	XC2S50E, 100E, 300E	-
I/O, L3N	0	E6	XC2S50E, 100E, 300E	-
I/O, L2P_YY	0	D5	All	-
I/O, VREF Bank 0, L2N_YY	0	C5	All	All
I/O, L1P_YY	0	B4	All	-
I/O, L1N_YY	0	C4	All	-
I/O, L0P_YY	0	A4	All	-
I/O, L0N_YY	0	A3	All	XC2S200E, 300E, 400E
I/O	0	B3	-	-
TCK	-	A2	-	-

Notes:
1. Although designated with the _YY suffix in the XC2S50E, XC2S100E, XC2S150E, XC2S200E, and XC2S300E, these differential pairs are not asynchronous in the XC2S400E.
2. There is no pair L37.

FT256 Differential Clock Pins

Clock	Bank	P		N	
		Pin	Name	Pin	Name
GCK0	4	T9	GCK0, I	R9	I/O (DLL), L52P
GCK1	5	T8	GCK1, I	R8	I/O (DLL), L52N
GCK2	1	B8	GCK2, I	A8	I/O (DLL), L8P
GCK3	0	C8	GCK3, I	D8	I/O (DLL), L8N

Additional FT256 Package Pins

VCCINT Pins				
C3	C14	D4	D13	E5
E12	M5	M12	N4	N13
P3	P14	-	-	-
VCCO Bank 0 Pins				
E8	F7	F8	-	-
VCCO Bank 1 Pins				
E9	F9	F10	-	-
VCCO Bank 2 Pins				
G11	H11	H12	-	-
VCCO Bank 3 Pins				
J11	J12	K11	-	-
VCCO Bank 4 Pins				
L9	L10	M9	-	-

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
M0	-	AA1	-	-	M0	M0	M0	M0	M0	M0
M2	-	AB2	-	-	M2	M2	M2	M2	M2	M2
I/O, L#N_Y	5	AA3	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L84N_Y	I/O, L89N_Y	I/O, L89N_Y	I/O, L89N_Y	I/O, L89N_Y
I/O, L#P_Y	5	AB3	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L84P_Y	I/O, L89P_Y	I/O, L89P_Y	I/O, L89P_Y	I/O, L89P_Y
I/O	5	AB4	-	-	-	-	-	I/O	I/O	I/O
I/O	5	AA5	XC2S100E, 150E	-	I/O, L63N_Y	I/O, L83N_Y	I/O	I/O	I/O	I/O
I/O, L#N_Y	5	W5	XC2S100E, 150E, 200E, 300E, 400E, 600E	-	I/O, L63P_Y	I/O, L83P_Y	I/O, L88N_Y	I/O, L88N_Y	I/O, L88N_Y	I/O, L88N_Y
I/O, L#P_Y	5	Y5	XC2S200E, 300E, 400E, 600E	-	I/O	I/O	I/O, L88P_Y	I/O, L88P_Y	I/O, L88P_Y	I/O, L88P_Y
I/O, L#N_Y	5	AB5	XC2S100E, 200E, 300E, 400E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L62N_Y	I/O, L82N	I/O, VREF Bank 5, L87N_Y	I/O, VREF Bank 5, L87N_Y	I/O, VREF Bank 5, L87N_Y	I/O, VREF Bank 5, L87N_Y
I/O, L#P_Y	5	AB6	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L62P_Y	I/O, L82P	I/O, L87P_Y	I/O, L87P_Y	I/O, L87P_Y	I/O, L87P_Y
I/O	5	Y6	-	-	-	-	-	I/O	I/O	I/O
I/O	5	AA6	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N_YY	5	V6	All	-	I/O, L61N_YY	I/O, L81N_YY	I/O, L86N_YY	I/O, L86N_YY	I/O, L86N_YY	I/O, L86N_YY
I/O, L#P_YY	5	W6	All	-	I/O, L61P_YY	I/O, L81P_YY	I/O, L86P_YY	I/O, L86P_YY	I/O, L86P_YY	I/O, L86P_YY
I/O, VREF Bank 5, L#N_YY	5	AB7	All	All	I/O, VREF Bank 5, L60N_YY	I/O, VREF Bank 5, L80N_YY	I/O, VREF Bank 5, L85N_YY	I/O, VREF Bank 5, L85N_YY	I/O, VREF Bank 5, L85N_YY	I/O, VREF Bank 5, L85N_YY
I/O, L#P_YY	5	AA7	All	-	I/O, L60P_YY	I/O, L80P_YY	I/O, L85P_YY	I/O, L85P_YY	I/O, L85P_YY	I/O, L85P_YY
I/O	5	Y7	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N_Y	5	V7	XC2S300E, 600E	-	-	I/O, L79N	I/O, L84N	I/O, L84N_Y	I/O, L84N	I/O, L84N_Y
I/O, L#P_Y	5	W7	XC2S300E, 600E	-	I/O	I/O, L79P	I/O, L84P	I/O, L84P_Y	I/O, L84P	I/O, L84P_Y
I/O, L#N_Y	5	AB8	XC2S100E, 300E, 600E	XC2S600E	I/O, L59N_Y	I/O, L78N	I/O, L83N	I/O, L83N_Y	I/O, L83N	I/O, VREF Bank 5, L83N_Y
I/O, L#P_Y	5	AA8	XC2S100E, 300E, 600E	-	I/O, L59P_Y	I/O, L78P	I/O, L83P	I/O, L83P_Y	I/O, L83P	I/O, L83P_Y
I/O	5	Y8	-	-	-	-	-	I/O	I/O	I/O

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O	3	P20	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#N	3	P18	XC2S150E, 200E, 300E, 400E	-	-	I/O, L46N_Y	I/O, L50N_Y	I/O, L50N_Y	I/O, L50N_Y	I/O, L50N
I/O, L#P	3	P19	XC2S100E, 150E, 200E, 300E, 400E	-	I/O, L34N_Y	I/O, L46P_Y	I/O, L50P_Y	I/O, L50P_Y	I/O, L50P_Y	I/O, L50P
I/O, L#N	3	N22	XC2S100E, 150E, 200E, 300E, 600E	-	I/O, L34P_Y	I/O, L45N_Y	I/O, L49N_Y	I/O, L49N_Y	I/O, L49N	I/O, L49N_Y
I/O, L#P	3	N21	XC2S150E, 200E, 300E, 600E	-	-	I/O, L45P_Y	I/O, L49P_Y	I/O, L49P_Y	I/O, L49P	I/O, L49P_Y
I/O	3	P17	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#N	3	N19	XC2S100E, 150E, 200E, 300E, 600E(1)	-	I/O, L33N_YY	I/O, L44N_YY	I/O, L48N_YY	I/O, L48N_YY	I/O, L48N	I/O, L48N_Y
I/O, L#P	3	N20	XC2S100E, 150E, 200E, 300E, 600E(1)	-	I/O, L33P_YY	I/O, L44P_YY	I/O, L48P_YY	I/O, L48P_YY	I/O, L48P	I/O, L48P_Y
I/O, VREF Bank 3, L#N	3	N18	XC2S300E, 400E, 600E	All	I/O, VREF Bank 3, L32N	I/O, VREF Bank 3, L43N	I/O, VREF Bank 3, L47N	I/O, VREF Bank 3, L47N_Y	I/O, VREF Bank 3, L47N_Y	I/O, VREF Bank 3, L47N_Y
I/O (D4), L#P	3	N17	XC2S300E, 400E, 600E	-	I/O (D4), L32P	I/O (D4), L43P	I/O (D4), L47P	I/O (D4), L47P_Y	I/O (D4), L47P_Y	I/O (D4), L47P_Y
I/O	3	M22	-	-	-	-	-	I/O	I/O	I/O
I/O, L#N	3	M20	XC2S300E, 400E	-	-	-	I/O, L46N	I/O, L46N_Y	I/O, L46N_Y	I/O, L46N
I/O, L#P	3	M21	XC2S100E, 150E, 300E, 400E	-	I/O, L31N_Y	I/O, L42N_Y	I/O, L46P	I/O, L46P_Y	I/O, L46P_Y	I/O, L46P
I/O, L#N	3	M18	XC2S100E, 150E, 200E, 300E, 600E	XC2S400E, 600E	I/O, L31P_Y	I/O, L42P_Y	I/O, L45N_Y	I/O, L45N_Y	I/O, VREF Bank 3, L45N	I/O, VREF Bank 3, L45N_Y
I/O, L#P	3	M19	XC2S200E, 300E, 600E	-	-	I/O	I/O, L45P_Y	I/O, L45P_Y	I/O, L45P	I/O, L45P_Y
I/O	3	M17	-	-	-	-	-	I/O	I/O	I/O
I/O (TRDY)	3	L22	-	-	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)
I/O (IRDY), L#N_YY	2	L21	All	-	I/O (IRDY), L30N_YY	I/O (IRDY), L41N_YY	I/O (IRDY), L44N_YY	I/O (IRDY), L44N_YY	I/O (IRDY), L44N_YY	I/O (IRDY), L44N_YY
I/O, L#P_YY	2	L20	All	-	I/O, L30P_YY	I/O, L41P_YY	I/O, L44P_YY	I/O, L44P_YY	I/O, L44P_YY	I/O, L44P_YY
I/O	2	L19	-	-	-	-	-	I/O	I/O	I/O
I/O, L#N	2	L18	XC2S200E, 300E, 600E	-	-	I/O	I/O, L43N_Y	I/O, L43N_Y	I/O, L43N	I/O, L43N_Y

Additional FG456 Package Pins *(Continued)*

VCCO Bank 1 Pins								
F15	F16	G13	G14	-	-	-	-	-
VCCO Bank 2 Pins								
G17	H17	J16	K16	-	-	-	-	-
VCCO Bank 3 Pins								
N16	P16	R17	T17	-	-	-	-	-
VCCO Bank 4 Pins								
T13	T14	U15	U16	-	-	-	-	-
VCCO Bank 5 Pins								
T9	T10	U7	U8	-	-	-	-	-
VCCO Bank 6 Pins								
N7	P7	R6	T6	-	-	-	-	-
VCCO Bank 7 Pins								
G6	H6	J7	K7	-	-	-	-	-
GND Pins								
A1	A2(2)	A22	B1(2)	B2	B21	C3	C20	G11
G12	J9	J10	J11	J12	J13	J14	K9	K10
K11	K12	K13	K14	L7	L9	L10	L11	L12
L13	L14	L16	M7	M9	M10	M11	M12	M13
M14	M16	N9	N10	N11	N12	N13	N14	P9
P10	P11	P12	P13	P14	T11	T12	Y20	Y3
Y4(2)	AA2	AA4(2)	AA21	AA22(2)	AB1	AB22	-	-
Not Connected Pins								
A2(2)	B1(2)	D4(1)	D19(1)	W4(1)	W19(1)	Y4(2)	AA4(2)	AA22(2)

Notes:
1. VCCINT connections in XC2S400E and XC2S600E. No Connects (no internal connection) in XC2S100E, XC2S150E, XC2S200E, and XC2S300E.
2. GND connections in XC2S400E and XC2S600E. No Connects (no internal connection) in XC2S100E, XC2S150E, XC2S200E, and XC2S300E

FG676 Pinouts (XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
TMS	-	B1	-	-	TMS	TMS
I/O	7	D3	-	-	I/O	I/O
I/O, L204P	7	C2	-	-	-	I/O, L204P
I/O, L204N	7	C1	-	-	-	I/O, L204N
I/O, L203P	7	D2	XC2S600E	-	-	I/O, L203P_Y
I/O, L203N	7	D1	XC2S600E	-	I/O	I/O, L203N_Y
I/O, L202P_YY	7	E2	All	-	I/O, L202P_YY	I/O, L202P_YY
I/O, L202N_YY	7	E1	All	-	I/O, L202N_YY	I/O, L202N_YY

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L201P	7	E4	XC2S400E	-	I/O, L201P_Y	I/O, L201P
I/O, L201N	7	F5	XC2S400E	-	I/O, L201N_Y	I/O, L201N
I/O, VREF Bank 7, L200P	7	F4	XC2S600E	All	I/O, VREF Bank 7, L200P	I/O, VREF Bank 7, L200P_Y
I/O, L200N	7	F3	XC2S600E	-	I/O, L200N	I/O, L200N_Y
I/O, L199P	7	F2	XC2S600E	-	-	I/O, L199P_Y
I/O, L199N	7	F1	XC2S600E	-	I/O	I/O, L199N_Y
I/O, L198P	7	G6	XC2S400E	-	I/O, L198P_Y	I/O, L198P
I/O, L198N	7	G5	XC2S400E	-	I/O, L198N_Y	I/O, L198N
I/O, L197P	7	G4	XC2S600E	-	I/O, L197P	I/O, L197P_Y
I/O, L197N	7	G3	XC2S600E	-	I/O, L197N	I/O, L197N_Y
I/O, VREF Bank 7, L196P_YY	7	G2	All	All	I/O, VREF Bank 7, L196P_YY	I/O, VREF Bank 7, L196P_YY
I/O, L196N_YY	7	G1	All	-	I/O, L196N_YY	I/O, L196N_YY
I/O	7	H7	-	-	I/O	I/O
I/O, L195P_YY	7	H6	All	-	I/O, L195P_YY	I/O, L195P_YY
I/O, L195N_YY	7	H5	All	-	I/O, L195N_YY	I/O, L195N_YY
I/O	7	J8	-	-	-	I/O
I/O, L194P	7	H2	XC2S400E	-	I/O, L194P_Y	I/O, L194P
I/O, L194N	7	H1	XC2S400E	-	I/O, L194N_Y	I/O, L194N
I/O, L193P	7	J7	XC2S600E	XC2S600E	I/O	I/O, VREF Bank 7, L193P_Y
I/O, L193N	7	J6	XC2S600E	-	-	I/O, L193N_Y
I/O	7	J5	-	-	I/O	I/O
I/O, L192P_YY	7	J4	All	-	I/O, L192P_YY	I/O, L192P_YY
I/O, L192N_YY	7	J3	All	-	I/O, L192N_YY	I/O, L192N_YY
I/O	7	K5	-	-	I/O	I/O
I/O, VREF Bank 7, L191P_YY	7	J2	All	All	I/O, VREF Bank 7, L191P_YY	I/O, VREF Bank 7, L191P_YY
I/O, L191N_YY	7	J1	All	-	I/O, L191N_YY	I/O, L191N_YY
I/O, L190P_YY	7	K8	All	-	I/O, L190P_YY	I/O, L190P_YY
I/O, L190N_YY	7	K7	All	-	I/O, L190N_YY	I/O, L190N_YY
I/O	7	K4	-	-	-	I/O
I/O, L189P_YY	7	K3	All	-	I/O, L189P_YY	I/O, L189P_YY
I/O, L189N_YY	7	K2	All	-	I/O, L189N_YY	I/O, L189N_YY
I/O	7	K1	-	-	-	I/O

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L138P_YY	5	Y10	All	-	I/O, L138P_YY	I/O, L138P_YY
I/O, L137N_YY	5	AB10	All	-	I/O, L137N_YY	I/O, L137N_YY
I/O, L137P_YY	5	AC10	All	-	I/O, L137P_YY	I/O, L137P_YY
I/O	5	AD10	-	-	-	I/O
I/O, L136N	5	AE10	XC2S600E	-	I/O, L136N	I/O, L136N_Y
I/O, L136P	5	AF10	XC2S600E	-	I/O, L136P	I/O, L136P_Y
I/O	5	AD11	-	-	-	I/O
I/O, L135N_YY	5	W11	All	-	I/O, L135N_YY	I/O, L135N_YY
I/O, L135P_YY	5	Y11	All	-	I/O, L135P_YY	I/O, L135P_YY
I/O, L134N_YY	5	AA11	All	-	I/O, L134N_YY	I/O, L134N_YY
I/O, L134P_YY	5	AB11	All	-	I/O, L134P_YY	I/O, L134P_YY
I/O	5	V12	-	-	-	I/O
I/O, L133N	5	AE11	-	-	I/O, L133N	I/O, L133N
I/O, L133P	5	AF11	-	-	I/O, L133P	I/O, L133P
I/O	5	W12	-	-	-	I/O
I/O, L132N_YY	5	Y12	All	-	I/O, L132N_YY	I/O, L132N_YY
I/O, L132P_YY	5	AA12	All	-	I/O, L132P_YY	I/O, L132P_YY
I/O, VREF Bank 5, L131N_YY	5	AB12	All	All	I/O, VREF Bank 5, L131N_YY	I/O, VREF Bank 5, L131N_YY
I/O, L131P_YY	5	AC12	All	-	I/O, L131P_YY	I/O, L131P_YY
I/O	5	V13	-	-	-	I/O
I/O, L130N_YY	5	AE12	All	-	I/O, L130N_YY	I/O, L130N_YY
I/O, L130P_YY	5	AF12	All	-	I/O, L130P_YY	I/O, L130P_YY
I/O	5	W13	-	-	-	I/O
I/O, L129N	5	Y13	XC2S600E	-	I/O, L129N	I/O, L129N_Y
I/O, L129P	5	AA13	XC2S600E	-	I/O, L129P	I/O, L129P_Y
I/O, VREF Bank 5, L128N	5	AB13	XC2S600E	All	I/O, VREF Bank 5, L128N	I/O, VREF Bank 5, L128N_Y
I/O, L128P	5	AC13	XC2S600E	-	I/O, L128P	I/O, L128P_Y
I/O	5	AD13	-	-	-	I/O
I/O, L127N	5	V14	-	-	I/O	I/O, L127N
I/O, L127P	5	W14	-	-	-	I/O, L127P
I/O (DLL), L126N	5	AE13	-	-	I/O (DLL), L126N	I/O (DLL), L126N
GCK1, I	5	AF13	-	-	GCK1, I	GCK1, I

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O	4	AC18	-	-	I/O	I/O
I/O, VREF Bank 4, L114N	4	AB18	-	All	I/O, VREF Bank 4, L114N	I/O, VREF Bank 4, L114N
I/O, L114P	4	AA18	-	-	I/O, L114P	I/O, L114P
I/O, L113N	4	Y18	-	-	I/O, L113N	I/O, L113N
I/O, L113P	4	W18	-	-	I/O, L113P	I/O, L113P
I/O	4	AB19	-	-	I/O	I/O
I/O, L112N	4	AF19	XC2S600E	-	I/O	I/O, L112N_Y
I/O, L112P	4	AE19	XC2S600E	XC2S600E	-	I/O, VREF Bank 4, L112P_Y
I/O, L111N	4	AA19	XC2S600E	-	I/O, L111N	I/O, L111N_Y
I/O, L111P	4	Y19	XC2S600E	-	I/O, L111P	I/O, L111P_Y
I/O	4	AF20	-	-	-	I/O
I/O, L110N	4	AE20	XC2S600E	-	I/O, L110N	I/O, L110N_Y
I/O, L110P	4	AD20	XC2S600E	-	I/O, L110P	I/O, L110P_Y
I/O	4	AC20	-	-	I/O	I/O
I/O, L109N_YY	4	AB20	All	-	I/O, L109N_YY	I/O, L109N_YY
I/O, VREF Bank 4, L109P_YY	4	AA20	All	All	I/O, VREF Bank 4, L109P_YY	I/O, VREF Bank 4, L109P_YY
I/O	4	Y20	-	-	I/O	I/O
I/O, L108N	4	AF21	-	-	I/O, L108N	I/O, L108N
I/O, L108P	4	AE21	-	-	I/O, L108P	I/O, L108P
I/O, L107N	4	AD21	-	-	I/O, L107N	I/O, L107N
I/O, L107P	4	AC21	-	-	I/O, L107P	I/O, L107P
I/O	4	AC22	-	-	-	I/O
I/O, L106N_YY	4	AF22	All	-	I/O, L106N_YY	I/O, L106N_YY
I/O, VREF Bank 4, L106P_YY	4	AE22	All	All	I/O, VREF Bank 4, L106P_YY	I/O, VREF Bank 4, L106P_YY
I/O, L105N_YY	4	AB21	All	-	I/O, L105N_YY	I/O, L105N_YY
I/O, L105P_YY	4	AA21	All	-	I/O, L105P_YY	I/O, L105P_YY
I/O, L104N_YY	4	AF23	All	-	I/O, L104N_YY	I/O, L104N_YY
I/O, L104P_YY	4	AE23	All	-	I/O, L104P_YY	I/O, L104P_YY
I/O, L103N	4	AD23	XC2S600E	-	I/O	I/O, L103N_Y
I/O, L103P	4	AE24	XC2S600E	-	-	I/O, L103P_Y
I/O, L102N_YY	4	AF24	All	-	I/O, L102N_YY	I/O, L102N_YY
I/O, L102P_YY	4	AF25	All	-	I/O, L102P_YY	I/O, L102P_YY

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L88P_YY	3	V25	All	-	I/O, L88P_YY	I/O, L88P_YY
I/O	3	V26	-	-	I/O	I/O
I/O, VREF Bank 3, L87N_YY	3	U19	All	All	I/O, VREF Bank 3, L87N_YY	I/O, VREF Bank 3, L87N_YY
I/O (D6), L87P_YY	3	U20	All	-	I/O (D6), L87P_YY	I/O (D6), L87P_YY
I/O (D5), L86N_YY	3	U22	All	-	I/O (D5), L86N_YY	I/O (D5), L86N_YY
I/O, L86P_YY	3	U23	All	-	I/O, L86P_YY	I/O, L86P_YY
I/O	3	U24	-	-	-	I/O
I/O, L85N	3	U25	XC2S600E	-	-	I/O, L85N_Y
I/O, L85P	3	U26	XC2S600E	-	I/O	I/O, L85P_Y
I/O	3	R18	-	-	I/O	I/O
I/O, L84N	3	T19	XC2S400E	-	I/O, L84N_Y	I/O, L84N
I/O, L84P	3	T20	XC2S400E	-	I/O, L84P_Y	I/O, L84P
I/O, L83N	3	T21	XC2S600E	-	I/O, L83N	I/O, L83N_Y
I/O, L83P	3	T22	XC2S600E	-	I/O, L83P	I/O, L83P_Y
I/O	3	T24	-	-	-	I/O
I/O, L82N	3	T25	XC2S600E	-	I/O, L82N	I/O, L82N_Y
I/O, L82P	3	T26	XC2S600E	-	I/O, L82P	I/O, L82P_Y
I/O	3	R19	-	-	-	I/O
I/O, L81N	3	R20	XC2S600E	-	I/O, L81N	I/O, L81N_Y
I/O, L81P	3	R21	XC2S600E	-	I/O, L81P	I/O, L81P_Y
I/O, VREF Bank 3, L80N_YY	3	R22	All	All	I/O, VREF Bank 3, L80N_YY	I/O, VREF Bank 3, L80N_YY
I/O (D4), L80P_YY	3	R23	All	-	I/O (D4), L80P_YY	I/O (D4), L80P_YY
I/O	3	P18	-	-	-	I/O
I/O, L79N_YY	3	R25	All	-	I/O, L79N_YY	I/O, L79N_YY
I/O, L79P_YY	3	R26	All	-	I/O, L79P_YY	I/O, L79P_YY
I/O	3	P19	-	-	-	I/O
I/O, L78N	3	P20	XC2S400E	-	I/O, L78N_Y	I/O, L78N
I/O, L78P	3	P21	XC2S400E	-	I/O, L78P_Y	I/O, L78P
I/O, VREF Bank 3, L77N	3	P22	XC2S600E	All	I/O, VREF Bank 3, L77N	I/O, VREF Bank 3, L77N_Y
I/O, L77P	3	P23	XC2S600E	-	I/O, L77P	I/O, L77P_Y
I/O	3	P24	-	-	-	I/O
I/O, L76N_YY	3	P25	All	-	I/O, L76N_YY	I/O, L76N_YY
I/O, L76P_YY	3	P26	All	-	I/O, L76P_YY	I/O, L76P_YY

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L64N_YY	2	J25	All	-	I/O, L64N_YY	I/O, L64N_YY
I/O (D2), L64P_YY	2	J24	All	-	I/O (D2), L64P_YY	I/O (D2), L64P_YY
I/O (D1)	2	J23	-	-	I/O (D1)	I/O (D1)
I/O, VREF Bank 2, L63N_YY	2	J22	All	All	I/O, VREF Bank 2, L63N_YY	I/O, VREF Bank 2, L63N_YY
I/O, L63P_YY	2	J21	All	-	I/O, L63P_YY	I/O, L63P_YY
I/O, L62N_YY	2	J20	All	-	I/O, L62N_YY	I/O, L62N_YY
I/O, L62P_YY	2	J19	All	-	I/O, L62P_YY	I/O, L62P_YY
I/O	2	H22	-	-	I/O	I/O
I/O, L61N	2	H26	XC2S600E	-	I/O	I/O, L61N_Y
I/O, L61P	2	H25	XC2S600E	XC2S600E	-	I/O, VREF Bank 2, L61P_Y
I/O, L60N	2	H21	XC2S400E	-	I/O, L60N_Y	I/O, L60N
I/O, L60P	2	H20	XC2S400E	-	I/O, L60P_Y	I/O, L60P
I/O	2	G26	-	-	-	I/O
I/O, L59N_YY	2	G25	All	-	I/O, L59N_YY	I/O, L59N_YY
I/O, L59P_YY	2	G24	All	-	I/O, L59P_YY	I/O, L59P_YY
I/O	2	G23	-	-	I/O	I/O
I/O, L58N_YY	2	G22	All	-	I/O, L58N_YY	I/O, L58N_YY
I/O, VREF Bank 2, L58P_YY	2	G21	All	All	I/O, VREF Bank 2, L58P_YY	I/O, VREF Bank 2, L58P_YY
I/O	2	G20	-	-	I/O	I/O
I/O, L57N_YY	2	F26	All	-	I/O, L57N_YY	I/O, L57N_YY
I/O, L57P_YY	2	F25	All	-	I/O, L57P_YY	I/O, L57P_YY
I/O, L56N	2	F24	XC2S600E	-	I/O, L56N	I/O, L56N_Y
I/O, L56P	2	F23	XC2S600E	-	I/O, L56P	I/O, L56P_Y
I/O	2	F22	-	-	-	I/O
I/O, L55N	2	E26	XC2S600E	-	I/O, L55N	I/O, L55N_Y
I/O, VREF Bank 2, L55P	2	E25	XC2S600E	All	I/O, VREF Bank 2, L55P	I/O, VREF Bank 2, L55P_Y
I/O, L54N	2	E23	XC2S400E	-	I/O, L54N_Y	I/O, L54N
I/O, L54P	2	E22	XC2S400E	-	I/O, L54P_Y	I/O, L54P
I/O, L53N_YY	2	F21	All	-	I/O, L53N_YY	I/O, L53N_YY
I/O, L53P_YY	2	E21	All	-	I/O, L53P_YY	I/O, L53P_YY
I/O, L52N	2	D26	XC2S600E	-	I/O	I/O, L52N_Y
I/O, L52P	2	D25	XC2S600E	-	-	I/O, L52P_Y

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L51N	2	D24	-	-	-	I/O, L51N
I/O, L51P	2	C25	-	-	-	I/O, L51P
I/O (DIN, D0), L50N_YY	2	C26	All	-	I/O (DIN, D0), L50N_YY	I/O (DIN, D0), L50N_YY
I/O (DOUT, BUSY), L50P_YY	2	B26	All	-	I/O (DOUT, BUSY), L50P_YY	I/O (DOUT, BUSY), L50P_YY
CCLK	2	A25	-	-	CCLK	CCLK
TDO	2	C23	-	-	TDO	TDO
TDI	-	D22	-	-	TDI	TDI
I/O ($\overline{CS}$), L49P_YY	1	B24	All	-	I/O ($\overline{CS}$), L49P_YY	I/O ($\overline{CS}$), L49P_YY
I/O ($\overline{WRITE}$), L49N_YY	1	A24	All	-	I/O ($\overline{WRITE}$), L49N_YY	I/O ($\overline{WRITE}$), L49N_YY
I/O, L48P	1	B23	-	-	I/O	I/O, L48P
I/O, L48N	1	A23	-	-	-	I/O, L48N
I/O, L47P	1	B22	XC2S400E	-	I/O, L47P_Y	I/O, L47P
I/O, L47N	1	A22	XC2S400E	-	I/O, L47N_Y	I/O, L47N
I/O, L46P_YY	1	D21	All	-	I/O, L46P_YY	I/O, L46P_YY
I/O, L46N_YY	1	C21	All	-	I/O, L46N_YY	I/O, L46N_YY
I/O, VREF Bank 1, L45P_YY	1	B21	All	All	I/O, VREF Bank 1, L45P_YY	I/O, VREF Bank 1, L45P_YY
I/O, L45N_YY	1	A21	All	-	I/O, L45N_YY	I/O, L45N_YY
I/O, L44P	1	F20	XC2S600E	-	-	I/O, L44P_Y
I/O, L44N	1	E20	XC2S600E	-	I/O	I/O, L44N_Y
I/O, L43P_YY	1	D20	All	-	I/O, L43P_YY	I/O, L43P_YY
I/O, L43N_YY	1	C20	All	-	I/O, L43N_YY	I/O, L43N_YY
I/O, L42P_YY	1	B20	All	-	I/O, L42P_YY	I/O, L42P_YY
I/O, L42N_YY	1	A20	All	-	I/O, L42N_YY	I/O, L42N_YY
I/O, VREF Bank 1, L41P_YY	1	G19	All	All	I/O, VREF Bank 1, L41P_YY	I/O, VREF Bank 1, L41P_YY
I/O, L41N_YY	1	F19	All	-	I/O, L41N_YY	I/O, L41N_YY
I/O	1	E19	-	-	-	I/O
I/O, L40P_YY	1	B19	All	-	I/O, L40P_YY	I/O, L40P_YY
I/O, L40N_YY	1	A19	All	-	I/O, L40N_YY	I/O, L40N_YY
I/O	1	H18	-	-	I/O	I/O
I/O, L39P	1	G18	XC2S600E	-	I/O, L39P	I/O, L39P_Y

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L2N_YY	0	E5	All	-	I/O, L2N_YY	I/O, L2N_YY
I/O, L1P_YY	0	B4	All	-	I/O, L1P_YY	I/O, L1P_YY
I/O, L1N_YY	0	C4	All	-	I/O, L1N_YY	I/O, L1N_YY
I/O, L0P	0	A3	XC2S600E	-	I/O	I/O, L0P_Y
I/O, L0N	0	B3	XC2S600E	-	-	I/O, L0N_Y
I/O	0	A4	-	-	I/O	I/O
TCK	-	A2	-	-	TCK	TCK

FG676 Differential Clock Pins

Clock	Bank	P Input		N Input	
		Pin	Name	Pin	Name
GCK0	4	AF14	GCK0, I	AE14	I/O (DLL), L126P
GCK1	5	AF13	GCK1, I	AE13	I/O (DLL), L126N
GCK2	1	A14	GCK2, I	B14	I/O (DLL), L23P
GCK3	0	A13	GCK3, I	B13	I/O (DLL), L23N

Additional FG676 Package Pins

VCCINT Pins						
H8	H19	J9	J18	K10	K11	K16
K17	L10	L17	T10	T17	U10	U11
U16	U17	V9	V18	W8	W19	-
VCCO Bank 0 Pins						
C5	C8	D11	J10	J11	K12	K13
VCCO Bank 1 Pins						
C19	C22	D16	J16	J17	K14	K15
VCCO Bank 2 Pins						
E24	H24	K18	L18	L23	M17	N17
VCCO Bank 3 Pins						
P17	R17	T18	T23	U18	W24	AB24
VCCO Bank 4 Pins						
U14	U15	V16	V17	AC16	AD19	AD22
VCCO Bank 5 Pins						
U12	U13	V10	V11	AC11	AD5	AD8
VCCO Bank 6 Pins						
P10	R10	T4	T9	U9	W3	AB3
VCCO Bank 7 Pins						
H3	K9	L4	L9	M10	N10	E3