AMD Xilinx - XC2S50E-6PQ208C Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	384
Number of Logic Elements/Cells	1728
Total RAM Bits	32768
Number of I/O	146
Number of Gates	50000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s50e-6pq208c

Table 8: **Boundary-Scan Instructions *(Continued)***

Boundary-Scan Command	Binary Code[4:0]	Description
INTEST	00111	Enables boundary-scan INTEST operation
USERCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIGHZ	01010	Disables output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions

The public boundary-scan instructions are available prior to configuration, except for USER1 and USER2. After configuration, the public instructions remain available together with any USERCODE instructions installed during the configuration. While the SAMPLE/PRELOAD and BYPASS instructions are available during configuration, it is recommended that boundary-scan operations not be performed during this transitional period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

To facilitate internal scan chains, the User Register provides three outputs (Reset, Update, and Shift) that represent the corresponding states in the boundary-scan internal state machine.

Figure 14 is a diagram of the Spartan-IIE family boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

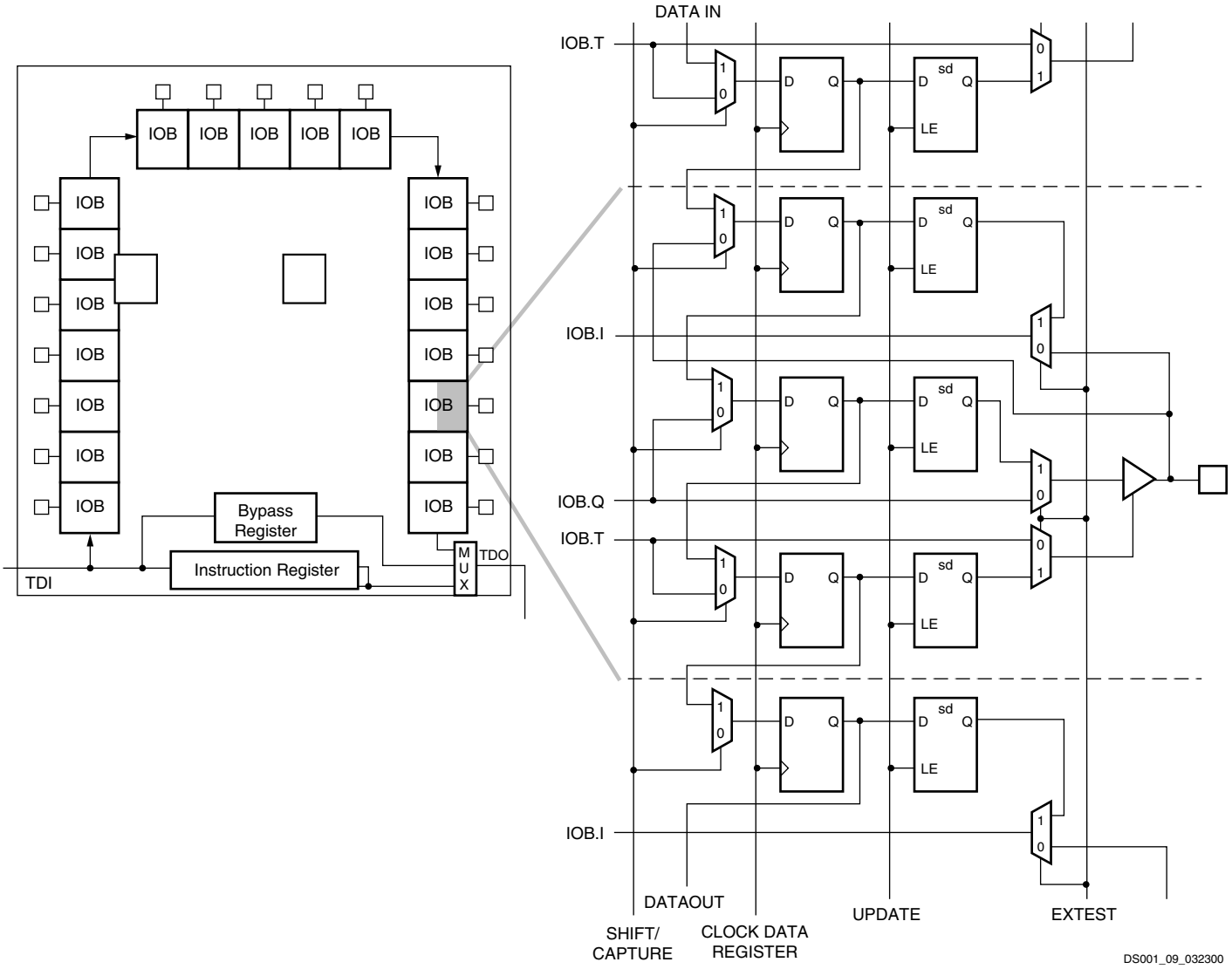


Figure 14: **Spartan-IIE Family Boundary Scan Logic**

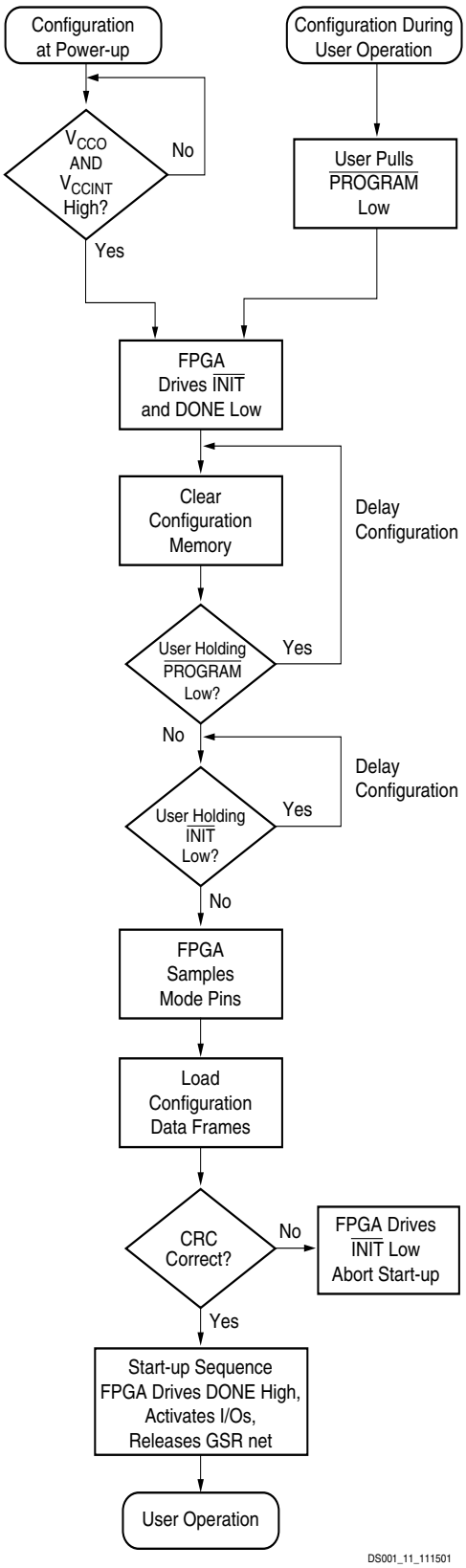


Figure 16: **Configuration Flow Diagram**

Clearing Configuration Memory

The device indicates that clearing the configuration memory is in progress by driving $\overline{\text{INIT}}$ Low.

Delaying Configuration

At this time, the user can delay configuration by holding either $\overline{\text{PROGRAM}}$ or $\overline{\text{INIT}}$ Low, which causes the device to remain in the memory clearing phase. Note that the bidirectional $\overline{\text{INIT}}$ line is driving a Low logic level during memory clearing. Thus, to avoid contention, use an open-drain driver to keep $\overline{\text{INIT}}$ Low.

With no delay in force, the device indicates that the memory is completely clear by driving $\overline{\text{INIT}}$ High. The FPGA samples its mode pins on this Low-to-High transition.

Loading Configuration Data

Once $\overline{\text{INIT}}$ is High, the user can begin loading configuration data frames into the device. The details of loading the configuration data are discussed in the sections treating the configuration modes individually. The sequence of operations necessary to load configuration data using the serial modes is shown in Figure 18. Loading data using the Slave Parallel mode is shown in Figure 21, page 28.

CRC Error Checking

After the loading of configuration data, a CRC value embedded in the configuration file is checked against a CRC value calculated within the FPGA. If the CRC values do not match, the FPGA drives $\overline{\text{INIT}}$ Low to indicate that an error has occurred and configuration is aborted. Note that attempting to load an incorrect bitstream causes configuration to fail and can damage the device.

To reconfigure the device, the $\overline{\text{PROGRAM}}$ pin should be asserted to reset the configuration logic. Recycling power also resets the FPGA for configuration. See Clearing Configuration Memory.

Start-up

The start-up sequence oversees the transition of the FPGA from the configuration state to full user operation. A match of CRC values, indicating a successful loading of the configuration data, initiates the sequence.

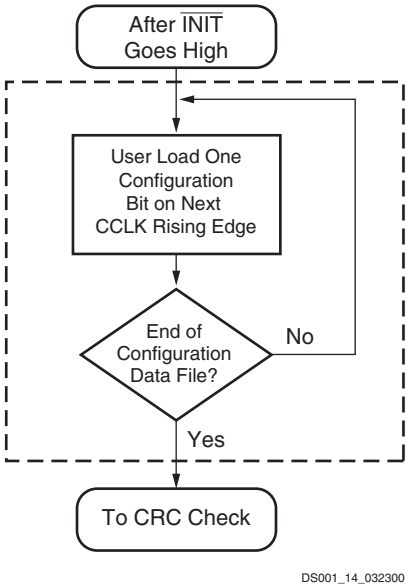


Figure 18: **Loading Serial Mode Configuration Data**

Slave Serial Mode

In Slave Serial mode, the FPGA's CCLK pin is driven by an external source, allowing the FPGA to be configured from other logic devices such as microprocessors or in a daisy-chain configuration. Figure 19 shows connections for a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-IIE device in slave serial mode should be connected as shown for the third device from the left. Slave Serial mode is selected by a <11x> on the mode pins (M0, M1, M2). The weak pull-ups on the mode pins make slave serial the default mode if the pins are left unconnected.

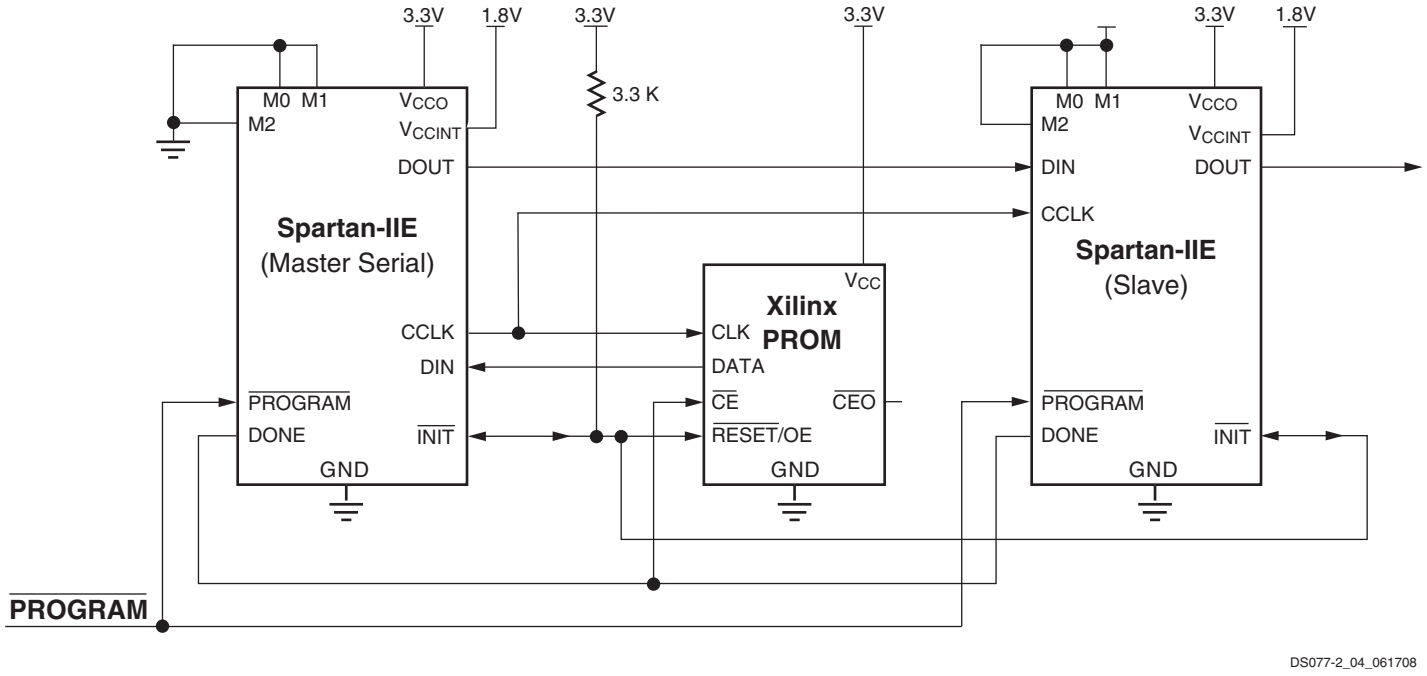
The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

Timing for Slave Serial mode is shown in Figure 24, page 49.

Daisy Chain

Multiple FPGAs in Slave Serial mode can be daisy-chained for configuration from a single source. After an FPGA is configured, data for the next device is sent to the DOUT pin. Data on the DOUT pin changes on the rising edge of CCLK. Note that DOUT changes on the falling edge of CCLK for some Xilinx families but mixed daisy chains are allowed. Configuration must be delayed until $\overline{\text{INIT}}$ pins of all daisy-chained FPGAs are High. For more information, see Start-up, page 23.

The maximum amount of data that can be sent to the DOUT pin for a serial daisy chain is 2^{20}-1 (1,048,575) 32-bit words, or 33,554,400 bits, which is approximately 8 XC2S600E bitstreams. The configuration bitstream of downstream devices is limited to this size.



Notes:
1. If the DriveDone configuration option is not active for any of the FPGAs, pull up DONE with a 330Ω resistor.

Figure 19: **Master/Slave Serial Configuration Circuit Diagram**

Master Serial Mode

In Master Serial mode, the CCLK output of the FPGA drives a Xilinx PROM, which feeds a serial stream of configuration data to the FPGA's DIN input. Figure 19 shows a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-IIE device in Master Serial mode should be connected as shown for the device on the left side. Master Serial mode is selected by a <00x> on the mode pins (M0, M1, M2). The PROM RESET pin is driven by $\overline{\text{INIT}}$, and the CE input is driven by DONE. For more information on serial PROMs, see the Xilinx Configuration PROM data sheets at www.xilinx.com.

The interface is identical to the slave serial mode except that an oscillator internal to the FPGA is used to generate the configuration clock (CCLK). Any of a number of different frequencies ranging from 4 to 60 MHz can be set using the ConfigRate option in the Xilinx development software. When selecting a CCLK frequency, ensure that the serial PROM and any daisy-chained FPGAs are fast enough to support the clock rate. On power-up, while the first 60 bytes of the configuration data are being loaded, the CCLK frequency is always 2.5 MHz. This frequency is used until the ConfigRate bits, part of the configuration file, have been loaded into the FPGA, at which point the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz. The frequency of the CCLK signal created by the internal oscillator has a variance of +45%, –30% from the specified value.

The FPGA accepts one bit of configuration data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge. The timing for Master Serial mode is shown in Figure 25, page 49.

Slave Parallel Mode (SelectMAP)

The Slave Parallel mode, also known as SelectMAP, is the fastest configuration option. Byte-wide data is written into the FPGA on the D0-D7 pins. Note that D0 is the MSB of each byte for configuration. A BUSY flag is provided for controlling the flow of data at a clock frequency above 50 MHz.

Figure 20, page 27 shows the connections for two Spartan-IIE devices using the Slave Parallel mode. Slave Parallel mode is selected by a <011> on the mode pins (M0, M1, M2).

The agent controlling configuration is not shown. Typically, a processor, a microcontroller, or CPLD controls the Slave Parallel interface. The controlling agent provides byte-wide configuration data, CCLK, a Chip Select ($\overline{\text{CS}}$) signal and a Write signal ($\overline{\text{WRITE}}$). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

After configuration, the pins of the Slave Parallel port (D0-D7) can be used as additional user I/O. Alternatively, the port may be retained to permit high-speed 8-bit readback. Then data can be read by deasserting $\overline{\text{WRITE}}$. If retention is selected, prohibit the D0-D7 pins from being used as user I/O. See Readback, page 28.

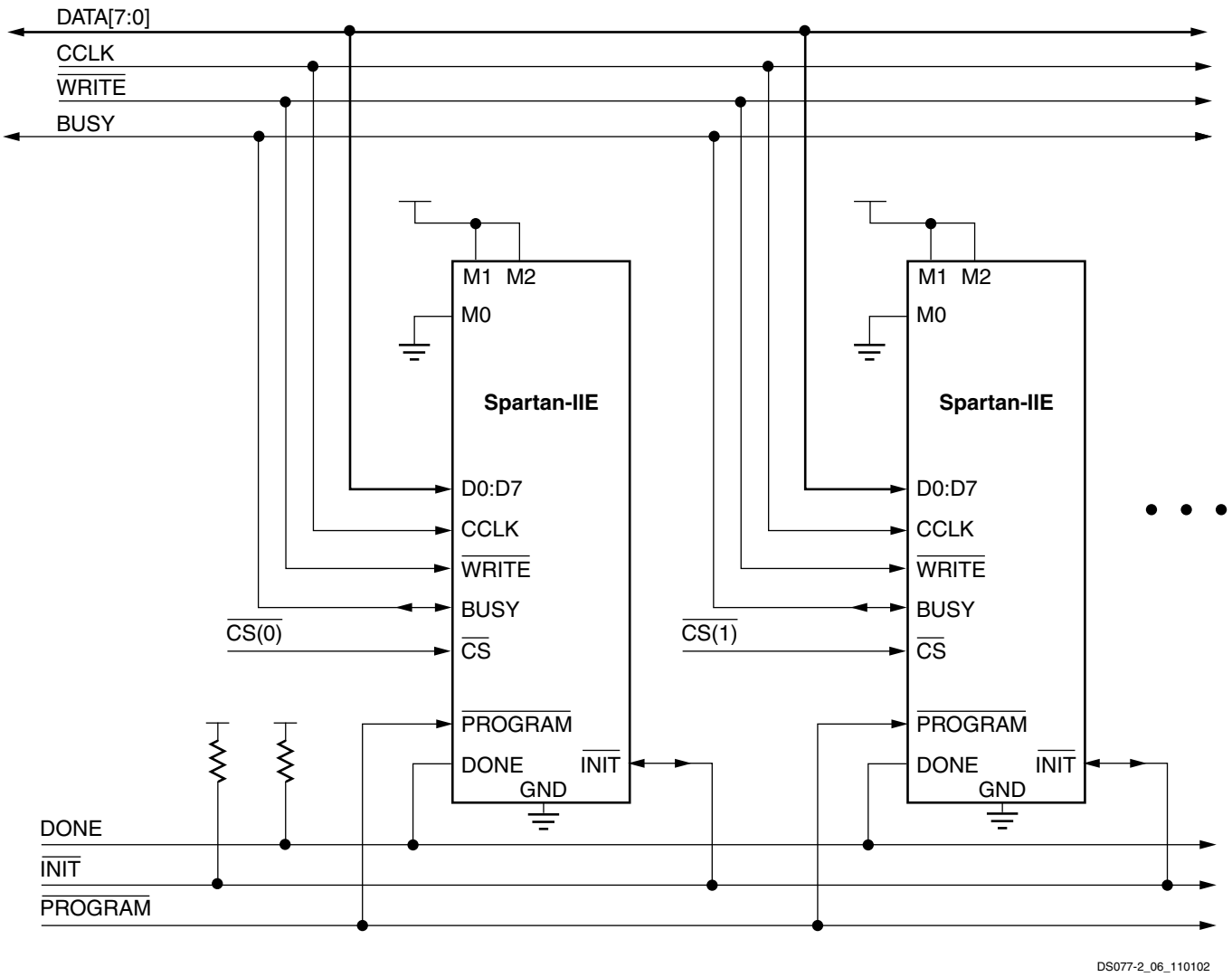


Figure 20: **Slave Parallel Configuration Circuit Diagram**

Multiple Spartan-IIE FPGAs can be configured using the Slave Parallel mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, $\overline{\text{WRITE}}$, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the $\overline{\text{CS}}$ pin of each device in turn and writing the appropriate data. Sync-to-DONE start-up timing is used to ensure that the start-up sequence does not begin until all the FPGAs have been loaded. See Start-up, page 23.

Write

When using the Slave Parallel Mode, write operations send packets of byte-wide configuration data into the FPGA. Figure 21, page 28 shows a flowchart of the write sequence used to load data into the Spartan-IIE FPGA. This is an expansion of the "Load Configuration Data Frames" block in Figure 16, page 23.

The timing for Slave Parallel mode is shown in Figure 26, page 50.

For the present example, the user holds $\overline{\text{WRITE}}$ and $\overline{\text{CS}}$ Low throughout the sequence of write operations. Note that when $\overline{\text{CS}}$ is asserted on successive CCLKs, $\overline{\text{WRITE}}$ must remain either asserted or deasserted. Otherwise an abort will be initiated, as in the next section.

1. Drive data onto D0-D7. Note that to avoid contention, the data source should not be enabled while $\overline{\text{CS}}$ is Low and $\overline{\text{WRITE}}$ is High. Similarly, while $\overline{\text{WRITE}}$ is High, no more than one device's $\overline{\text{CS}}$ should be asserted.
2. On the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this happens.
3. Repeat steps 1 and 2 until all the data has been sent.
4. Deassert $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL I	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	8	–8
HSTL III	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	24	–8
HSTL IV	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	48	–8
SSTL3 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	–8
SSTL3 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	–16
SSTL2 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.61	V_{REF} + 0.61	7.6	–7.6
SSTL2 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	15.2	–15.2
CTT	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.4	V_{REF} + 0.4	8	–8
AGP	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	Note (2)	Note (2)

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested.
2. Tested according to the relevant specifications.

LVDS DC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		2.375	2.5	2.625	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	1.25	1.425	1.6	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	0.9	1.075	1.25	V
V_{ODIFF}	Differential output voltage (Q – $\overline{Q}$), Q = High or ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	250	350	450	mV
V_{OCM}	Output common-mode voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.125	1.25	1.375	V
V_{IDIFF}	Differential input voltage (Q – $\overline{Q}$), Q = High or ($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25 V	100	350	-	mV
V_{ICM}	Input common-mode voltage	Differential input voltage = ±350 mV	0.2	1.25	2.2	V

LVPECL DC Specifications

These values are valid at the output of the source termination pack shown under LVPECL, with a 100Ω differential load only. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. The following table summarizes the DC output specifications of LVPECL.

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential input voltage	0.3	-	0.3	-	0.3	-	V

Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRACE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-IIE devices unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, *with* DLL (Pin-to-Pin)(1)

Symbol	Description	Speed Grade			Units
		All	-7	-6	
		Min	Max	Max	
$T_{ICKOFDLL}$	LVTTL global clock input to output delay using output flip-flop for LVTTL, 12 mA, fast slew rate, *with* DLL.	1.0	3.1	3.1	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables Constants for Calculating T_{IOOP} and Delay Measurement Methodology, page 41.
3. DLL output jitter is already included in the timing calculation.
4. For data *output* with different standards, adjust delays with the values shown in IOB Output Delay Adjustments for Different Standards(1), page 40. For a global clock input with standards other than LVTTL, adjust delays with values from the I/O Standard Global Clock Input Adjustments, page 42.

Global Clock Input to Output Delay for LVTTL, *without* DLL (Pin-to-Pin)(1)

Symbol	Description	Device	Speed Grade			Units
			All	-7	-6	
			Min	Max	Max	
T_{ICKOF}	LVTTL global clock input to output delay using output flip-flop for LVTTL, 12 mA, fast slew rate, *without* DLL.	XC2S50E	1.5	4.4	4.6	ns
		XC2S100E	1.5	4.4	4.6	ns
		XC2S150E	1.5	4.5	4.7	ns
		XC2S200E	1.5	4.5	4.7	ns
		XC2S300E	1.5	4.5	4.7	ns
		XC2S400E	1.5	4.6	4.8	ns
		XC2S600E	1.6	4.7	4.9	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables Constants for Calculating T_{IOOP} and Delay Measurement Methodology, page 41.
3. For data *output* with different standards, adjust delays with the values shown in IOB Output Delay Adjustments for Different Standards(1), page 40. For a global clock input with standards other than LVTTL, adjust delays with values from the I/O Standard Global Clock Input Adjustments, page 42.

IOB Output Delay Adjustments for Different Standards(1)

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade		Units
			-7	-6	
Output Delay Adjustments (Adj)					
T_{OLVTTL_S2}	Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, C_{SL})	LVTTL, Slow, 2 mA	14.7	14.7	ns
T_{OLVTTL_S4}		4 mA	7.5	7.5	ns
T_{OLVTTL_S6}		6 mA	4.8	4.8	ns
T_{OLVTTL_S8}		8 mA	3.0	3.0	ns
T_{OLVTTL_S12}		12 mA	1.9	1.9	ns
T_{OLVTTL_S16}		16 mA	1.7	1.7	ns
T_{OLVTTL_S24}		24 mA	1.3	1.3	ns
T_{OLVTTL_F2}		LVTTL, Fast, 2 mA	13.1	13.1	ns
T_{OLVTTL_F4}		4 mA	5.3	5.3	ns
T_{OLVTTL_F6}		6 mA	3.1	3.1	ns
T_{OLVTTL_F8}		8 mA	1.0	1.0	ns
T_{OLVTTL_F12}		12 mA	0	0	ns
T_{OLVTTL_F16}		16 mA	–0.05	–0.05	ns
T_{OLVTTL_F24}		24 mA	–0.20	–0.20	ns
$T_{OLVCMOS2}$		LVCMOS2	0.09	0.09	ns
$T_{OLVCMOS18}$		LVCMOS18	0.7	0.7	ns
T_{OLVDS}		LVDS	–1.2	–1.2	ns
$T_{OLVPECL}$		LVPECL	–0.41	–0.41	ns
T_{OPCI33_3}		PCI, 33 MHz, 3.3V	2.3	2.3	ns
T_{OPCI66_3}		PCI, 66 MHz, 3.3V	–0.41	–0.41	ns
T_{OGTL}		GTL	0.49	0.49	ns
T_{OGTLP}		GTL+	0.8	0.8	ns
T_{OHSTL_I}		HSTL I	–0.51	–0.51	ns
T_{OHSTL_III}		HSTL III	–0.91	–0.91	ns
T_{OHSTL_IV}		HSTL IV	–1.01	–1.01	ns
T_{OSSTL2_I}		SSTL2 I	–0.51	–0.51	ns
T_{OSSLT2_II}		SSTL2 II	–0.91	–0.91	ns
T_{OSSTL3_I}		SSTL3 I	–0.51	–0.51	ns
T_{OSSTL3_II}		SSTL3 II	–1.01	–1.01	ns
T_{OCTT}		CTT	–0.61	–0.61	ns
T_{OAGP}		AGP	–0.91	–0.91	ns

Notes:

1. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see the tables Constants for Calculating T_{IOOP} and Delay Measurement Methodology, page 41.

Calculation of T_{IOOP} as a Function of Capacitance

T_{IOOP} is the propagation delay from the O Input of the IOB to the pad. The values for T_{IOOP} are based on the standard capacitive load (C_{SL}) for each I/O standard as listed in the table Constants for Calculating T_{IOOP}, below.

For other capacitive loads, use the formulas below to calculate an adjusted propagation delay, T_{IOOP1}.

$$T_{IOOP1} = T_{IOOP} + Adj + (C_{LOAD} - C_{SL}) * F_L$$

Where:

- Adj — is selected from IOB Output Delay Adjustments for Different Standards(1), page 40, according to the I/O standard used
- C_{LOAD} — is the capacitive load for the design
- F_L — is the capacitance scaling factor

Delay Measurement Methodology

Standard	V_L(1)	V_H(1)	Meas. Point	V_{REF} Typ(2)
LVTTL	0	3	1.4	-
LVCMOS2	0	2.5	1.125	-
PCI33_3	Per PCI Spec			-
PCI66_3	Per PCI Spec			-
GTL	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.80
GTL+	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.0
HSTL Class I	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL Class III	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL Class IV	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
SSTL3 I and II	V_{REF} – 1.0	V_{REF} + 1.0	V_{REF}	1.5
SSTL2 I and II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
CTT	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.5
AGP	V_{REF} – (0.2xV_{CCO})	V_{REF} + (0.2xV_{CCO})	V_{REF}	Per AGP Spec
LVDS	1.2 – 0.125	1.2 + 0.125	1.2	
LVPECL	1.6 – 0.3	1.6 + 0.3	1.6	

Notes:

1. Input waveform switches between V_L and V_H.
2. Measurements are made at V_{REF} Typ, Maximum, and Minimum. Worst-case values are reported.
3. I/O parameter measurements are made with the capacitance values shown in the following table, Constants for Calculating T_{IOOP}. Refer to Application Note XAPP179 for appropriate terminations.
4. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Constants for Calculating T_{IOOP}

Standard	C_{SL}(1) (pF)	F_L (ns/pF)
LVTTL Fast Slew Rate, 2 mA drive	35	0.41
LVTTL Fast Slew Rate, 4 mA drive	35	0.20
LVTTL Fast Slew Rate, 6 mA drive	35	0.13
LVTTL Fast Slew Rate, 8 mA drive	35	0.079
LVTTL Fast Slew Rate, 12 mA drive	35	0.044
LVTTL Fast Slew Rate, 16 mA drive	35	0.043
LVTTL Fast Slew Rate, 24 mA drive	35	0.033
LVTTL Slow Slew Rate, 2 mA drive	35	0.41
LVTTL Slow Slew Rate, 4 mA drive	35	0.20
LVTTL Slow Slew Rate, 6 mA drive	35	0.100
LVTTL Slow Slew Rate, 8 mA drive	35	0.086
LVTTL Slow Slew Rate, 12 mA drive	35	0.058
LVTTL Slow Slew Rate, 16 mA drive	35	0.050
LVTTL Slow Slew Rate, 24 mA drive	35	0.048
LVCMOS2	35	0.041
LVCMOS18	35	0.050
PCI 33 MHz 3.3V	10	0.050
PCI 66 MHz 3.3V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

Notes:

1. I/O parameter measurements are made with the capacitance values shown above. Refer to Application Note XAPP179 for appropriate terminations.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Pinout Tables

The following device-specific pinout tables include all packages available for each Spartan-IIE device. They follow the pad locations around the die. In the TQ144 package, all VCCO pins must be connected to the same voltage.

TQ144 Pinouts (XC2S50E and XC2S100E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
GND	-	P1	-	-
TMS	-	P2	-	-
I/O	7	P3	-	-
I/O	7	P4	-	-
I/O, VREF Bank 7	7	P5	-	All
I/O	7	P6	-	-
I/O, L27P	7	P7	XC2S50E	XC2S100E
I/O, L27N	7	P8	XC2S50E	-
GND	-	P9	-	-
I/O, L26P_YY	7	P10	All	-
I/O, L26N_YY	7	P11	All	-
I/O, VREF Bank 7, L25P	7	P12	XC2S50E	All
I/O, L25N	7	P13	XC2S50E	-
I/O	7	P14	-	-
I/O (IRDY)	7	P15	-	-
GND	-	P16	-	-
VCCO	-	P17	-	-
I/O (TRDY)	6	P18	-	-
VCCINT	-	P19	-	-
I/O	6	P20	-	-
I/O, L24P	6	P21	XC2S50E	-
I/O, VREF Bank 6, L24N	6	P22	XC2S50E	All
I/O, L23P_YY	6	P23	All	-
I/O, L23N_YY	6	P24	All	-
GND	-	P25	-	-
I/O, L22P	6	P26	XC2S50E	-

TQ144 Pinouts (XC2S50E and XC2S100E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L22N	6	P27	XC2S50E	XC2S100E
I/O	6	P28	-	-
I/O, VREF Bank 6	6	P29	-	All
I/O	6	P30	-	-
I/O, L21P_YY	6	P31	All	-
I/O, L21N_YY	6	P32	All	-
M1	-	P33	-	-
GND	-	P34	-	-
M0	-	P35	-	-
VCCO	-	P36	-	-
M2	-	P37	-	-
I/O, L20N_YY	5	P38	All	-
I/O, L20P_YY	5	P39	All	-
I/O	5	P40	-	-
I/O, VREF Bank 5	5	P41	-	All
I/O	5	P42	-	-
I/O, L19N_YY	5	P43	All	XC2S100E
I/O, L19P_YY	5	P44	All	-
GND	-	P45	-	-
VCCINT	-	P46	-	-
I/O, L18N_YY	5	P47	All	-
I/O, L18P_YY	5	P48	All	-
I/O, VREF Bank 5	5	P49	-	All
I/O (DLL), L17N	5	P50	-	-
VCCINT	-	P51	-	-
GCK1, I	5	P52	-	-
VCCO	5	P53	-	-
GND	-	P54	-	-
GCK0, I	4	P55	-	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L20P	2	D14	XC2S100E, 200E, 300E	XC2S200E, 300E, 400E
I/O (DIN, D0), L19N_YY	2	B16	All	-
I/O (DOUT, BUSY), L19P_YY	2	C15	All	-
CCLK	2	A15	-	-
TDO	2	B14	-	-
TDI	-	C13	-	-
I/O ($\overline{CS}$), L18P_YY	1	A14	All	-
I/O ($\overline{WRITE}$), L18N_YY	1	A13	All	-
I/O, L17P	1	B13	XC2S50E, 100E, 200E, 300E, 400E	XC2S200E, 300E, 400E
I/O, L17N	1	C12	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L16P_YY	1	B12	All	-
I/O, L16N_YY	1	A12	All	-
I/O, VREF Bank 1, L15P_YY	1	D12	All	All
I/O, L15N_YY	1	E11	All	-
I/O, L14P	1	D11	XC2S50E, 100E, 150E, 300E	-
I/O, L14N	1	C11	XC2S50E, 100E, 150E, 300E	-
I/O, L13P	1	B11	XC2S50E, 100E, 200E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L13N	1	A11	XC2S50E, 100E, 200E, 300E, 400E	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L12P	1	E10	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L12N	1	D10	XC2S50E, 100E, 200E, 300E, 400E	-
I/O	1	C10	-	-
I/O, L11P	1	B10	XC2S50E, 200E, 300E, 400E	-
I/O, L11N	1	A10	XC2S50E, 200E, 300E, 400E	-
I/O, VREF Bank 1, L10P	1	D9	XC2S50E, 200E, 300E, 400E	All
I/O, L10N	1	C9	XC2S50E, 200E, 300E, 400E	-
I/O, L9P	1	B9	XC2S50E, 150E, 200E, 400E	-
I/O, L9N	1	A9	XC2S50E, 150E, 200E, 400E	XC2S400E
I/O (DLL), L8P	1	A8	-	-
GCK2, I	1	B8	-	-
GCK3, I	0	C8	-	-
I/O (DLL), L8N	0	D8	-	-
I/O	0	A7	-	XC2S400E
I/O, L7P	0	E7	XC2S50E, 200E, 300E, 400E	-
I/O, VREF Bank 0, L7N	0	D7	XC2S50E, 200E, 300E, 400E	All

Additional FT256 Package Pins *(Continued)*

VCCO Bank 5 Pins				
L7	L8	M8	-	-
VCCO Bank 6 Pins				
J5	J6	K6	-	-
VCCO Bank 7 Pins				
G6	H5	H6	-	-
GND Pins				
A1	A16	B2	B15	F6
F11	G7	G8	G9	G10
H7	H8	H9	H10	J7
J8	J9	J10	K7	K8
K9	K10	L6	L11	R2
R15	T1	T16	-	-

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
GCK0, I	4	AA12	-	-	GCK0, I	GCK0, I	GCK0, I	GCK0, I	GCK0, I	GCK0, I
I/O (DLL), L#P	4	Y12	-	-	I/O (DLL), L53P	I/O (DLL), L70P	I/O (DLL), L75P	I/O (DLL), L75P	I/O (DLL), L75P	I/O (DLL), L75P
I/O	4	W12	-	-	-	-	-	I/O	I/O	I/O
I/O, L#N	4	V12	XC2S150E, 300E, 600E	-	-	I/O, L69N_Y	I/O, L74N	I/O, L74N_Y	I/O, L74N	I/O, L74N_Y
I/O, L#P	4	U12	XC2S150E, 300E, 600E	XC2S400E, 600E	I/O, L52N	I/O, L69P_Y	I/O, L74P	I/O, L74P_Y	I/O, VREF Bank 4, L74P	I/O, VREF Bank 4, L74P_Y
I/O, L#N	4	AB13	XC2S300E, 600E	-	I/O, L52P	I/O	I/O, L73N	I/O, L73N_Y	I/O, L73N	I/O, L73N_Y
I/O, L#P	4	AA13	XC2S300E, 600E	-	-	-	I/O, L73P	I/O, L73P_Y	I/O, L73P	I/O, L73P_Y
I/O	4	Y13	-	-	-	-	-	I/O	I/O	I/O
I/O, L#N	4	W13	XC2S200E, 300E, 400E, 600E	-	I/O, L51N	I/O, L68N	I/O, L72N_Y	I/O, L72N_Y	I/O, L72N_Y	I/O, L72N_Y
I/O, VREF Bank 4, L#P	4	V13	XC2S200E, 300E, 400E, 600E	All	I/O, VREF Bank 4, L51P	I/O, VREF Bank 4, L68P	I/O, VREF Bank 4, L72P_Y	I/O, VREF Bank 4, L72P_Y	I/O, VREF Bank 4, L72P_Y	I/O, VREF Bank 4, L72P_Y
I/O	4	U13	-	-	I/O, L50N	I/O, L67N	I/O	I/O	I/O	I/O
I/O, L#N	4	AB14	-	-	I/O, L50P	I/O, L67P	I/O, L71N	I/O, L71N	I/O, L71N	I/O, L71N
I/O, L#P	4	AA14	-	-	-	-	I/O, L71P	I/O, L71P	I/O, L71P	I/O, L71P
I/O	4	AB15	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#N	4	Y14	XC2S100E, 150E, 200E	-	I/O, L49N_Y	I/O, L66N_Y	I/O, L70N_Y	I/O, L70N	I/O, L70N	I/O, L70N
I/O, L#P	4	W14	XC2S100E, 150E, 200E	-	I/O, L49P_Y	I/O, L66P_Y	I/O, L70P_Y	I/O, L70P	I/O, L70P	I/O, L70P
I/O, L#N	4	U14	XC2S150E, 200E	-	-	I/O, L65N_Y	I/O, L69N_Y	I/O, L69N	I/O, L69N	I/O, L69N
I/O, L#P	4	V14	XC2S150E, 200E	-	-	I/O, L65P_Y	I/O, L69P_Y	I/O, L69P	I/O, L69P	I/O, L69P
I/O, L#N	4	AA15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L48N_Y	I/O, L64N	I/O, L68N_Y	I/O, L68N_Y	I/O, L68N_Y	I/O, L68N_Y
I/O, L#P	4	Y15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L48P_Y	I/O, L64P	I/O, L68P_Y	I/O, L68P_Y	I/O, L68P_Y	I/O, L68P_Y
I/O, L#N	4	W15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L47N_Y	I/O, L63N	I/O, L67N_Y	I/O, L67N_Y	I/O, L67N_Y	I/O, L67N_Y
I/O, VREF Bank 4, L#P	4	V15	XC2S100E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 4, L47P_Y	I/O, VREF Bank 4, L63P	I/O, VREF Bank 4, L67P_Y	I/O, VREF Bank 4, L67P_Y	I/O, VREF Bank 4, L67P_Y	I/O, VREF Bank 4, L67P_Y
I/O	4	AB16	-	-	-	-	-	I/O	I/O	I/O
I/O	4	AB17	-	-	I/O	I/O	I/O	I/O	I/O	I/O

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L201P	7	E4	XC2S400E	-	I/O, L201P_Y	I/O, L201P
I/O, L201N	7	F5	XC2S400E	-	I/O, L201N_Y	I/O, L201N
I/O, VREF Bank 7, L200P	7	F4	XC2S600E	All	I/O, VREF Bank 7, L200P	I/O, VREF Bank 7, L200P_Y
I/O, L200N	7	F3	XC2S600E	-	I/O, L200N	I/O, L200N_Y
I/O, L199P	7	F2	XC2S600E	-	-	I/O, L199P_Y
I/O, L199N	7	F1	XC2S600E	-	I/O	I/O, L199N_Y
I/O, L198P	7	G6	XC2S400E	-	I/O, L198P_Y	I/O, L198P
I/O, L198N	7	G5	XC2S400E	-	I/O, L198N_Y	I/O, L198N
I/O, L197P	7	G4	XC2S600E	-	I/O, L197P	I/O, L197P_Y
I/O, L197N	7	G3	XC2S600E	-	I/O, L197N	I/O, L197N_Y
I/O, VREF Bank 7, L196P_YY	7	G2	All	All	I/O, VREF Bank 7, L196P_YY	I/O, VREF Bank 7, L196P_YY
I/O, L196N_YY	7	G1	All	-	I/O, L196N_YY	I/O, L196N_YY
I/O	7	H7	-	-	I/O	I/O
I/O, L195P_YY	7	H6	All	-	I/O, L195P_YY	I/O, L195P_YY
I/O, L195N_YY	7	H5	All	-	I/O, L195N_YY	I/O, L195N_YY
I/O	7	J8	-	-	-	I/O
I/O, L194P	7	H2	XC2S400E	-	I/O, L194P_Y	I/O, L194P
I/O, L194N	7	H1	XC2S400E	-	I/O, L194N_Y	I/O, L194N
I/O, L193P	7	J7	XC2S600E	XC2S600E	I/O	I/O, VREF Bank 7, L193P_Y
I/O, L193N	7	J6	XC2S600E	-	-	I/O, L193N_Y
I/O	7	J5	-	-	I/O	I/O
I/O, L192P_YY	7	J4	All	-	I/O, L192P_YY	I/O, L192P_YY
I/O, L192N_YY	7	J3	All	-	I/O, L192N_YY	I/O, L192N_YY
I/O	7	K5	-	-	I/O	I/O
I/O, VREF Bank 7, L191P_YY	7	J2	All	All	I/O, VREF Bank 7, L191P_YY	I/O, VREF Bank 7, L191P_YY
I/O, L191N_YY	7	J1	All	-	I/O, L191N_YY	I/O, L191N_YY
I/O, L190P_YY	7	K8	All	-	I/O, L190P_YY	I/O, L190P_YY
I/O, L190N_YY	7	K7	All	-	I/O, L190N_YY	I/O, L190N_YY
I/O	7	K4	-	-	-	I/O
I/O, L189P_YY	7	K3	All	-	I/O, L189P_YY	I/O, L189P_YY
I/O, L189N_YY	7	K2	All	-	I/O, L189N_YY	I/O, L189N_YY
I/O	7	K1	-	-	-	I/O

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, VREF Bank 6, L176N	6	P9	XC2S600E	All	I/O, VREF Bank 6, L176N	I/O, VREF Bank 6, L176N_Y
I/O, L175P	6	R1	XC2S400E	-	I/O, L175P_Y	I/O, L175P
I/O, L175N	6	R2	XC2S400E	-	I/O, L175N_Y	I/O, L175N
I/O	6	R4	-	-	-	I/O
I/O, L174P_YY	6	R5	All	-	I/O, L174P_YY	I/O, L174P_YY
I/O, L174N_YY	6	R6	All	-	I/O, L174N_YY	I/O, L174N_YY
I/O	6	R7	-	-	-	I/O
I/O, L173P_YY	6	R8	All	-	I/O, L173P_YY	I/O, L173P_YY
I/O, VREF Bank 6, L173N_YY	6	R9	All	All	I/O, VREF Bank 6, L173N_YY	I/O, VREF Bank 6, L173N_YY
I/O, L172P	6	T1	XC2S600E	-	I/O, L172P	I/O, L172P_Y
I/O, L172N	6	T2	XC2S600E	-	I/O, L172N	I/O, L172N_Y
I/O	6	T3	-	-	-	I/O
I/O, L171P	6	T5	XC2S600E	-	I/O, L171P	I/O, L171P_Y
I/O, L171N	6	T6	XC2S600E	-	I/O, L171N	I/O, L171N_Y
I/O	6	U1	-	-	-	I/O
I/O, L170P	6	T7	XC2S600E	-	I/O, L170P	I/O, L170P_Y
I/O, L170N	6	T8	XC2S600E	-	I/O, L170N	I/O, L170N_Y
I/O, L169P	6	U2	XC2S400E	-	I/O, L169P_Y	I/O, L169P
I/O, L169N	6	U3	XC2S400E	-	I/O, L169N_Y	I/O, L169N
I/O	6	U7	-	-	-	I/O
I/O, L168P	6	U4	XC2S600E	-	-	I/O, L168P_Y
I/O, L168N	6	U5	XC2S600E	-	I/O	I/O, L168N_Y
I/O	6	U8	-	-	I/O	I/O
I/O, L167P_YY	6	V1	All	-	I/O, L167P_YY	I/O, L167P_YY
I/O, L167N_YY	6	V2	All	-	I/O, L167N_YY	I/O, L167N_YY
I/O	6	V3	-	-	I/O	I/O
I/O, VREF Bank 6, L166P_YY	6	V4	All	All	I/O, VREF Bank 6, L166P_YY	I/O, VREF Bank 6, L166P_YY
I/O, L166N_YY	6	V5	All	-	I/O, L166N_YY	I/O, L166N_YY
I/O, L165P_YY	6	V6	All	-	I/O, L165P_YY	I/O, L165P_YY
I/O, L165N_YY	6	V7	All	-	I/O, L165N_YY	I/O, L165N_YY
I/O	6	V8	-	-	-	I/O
I/O, L164P	6	W1	XC2S600E	-	I/O, L164P	I/O, L164P_Y

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L88P_YY	3	V25	All	-	I/O, L88P_YY	I/O, L88P_YY
I/O	3	V26	-	-	I/O	I/O
I/O, VREF Bank 3, L87N_YY	3	U19	All	All	I/O, VREF Bank 3, L87N_YY	I/O, VREF Bank 3, L87N_YY
I/O (D6), L87P_YY	3	U20	All	-	I/O (D6), L87P_YY	I/O (D6), L87P_YY
I/O (D5), L86N_YY	3	U22	All	-	I/O (D5), L86N_YY	I/O (D5), L86N_YY
I/O, L86P_YY	3	U23	All	-	I/O, L86P_YY	I/O, L86P_YY
I/O	3	U24	-	-	-	I/O
I/O, L85N	3	U25	XC2S600E	-	-	I/O, L85N_Y
I/O, L85P	3	U26	XC2S600E	-	I/O	I/O, L85P_Y
I/O	3	R18	-	-	I/O	I/O
I/O, L84N	3	T19	XC2S400E	-	I/O, L84N_Y	I/O, L84N
I/O, L84P	3	T20	XC2S400E	-	I/O, L84P_Y	I/O, L84P
I/O, L83N	3	T21	XC2S600E	-	I/O, L83N	I/O, L83N_Y
I/O, L83P	3	T22	XC2S600E	-	I/O, L83P	I/O, L83P_Y
I/O	3	T24	-	-	-	I/O
I/O, L82N	3	T25	XC2S600E	-	I/O, L82N	I/O, L82N_Y
I/O, L82P	3	T26	XC2S600E	-	I/O, L82P	I/O, L82P_Y
I/O	3	R19	-	-	-	I/O
I/O, L81N	3	R20	XC2S600E	-	I/O, L81N	I/O, L81N_Y
I/O, L81P	3	R21	XC2S600E	-	I/O, L81P	I/O, L81P_Y
I/O, VREF Bank 3, L80N_YY	3	R22	All	All	I/O, VREF Bank 3, L80N_YY	I/O, VREF Bank 3, L80N_YY
I/O (D4), L80P_YY	3	R23	All	-	I/O (D4), L80P_YY	I/O (D4), L80P_YY
I/O	3	P18	-	-	-	I/O
I/O, L79N_YY	3	R25	All	-	I/O, L79N_YY	I/O, L79N_YY
I/O, L79P_YY	3	R26	All	-	I/O, L79P_YY	I/O, L79P_YY
I/O	3	P19	-	-	-	I/O
I/O, L78N	3	P20	XC2S400E	-	I/O, L78N_Y	I/O, L78N
I/O, L78P	3	P21	XC2S400E	-	I/O, L78P_Y	I/O, L78P
I/O, VREF Bank 3, L77N	3	P22	XC2S600E	All	I/O, VREF Bank 3, L77N	I/O, VREF Bank 3, L77N_Y
I/O, L77P	3	P23	XC2S600E	-	I/O, L77P	I/O, L77P_Y
I/O	3	P24	-	-	-	I/O
I/O, L76N_YY	3	P25	All	-	I/O, L76N_YY	I/O, L76N_YY
I/O, L76P_YY	3	P26	All	-	I/O, L76P_YY	I/O, L76P_YY

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L14N_YY	0	E10	All	-	I/O, L14N_YY	I/O, L14N_YY
I/O	0	G10	-	-	-	I/O
I/O, L13P	0	A9	XC2S600E	-	I/O, L13P	I/O, L13P_Y
I/O, L13N	0	B9	XC2S600E	-	I/O, L13N	I/O, L13N_Y
I/O	0	H10	-	-	-	I/O
I/O, L12P_YY	0	C9	All	-	I/O, L12P_YY	I/O, L12P_YY
I/O, L12N_YY	0	D9	All	-	I/O, L12N_YY	I/O, L12N_YY
I/O	0	E9	-	-	I/O	I/O
I/O, VREF Bank 0, L11P	0	F9	-	All	I/O, VREF Bank 0, L11P	I/O, VREF Bank 0, L11P
I/O, L11N	0	G9	-	-	I/O, L11N	I/O, L11N
I/O, L10P	0	A8	-	-	I/O, L10P	I/O, L10P
I/O, L10N	0	B8	-	-	I/O, L10N	I/O, L10N
I/O	0	H9	-	-	I/O	I/O
I/O, L9P	0	E8	XC2S600E	-	I/O	I/O, L9P_Y
I/O, L9N	0	F8	XC2S600E	XC2S600E	-	I/O, VREF Bank 0, L9N_Y
I/O, L8P	0	A7	XC2S600E	-	I/O, L8P	I/O, L8P_Y
I/O, L8N	0	B7	XC2S600E	-	I/O, L8N	I/O, L8N_Y
I/O	0	G8	-	-	I/O	I/O
I/O, L7P_YY	0	C7	All	-	I/O, L7P_YY	I/O, L7P_YY
I/O, L7N_YY	0	D7	All	-	I/O, L7N_YY	I/O, L7N_YY
I/O	0	E7	-	-	-	I/O
I/O, L6P_YY	0	F7	All	-	I/O, L6P_YY	I/O, L6P_YY
I/O, VREF Bank 0, L6N_YY	0	G7	All	All	I/O, VREF Bank 0, L6N_YY	I/O, VREF Bank 0, L6N_YY
I/O	0	A6	-	-	I/O	I/O
I/O, L5P	0	B6	-	-	I/O, L5P	I/O, L5P
I/O, L5N	0	C6	-	-	I/O, L5N	I/O, L5N
I/O, L4P	0	D6	-	-	I/O, L4P	I/O, L4P
I/O, L4N	0	E6	-	-	I/O, L4N	I/O, L4N
I/O	0	F6	-	-	-	I/O
I/O, L3P_YY	0	A5	All	-	I/O, L3P_YY	I/O, L3P_YY
I/O, VREF Bank 0, L3N_YY	0	B5	All	All	I/O, VREF Bank 0, L3N_YY	I/O, VREF Bank 0, L3N_YY
I/O, L2P_YY	0	D5	All	-	I/O, L2P_YY	I/O, L2P_YY

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L2N_YY	0	E5	All	-	I/O, L2N_YY	I/O, L2N_YY
I/O, L1P_YY	0	B4	All	-	I/O, L1P_YY	I/O, L1P_YY
I/O, L1N_YY	0	C4	All	-	I/O, L1N_YY	I/O, L1N_YY
I/O, L0P	0	A3	XC2S600E	-	I/O	I/O, L0P_Y
I/O, L0N	0	B3	XC2S600E	-	-	I/O, L0N_Y
I/O	0	A4	-	-	I/O	I/O
TCK	-	A2	-	-	TCK	TCK

FG676 Differential Clock Pins

Clock	Bank	P Input		N Input	
		Pin	Name	Pin	Name
GCK0	4	AF14	GCK0, I	AE14	I/O (DLL), L126P
GCK1	5	AF13	GCK1, I	AE13	I/O (DLL), L126N
GCK2	1	A14	GCK2, I	B14	I/O (DLL), L23P
GCK3	0	A13	GCK3, I	B13	I/O (DLL), L23N

Additional FG676 Package Pins

VCCINT Pins						
H8	H19	J9	J18	K10	K11	K16
K17	L10	L17	T10	T17	U10	U11
U16	U17	V9	V18	W8	W19	-
VCCO Bank 0 Pins						
C5	C8	D11	J10	J11	K12	K13
VCCO Bank 1 Pins						
C19	C22	D16	J16	J17	K14	K15
VCCO Bank 2 Pins						
E24	H24	K18	L18	L23	M17	N17
VCCO Bank 3 Pins						
P17	R17	T18	T23	U18	W24	AB24
VCCO Bank 4 Pins						
U14	U15	V16	V17	AC16	AD19	AD22
VCCO Bank 5 Pins						
U12	U13	V10	V11	AC11	AD5	AD8
VCCO Bank 6 Pins						
P10	R10	T4	T9	U9	W3	AB3
VCCO Bank 7 Pins						
H3	K9	L4	L9	M10	N10	E3