# AMD Xilinx - XC2S50E-6PQ208I Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 384 |
| Number of Logic Elements/Cells | 1728 |
| Total RAM Bits | 32768 |
| Number of I/O | 146 |
| Number of Gates | 50000 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2s50e-6pq208i |

# Architectural Description

## Spartan-IIE FPGA Array

The Spartan®-IIE user-programmable gate array, shown in Figure 3, is composed of five major configurable elements:

- IOBs provide the interface between the package pins and the internal logic
- CLBs provide the functional elements for constructing most logic
- Dedicated block RAM memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- Versatile multi-level interconnect structure

As can be seen in Figure 3, the CLBs form the central logic structure with easy access to all support and routing structures. The IOBs are located around all the logic and memory elements for easy and quick routing of signals on and off the chip.

Values stored in static memory cells control all the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

Each of these elements will be discussed in detail in the following sections.

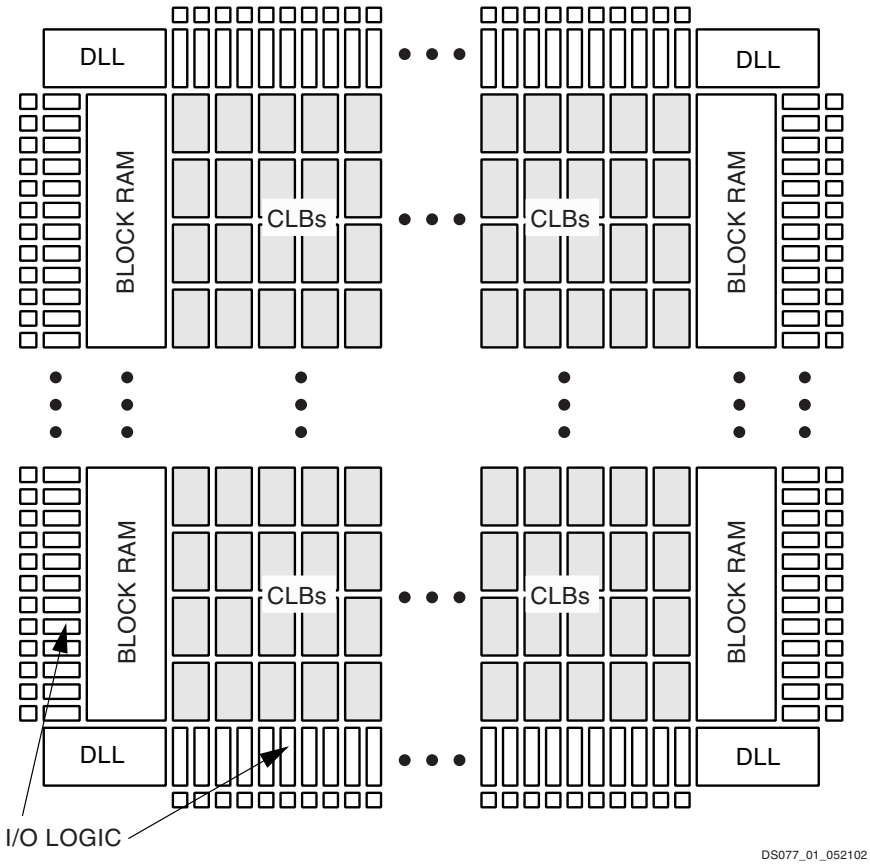



*Figure 3:* **Basic Spartan-IIE Family FPGA Block Diagram**

## Configurable Logic Block

The basic building block of the Spartan-IIE FPGA CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and storage element. The output from the function generator in each LC drives the CLB output or the D input of the flip-flop. Each Spartan-IIE FPGA CLB contains four LCs, organized in two similar slices; a single slice is shown in Figure 6.

In addition to the four basic LCs, the Spartan-IIE FPGA CLB contains logic that combines function generators to provide functions of five or six inputs.

### *Look-Up Tables*

Spartan-IIE FPGA function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16 x 1-bit dual-port synchronous RAM.

The Spartan-IIE FPGA LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

### *Storage Elements*

Storage elements in the Spartan-IIE FPGA slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals may be configured to operate asynchronously.

All control signals are independently invertible, and are shared by the two flip-flops within the slice.

During start-up, the device performs four operations:

1. The assertion of DONE. The failure of DONE to go High may indicate the unsuccessful loading of configuration data.
2. The release of the Global Three State (GTS). This activates all the I/Os to which signals are assigned. The remaining I/Os stay in a high-impedance state with internal weak pull-up resistors present.
3. The release of the Global Set Reset (GSR). This allows all flip-flops to change state.
4. The assertion of Global Write Enable (GWE). This allows all RAMs and flip-flops to change state.

By default, these operations are synchronized to CCLK. The entire start-up sequence lasts eight cycles, called C0-C7, after which the loaded design is fully functional. The four operations can be selected to switch on any CCLK cycle C1-C6 through settings in the Xilinx Development Software. The default timing for start-up is shown in the top half of Figure 17; heavy lines show default settings.

The default Start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The bottom half of Figure 17 shows another commonly used version of the start-up timing known as Sync-to-DONE. This version makes the GTS, GSR, and GWE events conditional upon the DONE pin going High. This timing is important for a daisy chain of multiple FPGAs in serial mode, since it ensures that all FPGAs go through start-up together, after all their DONE pins have gone High.

Sync-to-DONE timing is selected by setting the GTS, GSR, and GWE cycles to a value of DONE in the configuration options. This causes these signals to transition one clock cycle after DONE externally transitions High.

The sequence can also be paused at any stage until lock has been achieved on any or all DLLs.

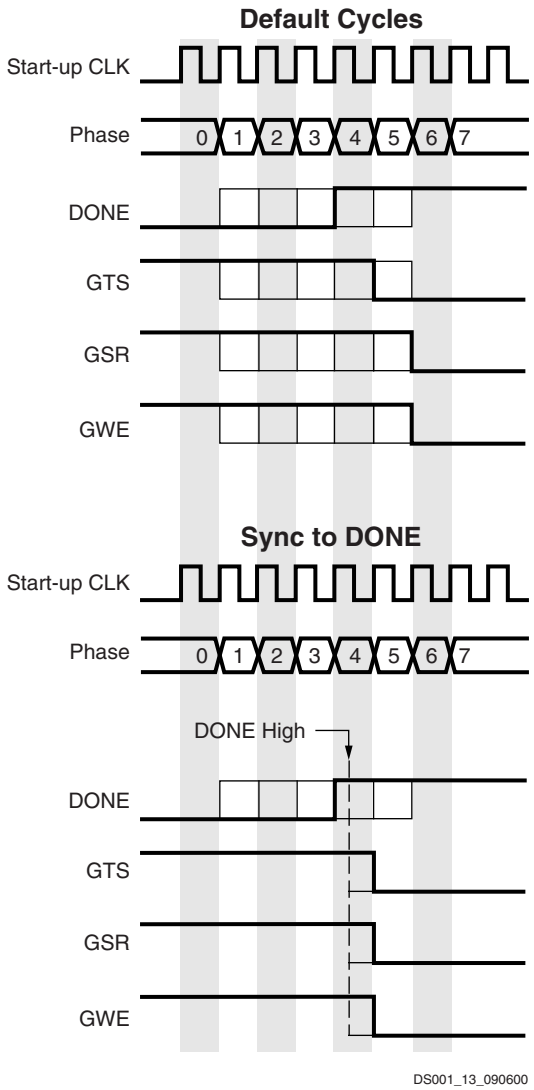



*Figure 17:* **Start-Up Waveforms**

## Serial Modes

There are two serial configuration modes. In Master Serial mode, the FPGA controls the configuration process by driving CCLK as an output. In Slave Serial mode, the FPGA passively receives CCLK as an input from an external agent (e.g., a microprocessor, CPLD, or second FPGA in master mode) that is controlling the configuration process. In both modes, the FPGA is configured by loading one bit per CCLK cycle. The MSB of each configuration data byte is always written to the DIN pin first.

See Figure 18 for the sequence for loading data into the Spartan-IIE FPGA serially. This is an expansion of the "Load Configuration Data Frames" block in Figure 16, page 23. Note that $\overline{CS}$ and $\overline{WRITE}$ are not normally used during serial configuration. To ensure successful loading of the FPGA, do not toggle $\overline{WRITE}$ with $\overline{CS}$ Low during serial configuration.

## Power-On Requirements

Spartan®-IIE FPGAs require that a minimum supply current $I_{CCPO}$ be provided to the $V_{CCINT}$ lines for a successful power-on. If more current is available, the FPGA can consume more than $I_{CCPO}$ min., though this cannot adversely affect reliability.

A maximum limit for $I_{CCPO}$ is not specified. Be careful when using foldback/crowbar supplies and fuses. It is possible to control the magnitude of $I_{CCPO}$ by limiting the supply current available to the FPGA. A current limit below the trip level will avoid inadvertently activating over-current protection circuits.

| Symbol | Description | | | | Min(1) | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $I_{CCPO}$ | Total $V_{CCINT}$ supply current required during power-on | Commercial | XC2S50E - XC2S300E | After PCN(2) | 300 | - | - | mA |
| | | | | Before PCN(2) | 500 | - | - | mA |
| | | | XC2S400E - XC2S600E | | 500 | - | - | mA |
| | | Industrial | XC2S50E - XC2S300E | After PCN(2) | 500 | - | - | mA |
| | | | | Before PCN(2) | 2 | - | - | A |
| | | | XC2S400E - XC2S600E | | 700 | - | - | mA |
| $T_{CCPO}$ | $V_{CCINT}$(3,4) ramp time | | After PCN(2) | | 500 | - | - | µs |
| | | | Before PCN(2) | | 2 | - | 50 | ms |
| $I_{HSPO}$ | AC current per pin during power-on in hot-swap applications when $V_{IN} > V_{CCO} + 0.4V$; duration < 10ns | | After PCN(2) | | - | ±60 | - | µA |

**Notes:**
1. The $I_{CCPO}$ requirement applies for a brief time (commonly only a few milliseconds) when $V_{CCINT}$ ramps from 0 to 1.8V.
2. Devices built after the Product Change Notice PCN 2002-05 (see http://www.xilinx.com/support/documentation/customer_notices/pcn2002-05.pdf) have improved power-on requirements. Devices after the PCN have a 'T' preceding the date code as referenced in the PCN. Note that the XC2S150E, XC2S400E, and XC2S600E always have this mark. Devices before the PCN have an 'S' preceding the date code. Note that devices before the PCN are measured with $V_{CCINT}$ and $V_{CCO}$ powering up simultaneously.
3. The ramp time is measured from GND to 1.8V on a fully loaded board.
4. $V_{CCINT}$ must not dip in the negative direction during power on.
5. I/Os are not guaranteed to be disabled until $V_{CCINT}$ is applied.
6. For more information on designing to meet the power-on specifications, refer to the application note XAPP450 "Power-On Current Requirements for the Spartan-II and Spartan-IIE Families".

## DC Input and Output Levels

Values for $V_{IL}$ and $V_{IH}$ are recommended input voltages. Values for $V_{OL}$ and $V_{OH}$ are guaranteed output voltages over the recommended operating conditions. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum $V_{CCO}$ with the respective $I_{OL}$ and $I_{OH}$ currents shown. Other standards are sample tested.

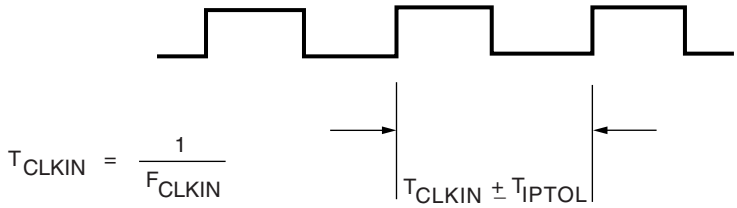
| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| LVTTL(1) | –0.5 | 0.8 | 2.0 | 3.6 | 0.4 | 2.4 | 24 | –24 |
| LVCMOS2 | –0.5 | 0.7 | 1.7 | 2.7 | 0.4 | 1.9 | 12 | –12 |
| LVCMOS18 | –0.5 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | 1.95 | 0.4 | $V_{CCO}$ – 0.4 | 8 | –8 |
| PCI, 3.3V | –0.5 | 30% $V_{CCO}$ | 50% $V_{CCO}$ | $V_{CCO}$ + 0.5 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | Note (2) | Note (2) |
| GTL | –0.5 | $V_{REF}$ – 0.05 | $V_{REF}$ + 0.05 | 3.6 | 0.4 | - | 40 | - |
| GTL+ | –0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.6 | - | 36 | - |

## IOB Input Delay Adjustments for Different Standards

Input delays associated with the pad are specified for LVTTL. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

| Symbol | Description | Standard | Speed Grade | | Units |
|---|---|---|---|---|---|
| | | | -7 | -6 | |
| **Data Input Delay Adjustments** | | | | | |
| $T_{ILVTTL}$ | Standard-specific data input delay adjustments | LVTTL | 0 | 0 | ns |
| $T_{ILVCMOS2}$ | | LVCMOS2 | 0 | 0 | ns |
| $T_{ILVCMOS18}$ | | LVCMOS18 | 0.20 | 0.20 | ns |
| $T_{ILVDS}$ | | LVDS | 0.15 | 0.15 | ns |
| $T_{ILVPECL}$ | | LVPECL | 0.15 | 0.15 | ns |
| $T_{IPCI33\_3}$ | | PCI, 33 MHz, 3.3V | 0.08 | 0.08 | ns |
| $T_{IPCI66\_3}$ | | PCI, 66 MHz, 3.3V | –0.11 | –0.11 | ns |
| $T_{IGTL}$ | | GTL | 0.14 | 0.14 | ns |
| $T_{IGTLP}$ | | GTL+ | 0.14 | 0.14 | ns |
| $T_{IHSTL}$ | | HSTL | 0.04 | 0.04 | ns |
| $T_{ISSTL2}$ | | SSTL2 | 0.04 | 0.04 | ns |
| $T_{ISSTL3}$ | | SSTL3 | 0.04 | 0.04 | ns |
| $T_{ICTT}$ | | CTT | 0.10 | 0.10 | ns |
| $T_{IAGP}$ | | AGP | 0.04 | 0.04 | ns |

***Period Tolerance:*** the allowed input clock period change in nanoseconds.




***Output Jitter:*** the difference between an ideal reference clock edge and the actual design.

***Phase Offset and Maximum Phase Difference***

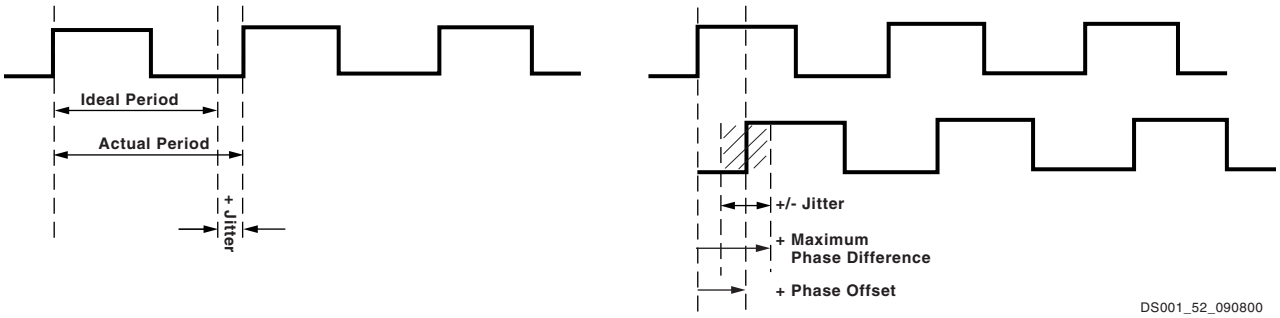



*Figure 22:* **Period Tolerance and Clock Jitter**

## CLB Distributed RAM Switching Characteristics

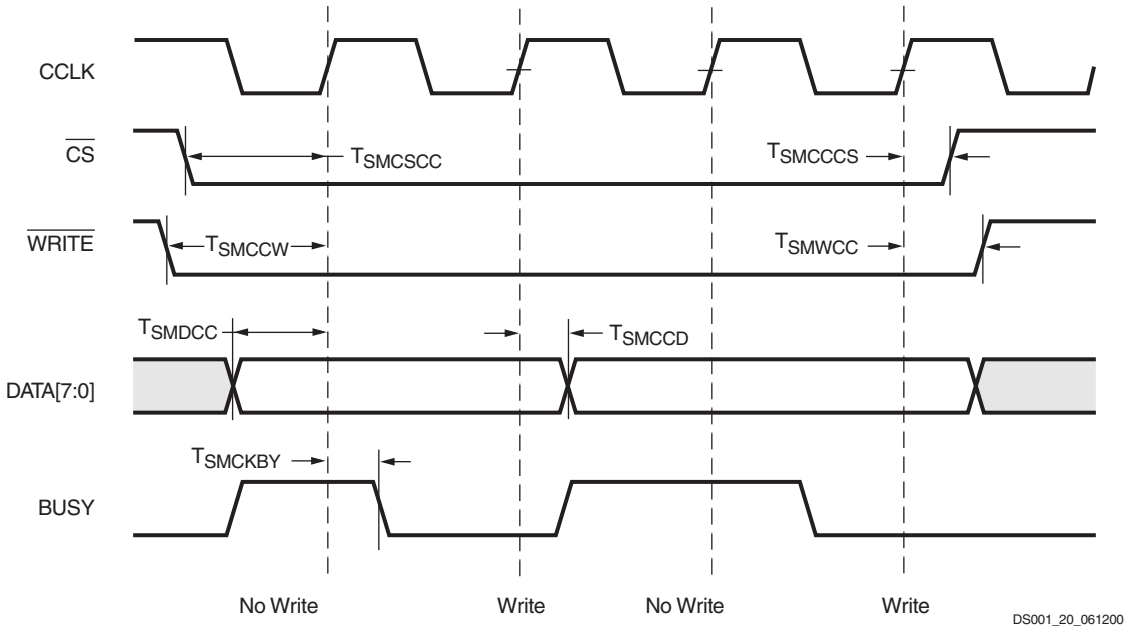
| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -7 | | -6 | | |
| | | Min | Max | Min | Max | |
| **Sequential Delays** | | | | | | |
| $T_{SHCKO16}$ | Clock CLK to X/Y outputs (WE active, 16 x 1 mode) | 0.6 | 1.5 | 0.6 | 1.7 | ns |
| $T_{SHCKO32}$ | Clock CLK to X/Y outputs (WE active, 32 x 1 mode) | 0.8 | 1.9 | 0.8 | 2.1 | ns |
| **Setup/Hold Times with Respect to Clock CLK** | | | | | | |
| $T_{AS}$ / $T_{AH}$ | F/G address inputs | 0.42 / 0 | - | 0.5 / 0 | - | ns |
| $T_{DS}$ / $T_{DH}$ | BX/BY data inputs (DIN) | 0.53 / 0 | - | 0.6 / 0 | - | ns |
| $T_{WS}$ / $T_{WH}$ | CE input (WS) | 0.7 / 0 | - | 0.8 / 0 | - | ns |
| **Clock CLK** | | | | | | |
| $T_{WPH}$ | Pulse width, High | 2.1 | - | 2.4 | - | ns |
| $T_{WPL}$ | Pulse width, Low | 2.1 | - | 2.4 | - | ns |
| $T_{WC}$ | Clock period to meet address write cycle time | 4.2 | - | 4.8 | - | ns |

## CLB Shift Register Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -7 | | -6 | | |
| | | Min | Max | Min | Max | |
| **Sequential Delays** | | | | | | |
| $T_{REG}$ | Clock CLK to X/Y outputs | 1.2 | 2.9 | 1.2 | 3.2 | ns |
| **Setup/Hold Times with Respect to Clock CLK** | | | | | | |
| $T_{SHDICK}$ | BX/BY data inputs (DIN) | 0.53 / 0 | - | 0.6 / 0 | - | ns |
| $T_{SHCECK}$ | CE input (WS) | 0.7 / 0 | - | 0.8 / 0 | - | ns |
| **Clock CLK** | | | | | | |
| $T_{SRPH}$ | Pulse width, High | 2.1 | - | 2.4 | - | ns |
| $T_{SRPL}$ | Pulse width, Low | 2.1 | - | 2.4 | - | ns |

## Block RAM Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -7 | | -6 | | |
| | | Min | Max | Min | Max | |
| **Sequential Delays** | | | | | | |
| $T_{BCKO}$ | Clock CLK to DOUT output | 0.6 | 3.1 | 0.6 | 3.5 | ns |
| **Setup/Hold Times with Respect to Clock CLK** | | | | | | |
| $T_{BACK}$ / $T_{BCKA}$ | ADDR inputs | 1.0 / 0 | - | 1.1 / 0 | - | ns |
| $T_{BDCK}$/ $T_{BCKD}$ | DIN inputs | 1.0 / 0 | - | 1.1 / 0 | - | ns |
| $T_{BECK}$/ $T_{BCKE}$ | EN inputs | 2.2 / 0 | - | 2.5 / 0 | - | ns |
| $T_{BRCK}$/ $T_{BCKR}$ | RST input | 2.1 / 0 | - | 2.3 / 0 | - | ns |
| $T_{BWCK}$/ $T_{BCKW}$ | WEN input | 2.0 / 0 | - | 2.2 / 0 | - | ns |
| **Clock CLK** | | | | | | |
| $T_{BPWH}$ | Pulse width, High | 1.4 | - | 1.5 | - | ns |
| $T_{BPWL}$ | Pulse width, Low | 1.4 | - | 1.5 | - | ns |
| $T_{BCCS}$ | CLKA -> CLKB setup time for different ports | 2.7 | - | 3.0 | - | ns |




| Symbol | | Description | All Devices | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $T_{SMDCC}$ / $T_{SMCCD}$ | CCLK | D0-D7 setup/hold | 5 / 1 | - | ns |
| $T_{SMCSCC}$ / $T_{SMCCCS}$ | | $\overline{CS}$ setup/hold | 7 / 1 | - | ns |
| $T_{SMCCW}$ / $T_{SMWCC}$ | | $\overline{WRITE}$ setup/hold | 7 / 1 | - | ns |
| $T_{SMCKBY}$ | | BUSY propagation delay | - | 12 | ns |
| $F_{CC}$ | | Frequency | - | 66 | MHz |
| $F_{CCNH}$ | | Frequency with no handshake | - | 50 | MHz |

*Figure 26:* **Slave Parallel (SelectMAP) Mode Write Timing**

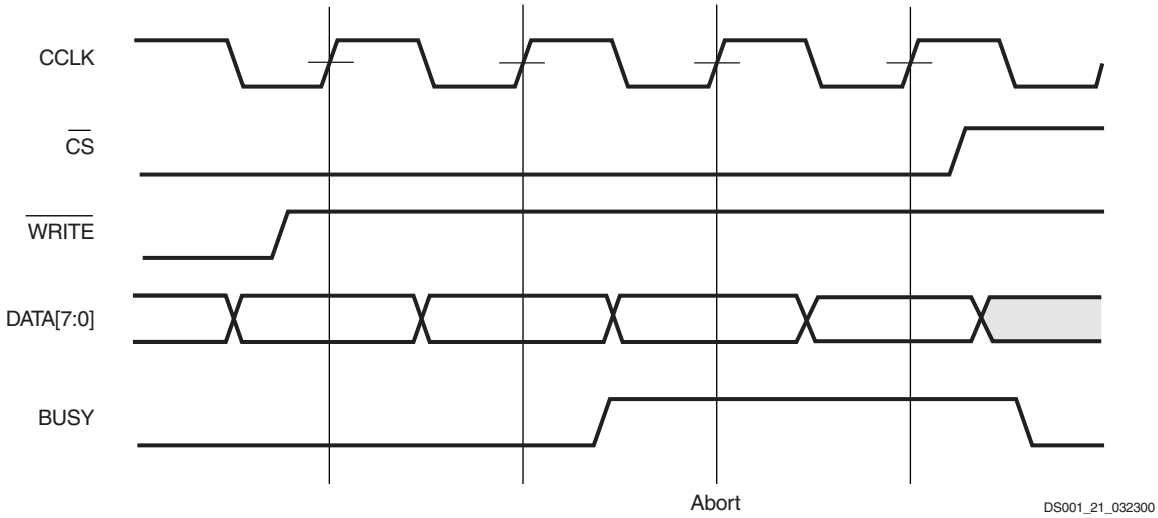



*Figure 27:* **Slave Parallel (SelectMAP) Mode Write Abort Waveforms**

## Low Voltage Differential Signals (LVDS and LVPECL)

The Spartan-IIE family features low-voltage differential signaling (LVDS and LVPECL). Each signal utilizes two pins on the Spartan-IIE device, known as differential pin pairs. Each differential pin pair has a Positive (P) and a Negative (N) pin. These pairs are labeled in the following manner.

I/O, L#[P/N][-/_Y/_YY]

where

L = LVDS or LVPECL pin

# = Pin pair number

P = Positive

N = Negative

_Y = Asynchronous output allowed (device-dependent)

_YY = Asynchronous output allowed (all devices)

### Available Differential Pairs According to Package Type

| Device | TQ144 | PQ208 | FT256 | FG456 | FG676 |
|---|---|---|---|---|---|
| XC2S50E | 28 | 50 | 83 | - | - |
| XC2S100E | 28 | 50 | 83 | 86 | - |
| XC2S150E | - | 50 | 83 | 114 | - |
| XC2S200E | - | 50 | 83 | 120 | - |
| XC2S300E | - | 50 | 83 | 120 | - |
| XC2S400E | - | - | 83 | 120 | 172 |
| XC2S600E | - | - | - | 120 | 205 |

### Synchronous or Asynchronous

I/O pins for differential signals can either be synchronous or asynchronous, input or output. Differential signaling requires the pins of each pair to switch simultaneously. If the output signals driving the pins are from IOB flip-flops, they are synchronous. If the signals driving the pins are from internal logic, they are asynchronous, and therefore more care must be taken that they are simultaneous. Any differential pairs can be used for synchronous input and output signals as well as asynchronous input signals.

However, only the differential pairs with the _Y or _YY suffix can be used for asynchronous output signals.

### Asynchronous Output Pad Name Designation

Because of differences between densities, the differential pairs that can be used for asynchronous outputs vary by device. The pairs that are available in all densities for a given package have the _YY suffix. These pins should be used for differential asynchronous outputs if the design may later move to a different density. All other differential pairs that can be used for asynchronous outputs have the _Y suffix.

To simplify the following tables, the "Pad Name" column shows the part of the name that is common across densities. The "Pad Name" column leaves out the _Y suffix and the "LVDS Asynchronous Output Option" column indicates the densities that allow asynchronous outputs for LVDS or LVPECL on the given pin.

### DLL Pins

Pins labeled "I/O (DLL)" can be used as general-purpose I/O or as inputs to the DLL. Adjacent DLL pins form a differential pair. They reside in two different banks, so if they are outputs the $V_{CCO}$ level must be the same for both banks. Each DLL pin can also be paired with the adjacent GCK clock pin for a differential clock input. The "I/O (DLL)" pin always becomes the N terminal when paired with GCK, even if it is labeled "P" for its pairing with the adjacent DLL pin.

### VREF Pins

Pins labeled "I/O, VREF" can be used as either an I/O or a VREF pin. If any I/O pin within the bank requires a VREF input, all the VREF pins in the bank must be connected to the same voltage. See the I/O banking rules in the Functional Description module for more detail. If no pin in a given bank requires VREF, then that bank's VREF pins can be used as general I/O.

To simplify the following tables, the "Pad Name" column shows the part of the name that is common across densities. When VREF is only available in limited densities, the "Pad Name" column leaves out the VREF designation and the "VREF Option" column indicates the densities that provide VREF on the given pin.

### VCCO Banks

In the TQ144 and PQ208 packages, the eight banks have VCCO connected together. Thus, only one VCCO is allowed in these packages, although different VREF values are allowed in each of the eight banks. See I/O Banking.

## PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| I/O, VREF Bank 6, L39P | 6 | P45 | XC2S100E, 150E | All |
| I/O, L39N | 6 | P46 | XC2S100E, 150E | - |
| I/O | 6 | P47 | - | XC2S200E, 300E |
| I/O, L38P_YY | 6 | P48 | All | - |
| I/O, L38N_YY | 6 | P49 | All | - |
| M1 | - | P50 | - | - |
| GND | - | P51 | - | - |
| M0 | - | P52 | - | - |
| VCCO | - | P53 | - | - |
| M2 | - | P54 | - | - |
| | | | | |
| I/O, L37N_YY | 5 | P55 | All | - |
| I/O, L37P_YY | 5 | P56 | All | - |
| I/O | 5 | P57 | - | XC2S200E, 300E |
| I/O | 5 | P58 | - | - |
| I/O, VREF Bank 5, L36N_YY | 5 | P59 | All | All |
| I/O, L36P_YY | 5 | P60 | All | - |
| I/O, L35N | 5 | P61 | XC2S50E, 100E, 300E | - |
| I/O, L35P | 5 | P62 | XC2S50E, 100E, 300E | - |
| I/O, L34N | 5 | P63 | XC2S50E, 100E, 200E, 300E | XC2S100E, 150E, 200E, 300E |
| I/O, L34P | 5 | P64 | XC2S50E, 100E, 200E, 300E | - |
| GND | - | P65 | - | - |

## PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| VCCO | - | P66 | - | - |
| VCCINT | - | P67 | - | - |
| I/O, L33N | 5 | P68 | XC2S50E, 100E, 200E, 300E | - |
| I/O, L33P | 5 | P69 | XC2S50E, 100E, 200E, 300E | - |
| I/O | 5 | P70 | - | - |
| I/O, L32N | 5 | P71 | XC2S100E, 150E | - |
| GND | - | P72 | - | - |
| I/O, VREF Bank 5, L32P | 5 | P73 | XC2S100E, 150E | All |
| I/O | 5 | P74 | - | - |
| I/O (DLL), L31N | 5 | P75 | - | - |
| VCCINT | - | P76 | - | - |
| GCK1, I | 5 | P77 | - | - |
| VCCO | - | P78 | - | - |
| GND | - | P79 | - | - |
| | | | | |
| GCK0, I | 4 | P80 | - | - |
| I/O (DLL), L31P | 4 | P81 | - | - |
| I/O | 4 | P82 | - | - |
| I/O, L30N | 4 | P83 | XC2S50E, 200E, 300E | - |
| I/O, VREF Bank 4, L30P | 4 | P84 | XC2S50E, 200E, 300E | All |
| GND | - | P85 | - | - |
| I/O, L29N | 4 | P86 | XC2S50E, 200E, 300E | - |
| I/O, L29P | 4 | P87 | XC2S50E, 200E, 300E | - |
| I/O, L28N | 4 | P88 | XC2S50E, 100E, 200E, 300E | - |

## PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| I/O | 2 | P134 | - | - |
| I/O (D3), L17N | 2 | P135 | XC2S50E, 300E | - |
| I/O, VREF Bank 2, L17P | 2 | P136 | XC2S50E, 300E | All |
| GND | - | P137 | - | - |
| I/O, L16N_YY | 2 | P138 | All | - |
| I/O, L16P_YY | 2 | P139 | All | - |
| I/O, L15N_YY | 2 | P140 | All | - |
| I/O (D2), L15P_YY | 2 | P141 | All | - |
| VCCINT | - | P142 | - | - |
| VCCO | - | P143 | - | - |
| GND | - | P144 | - | - |
| I/O (D1), L14N | 2 | P145 | XC2S50E, 300E | - |
| I/O, L14P | 2 | P146 | XC2S50E, 300E | XC2S100E, 150E, 200E, 300E |
| I/O | 2 | P147 | - | - |
| I/O | 2 | P148 | - | - |
| I/O | 2 | P149 | - | - |
| I/O, VREF Bank 2, L13N | 2 | P150 | XC2S100E, 150E | All |
| I/O, L13P | 2 | P151 | XC2S100E, 150E | - |
| I/O | 2 | P152 | - | XC2S200E, 300E |
| I/O (DIN, D0), L12N_YY | 2 | P153 | All | - |
| I/O (DOUT, BUSY), L12P_YY | 2 | P154 | All | - |
| CCLK | 2 | P155 | - | - |

## PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option |
|---|---|---|---|---|
| Function | Bank | | | |
| VCCO | - | P156 | - | - |
| TDO | 2 | P157 | - | - |
| GND | - | P158 | - | - |
| TDI | - | P159 | - | - |
| | | | | |
| I/O ($\overline{CS}$), L11P_YY | 1 | P160 | All | - |
| I/O ($\overline{WRITE}$), L11N_YY | 1 | P161 | All | - |
| I/O | 1 | P162 | - | XC2S200E, 300E |
| I/O | 1 | P163 | - | - |
| I/O, VREF Bank 1, L10P_YY | 1 | P164 | All | All |
| I/O, L10N_YY | 1 | P165 | All | - |
| I/O | 1 | P166 | - | - |
| I/O | 1 | P167 | - | - |
| I/O, L9P | 1 | P168 | XC2S50E, 100E, 200E, 300E | XC2S100E, 150E, 200E, 300E |
| I/O, L9N | 1 | P169 | XC2S50E, 100E, 200E, 300E | - |
| GND | - | P170 | - | - |
| VCCO | - | P171 | - | - |
| VCCINT | - | P172 | - | - |
| I/O, L8P | 1 | P173 | XC2S50E, 100E, 200E, 300E | - |
| I/O, L8N | 1 | P174 | XC2S50E, 100E, 200E, 300E | - |
| I/O, L7P | 1 | P175 | XC2S50E, 200E, 300E | - |
| I/O, L7N | 1 | P176 | XC2S50E, 200E, 300E | - |
| GND | - | P177 | - | - |

## FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

| Pad Name | | | LVDS Async. Output Option | $V_{REF}$ Option | Device-Specific Pinouts: XC2S | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Function | Bank | Pin | | | 100E | 150E | 200E | 300E | 400E | 600E |
| I/O | 7 | H5 | - | - | - | - | - | I/O | I/O | I/O |
| I/O, VREF Bank 7, L#P_Y | 7 | H3 | XC2S300E, 400E, 600E | All | I/O, VREF Bank 7, L81P | I/O, VREF Bank 7, L106P | I/O, VREF Bank 7, L113P | I/O, VREF Bank 7, L113P_Y | I/O, VREF Bank 7, L113P_Y | I/O, VREF Bank 7, L113P_Y |
| I/O, L#N_Y | 7 | H4 | XC2S300E, 400E, 600E | - | I/O, L81N | I/O, L106N | I/O, L113N | I/O, L113N_Y | I/O, L113N_Y | I/O, L113N_Y |
| I/O, L#P_YY | 7 | H2 | All | - | I/O, L80P_YY | I/O, L105P_YY | I/O, L112P_YY | I/O, L112P_YY | I/O, L112P_YY | I/O, L112P_YY |
| I/O, L#N_YY | 7 | H1 | All | - | I/O, L80N_YY | I/O, L105N_YY | I/O, L112N_YY | I/O, L112N_YY | I/O, L112N_YY | I/O, L112N_YY |
| I/O | 7 | J6 | - | - | - | - | I/O | I/O | I/O | I/O |
| I/O, L#P_Y | 7 | J4 | XC2S150E, 200E, 300E, 400E | - | - | I/O, L104P_Y | I/O, L111P_Y | I/O, L111P_Y | I/O, L111P_Y | I/O, L111P |
| I/O, L#N_Y | 7 | J5 | XC2S100E, 150E, 200E, 300E, 400E | - | I/O, L79P_Y | I/O, L104N_Y | I/O, L111N_Y | I/O, L111N_Y | I/O, L111N_Y | I/O, L111N |
| I/O, L#P_Y | 7 | J3 | XC2S100E, 150E, 200E, 300E, 600E | - | I/O, L79N_Y | I/O, L103P_Y | I/O, L110P_Y | I/O, L110P_Y | I/O, L110P | I/O, L110P_Y |
| I/O, L#N_Y | 7 | J2 | XC2S150E, 200E, 300E, 600E | - | - | I/O, L103N_Y | I/O, L110N_Y | I/O, L110N_Y | I/O, L110N | I/O, L110N_Y |
| I/O | 7 | J1 | - | - | - | - | I/O | I/O | I/O | I/O |
| I/O, L#P | 7 | K5 | XC2S100E, 150E, 200E, 300E, 600E[1] | - | I/O, L78P_YY | I/O, L102P_YY | I/O, L109P_YY | I/O, L109P_YY | I/O, L109P | I/O, L109P_Y |
| I/O, L#N | 7 | K6 | XC2S100E, 150E, 200E, 300E, 600E[1] | - | I/O, L78N_YY | I/O, L102N_YY | I/O, L109N_YY | I/O, L109N_YY | I/O, L109N | I/O, L109N_Y |
| I/O, VREF Bank 7, L#P_Y | 7 | K3 | XC2S300E, 400E, 600E | All | I/O, VREF Bank 7, L77P | I/O, VREF Bank 7, L101P | I/O, VREF Bank 7, L108P | I/O, VREF Bank 7, L108P_Y | I/O, VREF Bank 7, L108P_Y | I/O, VREF Bank 7, L108P_Y |
| I/O, L#N_Y | 7 | K4 | XC2S300E, 400E, 600E | - | I/O, L77N | I/O, L101N | I/O, L108N | I/O, L108N_Y | I/O, L108N_Y | I/O, L108N_Y |
| I/O | 7 | K2 | - | - | - | - | - | I/O | I/O | I/O |
| I/O, L#P_Y | 7 | K1 | XC2S300E, 400E | - | - | - | I/O, L107P | I/O, L107P_Y | I/O, L107P_Y | I/O, L107P |
| I/O, L#N_Y | 7 | L1 | XC2S100E, 150E, 300E, 400E | - | I/O, L76P_Y | I/O, L100P_Y | I/O, L107N | I/O, L107N_Y | I/O, L107N_Y | I/O, L107N |
| I/O, L#P_Y | 7 | L3 | XC2S100E, 150E, 200E, 300E, 600E | XC2S400E, 600E | I/O, L76N_Y | I/O, L100N_Y | I/O, L106P_Y | I/O, L106P_Y | I/O, VREF Bank 7, L106P | I/O, VREF Bank 7, L106P_Y |
| I/O, L#N_Y | 7 | L2 | XC2S200E, 300E, 600E | - | - | I/O | I/O, L106N_Y | I/O, L106N_Y | I/O, L106N | I/O, L106N_Y |
| I/O | 7 | L4 | - | - | - | - | - | I/O | I/O | I/O |

## FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

| Pad Name | | | LVDS Async. Output Option | $V_{REF}$ Option | Device-Specific Pinouts: XC2S | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Function | Bank | Pin | | | 100E | 150E | 200E | 300E | 400E | 600E |
| I/O, L#P_YY | 7 | L5 | All | - | I/O, L75P_YY | I/O, L99P_YY | I/O, L105P_YY | I/O, L105P_YY | I/O, L105P_YY | I/O, L105P_YY |
| I/O (IRDY), L#N_YY | 7 | L6 | All | - | I/O (IRDY), L75N_YY | I/O (IRDY), L99N_YY | I/O (IRDY), L105N_YY | I/O (IRDY), L105N_YY | I/O (IRDY), L105N_YY | I/O (IRDY), L105N_YY |
| | | | | | | | | | | |
| I/O (TRDY) | 6 | M1 | - | - | I/O (TRDY) | I/O (TRDY) | I/O (TRDY) | I/O (TRDY) | I/O (TRDY) | I/O (TRDY) |
| I/O | 6 | M2 | - | - | - | - | - | I/O | I/O | I/O |
| I/O, L#P_Y | 6 | M3 | XC2S200E, 300E, 600E | - | - | I/O | I/O, L104P_Y | I/O, L104P_Y | I/O, L104P | I/O, L104P_Y |
| I/O, L#N_Y | 6 | M4 | XC2S100E, 150E, 200E, 300E, 600E | XC2S400E, 600E | I/O, L74P_Y | I/O, L98P_Y | I/O, L104N_Y | I/O, L104N_Y | I/O, VREF Bank 6, L104N | I/O, VREF Bank 6, L104N_Y |
| I/O, L#P_Y | 6 | M5 | XC2S100E, 150E, 300E, 400E | - | I/O, L74N_Y | I/O, L98N_Y | I/O, L103P | I/O, L103P_Y | I/O, L103P_Y | I/O, L103P |
| I/O, L#N_Y | 6 | M6 | XC2S300E, 400E | - | - | - | I/O, L103N | I/O, L103N_Y | I/O, L103N_Y | I/O, L103N |
| I/O | 6 | N1 | - | - | - | - | - | I/O | I/O | I/O |
| I/O | 6 | N2 | - | - | I/O, L73P | I/O, L97P | I/O | I/O | I/O | I/O |
| I/O, VREF Bank 6, L#P | 6 | N3 | XC2S200E, 400E | All | I/O, VREF Bank 6, L73N | I/O, VREF Bank 6, L97N | I/O, VREF Bank 6, L102P_Y | I/O, VREF Bank 6, L102P | I/O, VREF Bank 6, L102P_Y | I/O, VREF Bank 6, L102P |
| I/O, L#N | 6 | N4 | XC2S100E, 150E, 200E, 400E | - | I/O, L72P_Y | I/O, L96P_Y | I/O, L102N_Y | I/O, L102N | I/O, L102N_Y | I/O, L102N |
| I/O, L#P_Y | 6 | N5 | XC2S100E, 150E, 300E, 600E | - | I/O, L72N_Y | I/O, L96N_Y | I/O, L101P | I/O, L101P_Y | I/O, L101P | I/O, L101P_Y |
| I/O, L#N_Y | 6 | N6 | XC2S300E, 600E | - | - | - | I/O, L101N | I/O, L101N_Y | I/O, L101N | I/O, L101N_Y |
| I/O, L#P_Y | 6 | P1 | XC2S150E, 200E, 300E, 600E | - | - | I/O, L95P_Y | I/O, L100P_Y | I/O, L100P_Y | I/O, L100P | I/O, L100P_Y |
| I/O, L#N_Y | 6 | P2 | XC2S100E, 150E, 200E, 300E, 600E | - | I/O, L71P_Y | I/O, L95N_Y | I/O, L100N_Y | I/O, L100N_Y | I/O, L100N | I/O, L100N_Y |
| I/O | 6 | R1 | XC2S100E, 150E | - | I/O, L71N_Y | I/O, L94P_Y | I/O | I/O | I/O | I/O |
| I/O, L#P_Y | 6 | P3 | XC2S150E, 200E, 300E, 400E, 600E | - | - | I/O, L94N_Y | I/O, L99P_Y | I/O, L99P_Y | I/O, L99P_Y | I/O, L99P_Y |
| I/O, L#N_Y | 6 | P4 | XC2S200E, 300E, 400E, 600E | - | - | - | I/O, L99N_Y | I/O, L99N_Y | I/O, L99N_Y | I/O, L99N_Y |
| I/O, L#P_YY | 6 | P5 | All | - | I/O, L70P_YY | I/O, L93P_YY | I/O, L98P_YY | I/O, L98P_YY | I/O, L98P_YY | I/O, L98P_YY |
| I/O, L#N_YY | 6 | P6 | All | - | I/O, L70N_YY | I/O, L93N_YY | I/O, L98N_YY | I/O, L98N_YY | I/O, L98N_YY | I/O, L98N_YY |

## FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

| Pad Name | | | LVDS Async. Output Option | $V_{REF}$ Option | Device-Specific Pinouts: XC2S | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Function | Bank | Pin | | | 100E | 150E | 200E | 300E | 400E | 600E |
| I/O, VREF Bank 5, L#N_Y | 5 | V8 | XC2S100E, 200E, 300E, 400E, 600E | All | I/O, VREF Bank 5, L58N_Y | I/O, VREF Bank 5, L77N | I/O, VREF Bank 5, L82N_Y | I/O, VREF Bank 5, L82N_Y | I/O, VREF Bank 5, L82N_Y | I/O, VREF Bank 5, L82N_Y |
| I/O, L#P_Y | 5 | W8 | XC2S100E, 200E, 300E, 400E, 600E | - | I/O, L58P_Y | I/O, L77P | I/O, L82P_Y | I/O, L82P_Y | I/O, L82P_Y | I/O, L82P_Y |
| I/O, L#N_Y | 5 | AB9 | XC2S100E, 200E, 300E, 400E, 600E | - | I/O, L57N_Y | I/O, L76N | I/O, L81N_Y | I/O, L81N_Y | I/O, L81N_Y | I/O, L81N_Y |
| I/O, L#P_Y | 5 | AA9 | XC2S100E, 200E, 300E, 400E, 600E | - | I/O, L57P_Y | I/O, L76P | I/O, L81P_Y | I/O, L81P_Y | I/O, L81P_Y | I/O, L81P_Y |
| I/O | 5 | AB10 | - | - | - | - | I/O | I/O | I/O | I/O |
| I/O, L#N_Y | 5 | W9 | XC2S150E, 300E, 400E, 600E | - | - | I/O, L75N_Y | I/O, L80N | I/O, L80N_Y | I/O, L80N_Y | I/O, L80N_Y |
| I/O, L#P_Y | 5 | Y9 | XC2S100E, 150E, 300E, 400E, 600E | - | I/O, L56N_Y | I/O, L75P_Y | I/O, L80P | I/O, L80P_Y | I/O, L80P_Y | I/O, L80P_Y |
| I/O, L#N_Y | 5 | V9 | XC2S100E, 150E, 300E, 400E, 600E | - | I/O, L56P_Y | I/O, L74N_Y | I/O, L79N | I/O, L79N_Y | I/O, L79N_Y | I/O, L79N_Y |
| I/O, L#P_Y | 5 | U9 | XC2S150E, 300E, 400E, 600E | - | - | I/O, L74P_Y | I/O, L79P | I/O, L79P_Y | I/O, L79P_Y | I/O, L79P_Y |
| I/O | 5 | AA10 | - | - | - | - | I/O | I/O | I/O | I/O |
| I/O, L#N_Y | 5 | W10 | XC2S200E, 300E, 400E, 600E | - | I/O, L55N | I/O, L73N | I/O, L78N_Y | I/O, L78N_Y | I/O, L78N_Y | I/O, L78N_Y |
| I/O, L#P_Y | 5 | Y10 | XC2S200E, 300E, 400E, 600E | - | I/O, L55P | I/O, L73P | I/O, L78P_Y | I/O, L78P_Y | I/O, L78P_Y | I/O, L78P_Y |
| I/O, VREF Bank 5, L#N_Y | 5 | V10 | XC2S200E, 300E, 400E, 600E | All | I/O, VREF Bank 5, L54N | I/O, VREF Bank 5, L72N | I/O, VREF Bank 5, L77N_Y | I/O, VREF Bank 5, L77N_Y | I/O, VREF Bank 5, L77N_Y | I/O, VREF Bank 5, L77N_Y |
| I/O, L#P_Y | 5 | U10 | XC2S200E, 300E, 400E, 600E | - | I/O, L54P | I/O, L72P | I/O, L77P_Y | I/O, L77P_Y | I/O, L77P_Y | I/O, L77P_Y |
| I/O | 5 | U11 | - | - | - | - | - | I/O | I/O | I/O |
| I/O | 5 | V11 | - | - | - | - | I/O | I/O | I/O | I/O |
| I/O, L#N | 5 | W11 | XC2S200E, 400E | - | I/O | I/O, L71N | I/O, L76N_Y | I/O, L76N | I/O, L76N_Y | I/O, L76N |
| I/O, L#P | 5 | Y11 | XC2S200E, 400E | XC2S400E, 600E | - | I/O, L71P | I/O, L76P_Y | I/O, L76P | I/O, VREF Bank 5, L76P_Y | I/O, VREF Bank 5, L76P |
| I/O | 5 | AA11 | - | - | - | - | - | I/O | I/O | I/O |
| I/O (DLL), L#N | 5 | AB11 | - | - | I/O (DLL), L53N | I/O (DLL), L70N | I/O (DLL), L75N | I/O (DLL), L75N | I/O (DLL), L75N | I/O (DLL), L75N |
| GCK1, I | 5 | AB12 | - | - | GCK1, I | GCK1, I | GCK1, I | GCK1, I | GCK1, I | GCK1, I |

## FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

| Pad Name | | Pin | LVDS Async. Output Option | $V_{REF}$ Option | Device-Specific Pinouts: XC2S | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Function | Bank | | | | 100E | 150E | 200E | 300E | 400E | 600E |
| I/O, L#P | 2 | L17 | XC2S100E, 150E, 200E, 300E, 600E | XC2S400E, 600E | I/O, L29N_Y | I/O, L40N_Y | I/O, L43P_Y | I/O, L43P_Y | I/O, VREF Bank 2, L43P | I/O, VREF Bank 2, L43P_Y |
| I/O, L#N | 2 | K22 | XC2S100E, 150E, 300E, 400E | - | I/O, L29P_Y | I/O, L40P_Y | I/O, L42N | I/O, L42N_Y | I/O, L42N_Y | I/O, L42N |
| I/O, L#P | 2 | K21 | XC2S300E, 400E | - | - | - | I/O, L42P | I/O, L42P_Y | I/O, L42P_Y | I/O, L42P |
| I/O | 2 | K20 | - | - | - | - | - | I/O | I/O | I/O |
| I/O (D3) | 2 | K19 | - | - | I/O (D3) | I/O (D3), L39N | I/O (D3) | I/O (D3) | I/O (D3) | I/O (D3) |
| I/O, VREF Bank 2, L#N | 2 | K18 | XC2S100E, 200E, 400E | All | I/O, VREF Bank 2, L28N_Y | I/O, VREF Bank 2, L39P | I/O, VREF Bank 2, L41N_Y | I/O, VREF Bank 2, L41N | I/O, VREF Bank 2, L41N_Y | I/O, VREF Bank 2, L41N |
| I/O, L#P | 2 | K17 | XC2S100, 150E, 200E, 400E | - | I/O, L28P_Y | I/O, L38N_Y | I/O, L41P_Y | I/O, L41P | I/O, L41P_Y | I/O, L41P |
| I/O, L#N | 2 | J22 | XC2S150E, 300E, 600E | - | I/O | I/O, L38P_Y | I/O, L40N | I/O, L40N_Y | I/O, L40N | I/O, L40N_Y |
| I/O, L#P | 2 | J21 | XC2S300E, 600E | - | - | - | I/O, L40P | I/O, L40P_Y | I/O, L40P | I/O, L40P_Y |
| I/O, L#N | 2 | J20 | XC2S150E, 200E, 300E, 600E | - | - | I/O, L37N_Y | I/O, L39N_Y | I/O, L39N_Y | I/O, L39N | I/O, L39N_Y |
| I/O, L#P | 2 | J19 | XC2S100E, 150E, 200E, 300E, 600E | - | I/O, L27N_Y | I/O, L37P_Y | I/O, L39P_Y | I/O, L39P_Y | I/O, L39P | I/O, L39P_Y |
| I/O | 2 | H22 | XC2S100E, 150E | - | I/O, L27P_Y | I/O, L36N_Y | I/O | I/O | I/O | I/O |
| I/O, L#N | 2 | J18 | XC2S150E, 200E, 300E, 400E, 600E | - | - | I/O, L36P_Y | I/O, L38N_Y | I/O, L38N_Y | I/O, L38N_Y | I/O, L38N_Y |
| I/O, L#P | 2 | J17 | XC2S200E, 300E, 400E, 600E | - | - | - | I/O, L38P_Y | I/O, L38P_Y | I/O, L38P_Y | I/O, L38P_Y |
| I/O, L#N | 2 | H21 | XC2S150E, 200E, 300E, 400E, 600E | - | I/O | I/O, L35N_Y | I/O, L37N_Y | I/O, L37N_Y | I/O, L37N_Y | I/O, L37N_Y |
| I/O (D2), L#P | 2 | H20 | XC2S150E, 200E, 300E, 400E, 600E | - | I/O (D2) | I/O (D2), L35P_Y | I/O (D2), L37P_Y | I/O (D2), L37P_Y | I/O (D2), L37P_Y | I/O (D2), L37P_Y |
| I/O (D1), L#N | 2 | H19 | XC2S300E, 400E, 600E | - | I/O (D1), L26N | I/O (D1), L34N | I/O (D1), L36N | I/O (D1), L36N_Y | I/O (D1), L36N_Y | I/O (D1), L36N_Y |
| I/O, VREF Bank 2, L#P | 2 | H18 | XC2S300E, 400E, 600E | All | I/O, VREF Bank 2, L26P | I/O, VREF Bank 2, L34P | I/O, VREF Bank 2, L36P | I/O, VREF Bank 2, L36P_Y | I/O, VREF Bank 2, L36P_Y | I/O, VREF Bank 2, L36P_Y |
| I/O | 2 | G22 | - | - | - | - | - | I/O | I/O | I/O |
| I/O | 2 | F22 | - | - | I/O | I/O | I/O | I/O | I/O | I/O |

## FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

| Pad Name | | | LVDS Async. Output Option | $V_{REF}$ Option | Device-Specific Pinouts: XC2S | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Function | Bank | Pin | | | 100E | 150E | 200E | 300E | 400E | 600E |
| I/O, L#P_YY | 0 | A6 | All | - | I/O, L2P_YY | I/O, L3P_YY | I/O, L3P_YY | I/O, L3P_YY | I/O, L3P_YY | I/O, L3P_YY |
| I/O, VREF Bank 0, L#N_YY | 0 | B6 | All | All | I/O, VREF Bank 0, L2N_YY | I/O, VREF Bank 0, L3N_YY | I/O, VREF Bank 0, L3N_YY | I/O, VREF Bank 0, L3N_YY | I/O, VREF Bank 0, L3N_YY | I/O, VREF Bank 0, L3N_YY |
| I/O | 0 | C6 | XC2S100E | - | I/O, L1P_Y | I/O | I/O | I/O | I/O | I/O |
| I/O, L#P | 0 | A5 | XC2S100E | - | I/O, L1N_Y | I/O, L2P | I/O, L2P | I/O, L2P | I/O, L2P | I/O, L2P |
| I/O, L#N | 0 | B5 | - | - | - | I/O, L2N | I/O, L2N | I/O, L2N | I/O, L2N | I/O, L2N |
| I/O | 0 | D6 | - | - | - | - | - | I/O | I/O | I/O |
| I/O, L#P | 0 | B4 | XC2S100E, 200E, 300E, 400E, 600E | - | I/O, L0P_Y | I/O, L1P | I/O, L1P_Y | I/O, L1P_Y | I/O, L1P_Y | I/O, L1P_Y |
| I/O, L#N | 0 | C5 | XC2S100E, 200E, 300E, 400E, 600E | XC2S200E, 300E, 400E, 600E | I/O, L0N_Y | I/O, L1N | I/O, VREF Bank 0, L1N_Y | I/O, VREF Bank 0, L1N_Y | I/O, VREF Bank 0, L1N_Y | I/O, VREF Bank 0, L1N_Y |
| I/O | 0 | A4 | - | - | I/O | I/O | I/O | I/O | I/O | I/O |
| I/O, L#P | 0 | A3 | XC2S150E, 400E, 600E | - | - | I/O, L0P_Y | I/O, L0P | I/O, L0P | I/O, L0P_Y | I/O, L0P_Y |
| I/O, L#N | 0 | B3 | XC2S150E, 400E, 600E | - | - | I/O, L0N_Y | I/O, L0N | I/O, L0N | I/O, L0N_Y | I/O, L0N_Y |
| I/O | 0 | C4 | - | - | - | - | - | I/O | I/O | I/O |
| I/O | 0 | D5 | - | - | I/O | I/O | I/O | I/O | I/O | I/O |
| TCK | - | E6 | - | - | TCK | TCK | TCK | TCK | TCK | TCK |

**Notes:**
1. Although designated with the _YY suffix in the XC2S100E, XC2S150E, XC2S200E, and XC2S300E, these differential pairs are not asynchronous in the XC2S400E.

## FG456 Differential Clock Pins

| Clock | Bank | P | | N | |
|---|---|---|---|---|---|
| | | Pin | Name | Pin | Name |
| GCK0 | 4 | AA12 | GCK0, I | Y12 | I/O (DLL), L#P |
| GCK1 | 5 | AB12 | GCK1, I | AB11 | I/O (DLL), L#N |
| GCK2 | 1 | A11 | GCK2, I | A12 | I/O (DLL), L#P |
| GCK3 | 0 | C11 | GCK3, I | B11 | I/O (DLL), L#N |

## Additional FG456 Package Pins

| **VCCINT Pins** | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| D4(1) | D19(1) | E5 | E18 | F6 | F17 | G7 | G8 | G15 |
| G16 | H7 | H16 | R7 | R16 | T7 | T8 | T15 | T16 |
| U6 | U17 | V5 | V18 | W4(1) | W19(1) | - | - | - |
| **VCCO Bank 0 Pins** | | | | | | | | |
| F7 | F8 | G9 | G10 | - | - | - | - | - |

## Additional FG456 Package Pins *(Continued)*

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **VCCO Bank 1 Pins** | | | | | | | | |
| F15 | F16 | G13 | G14 | - | - | - | - | - |
| **VCCO Bank 2 Pins** | | | | | | | | |
| G17 | H17 | J16 | K16 | - | - | - | - | - |
| **VCCO Bank 3 Pins** | | | | | | | | |
| N16 | P16 | R17 | T17 | - | - | - | - | - |
| **VCCO Bank 4 Pins** | | | | | | | | |
| T13 | T14 | U15 | U16 | - | - | - | - | - |
| **VCCO Bank 5 Pins** | | | | | | | | |
| T9 | T10 | U7 | U8 | - | - | - | - | - |
| **VCCO Bank 6 Pins** | | | | | | | | |
| N7 | P7 | R6 | T6 | - | - | - | - | - |
| **VCCO Bank 7 Pins** | | | | | | | | |
| G6 | H6 | J7 | K7 | - | - | - | - | - |
| **GND Pins** | | | | | | | | |
| A1 | A2(2) | A22 | B1(2) | B2 | B21 | C3 | C20 | G11 |
| G12 | J9 | J10 | J11 | J12 | J13 | J14 | K9 | K10 |
| K11 | K12 | K13 | K14 | L7 | L9 | L10 | L11 | L12 |
| L13 | L14 | L16 | M7 | M9 | M10 | M11 | M12 | M13 |
| M14 | M16 | N9 | N10 | N11 | N12 | N13 | N14 | P9 |
| P10 | P11 | P12 | P13 | P14 | T11 | T12 | Y20 | Y3 |
| Y4(2) | AA2 | AA4(2) | AA21 | AA22(2) | AB1 | AB22 | - | - |
| **Not Connected Pins** | | | | | | | | |
| A2(2) | B1(2) | D4(1) | D19(1) | W4(1) | W19(1) | Y4(2) | AA4(2) | AA22(2) |

**Notes:**
1. VCCINT connections in XC2S400E and XC2S600E. No Connects (no internal connection) in XC2S100E, XC2S150E, XC2S200E, and XC2S300E.
2. GND connections in XC2S400E and XC2S600E. No Connects (no internal connection) in XC2S100E, XC2S150E, XC2S200E, and XC2S300E

## FG676 Pinouts (XC2S400E, XC2S600E)

| Pad Name | | Pin | LVDS Async. Output Option | VREF Option | Device-Specific Pinouts | |
|---|---|---|---|---|---|---|
| Function | Bank | | | | XC2S400E | XC2S600E |
| TMS | - | B1 | - | - | TMS | TMS |
| I/O | 7 | D3 | - | - | I/O | I/O |
| I/O, L204P | 7 | C2 | - | - | - | I/O, L204P |
| I/O, L204N | 7 | C1 | - | - | - | I/O, L204N |
| I/O, L203P | 7 | D2 | XC2S600E | - | - | I/O, L203P_Y |
| I/O, L203N | 7 | D1 | XC2S600E | - | I/O | I/O, L203N_Y |
| I/O, L202P_YY | 7 | E2 | All | - | I/O, L202P_YY | I/O, L202P_YY |
| I/O, L202N_YY | 7 | E1 | All | - | I/O, L202N_YY | I/O, L202N_YY |

## FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

| Pad Name | | Pin | LVDS Async. Output Option | VREF Option | Device-Specific Pinouts | |
|---|---|---|---|---|---|---|
| Function | Bank | | | | XC2S400E | XC2S600E |
| | | | | | | |
| I/O | 5 | AC5 | - | - | I/O | I/O |
| I/O, L152N | 5 | AE4 | - | - | I/O | I/O, L152N |
| I/O, L152P | 5 | AF4 | - | - | - | I/O, L152P |
| I/O, L151N | 5 | AE5 | - | - | - | I/O, L151N |
| I/O, L151P | 5 | AF5 | - | - | I/O | I/O, L151P |
| I/O, L150N | 5 | AA6 | XC2S400E | - | I/O, L150N_Y | I/O, L150N |
| I/O, L150P | 5 | AB6 | XC2S400E | - | I/O, L150P_Y | I/O, L150P |
| I/O, L149N_YY | 5 | AC6 | All | - | I/O, L149N_YY | I/O, L149N_YY |
| I/O, L149P_YY | 5 | AD6 | All | - | I/O, L149P_YY | I/O, L149P_YY |
| I/O, VREF Bank 5, L148N_YY | 5 | AE6 | All | All | I/O, VREF Bank 5, L148N_YY | I/O, VREF Bank 5, L148N_YY |
| I/O, L148P_YY | 5 | AF6 | All | - | I/O, L148P_YY | I/O, L148P_YY |
| I/O, L147N | 5 | AA7 | XC2S600E | - | - | I/O, L147N_Y |
| I/O, L147P | 5 | AB7 | XC2S600E | - | I/O | I/O, L147P_Y |
| I/O, L146N_YY | 5 | AC7 | All | - | I/O, L146N_YY | I/O, L146N_YY |
| I/O, L146P_YY | 5 | AD7 | All | - | I/O, L146P_YY | I/O, L146P_YY |
| I/O, L145N_YY | 5 | AE7 | All | - | I/O, L145N_YY | I/O, L145N_YY |
| I/O, L145P_YY | 5 | AF7 | All | - | I/O, L145P_YY | I/O, L145P_YY |
| I/O, VREF Bank 5, L144N_YY | 5 | Y8 | All | All | I/O, VREF Bank 5, L144N_YY | I/O, VREF Bank 5, L144N_YY |
| I/O, L144P_YY | 5 | AA8 | All | - | I/O, L144P_YY | I/O, L144P_YY |
| I/O, L143N_YY | 5 | AE8 | All | - | I/O, L143N_YY | I/O, L143N_YY |
| I/O, L143P_YY | 5 | AF8 | All | - | I/O, L143P_YY | I/O, L143P_YY |
| I/O | 5 | AB8 | - | - | I/O | I/O |
| I/O, L142N | 5 | W9 | XC2S600E | - | I/O, L142N | I/O, L142N_Y |
| I/O, L142P | 5 | Y9 | XC2S600E | - | I/O, L142P | I/O, L142P_Y |
| I/O, L141N | 5 | AA9 | XC2S600E | XC2S600E | - | I/O, VREF Bank 5, L141N_Y |
| I/O, L141P | 5 | AB9 | XC2S600E | - | I/O | I/O, L141P_Y |
| I/O, L140N_YY | 5 | AC9 | All | - | I/O, L140N_YY | I/O, L140N_YY |
| I/O, L140P_YY | 5 | AD9 | All | - | I/O, L140P_YY | I/O, L140P_YY |
| I/O, L139N_YY | 5 | AE9 | All | - | I/O, L139N_YY | I/O, L139N_YY |
| I/O, L139P_YY | 5 | AF9 | All | - | I/O, L139P_YY | I/O, L139P_YY |
| I/O, VREF Bank 5, L138N_YY | 5 | W10 | All | All | I/O, VREF Bank 5, L138N_YY | I/O, VREF Bank 5, L138N_YY |

## FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

| Pad Name | | Pin | LVDS Async. Output Option | VREF Option | Device-Specific Pinouts | |
|---|---|---|---|---|---|---|
| Function | Bank | | | | XC2S400E | XC2S600E |
| I/O | 4 | AC18 | - | - | I/O | I/O |
| I/O, VREF Bank 4, L114N | 4 | AB18 | - | All | I/O, VREF Bank 4, L114N | I/O, VREF Bank 4, L114N |
| I/O, L114P | 4 | AA18 | - | - | I/O, L114P | I/O, L114P |
| I/O, L113N | 4 | Y18 | - | - | I/O, L113N | I/O, L113N |
| I/O, L113P | 4 | W18 | - | - | I/O, L113P | I/O, L113P |
| I/O | 4 | AB19 | - | - | I/O | I/O |
| I/O, L112N | 4 | AF19 | XC2S600E | - | I/O | I/O, L112N_Y |
| I/O, L112P | 4 | AE19 | XC2S600E | XC2S600E | - | I/O, VREF Bank 4, L112P_Y |
| I/O, L111N | 4 | AA19 | XC2S600E | - | I/O, L111N | I/O, L111N_Y |
| I/O, L111P | 4 | Y19 | XC2S600E | - | I/O, L111P | I/O, L111P_Y |
| I/O | 4 | AF20 | - | - | - | I/O |
| I/O, L110N | 4 | AE20 | XC2S600E | - | I/O, L110N | I/O, L110N_Y |
| I/O, L110P | 4 | AD20 | XC2S600E | - | I/O, L110P | I/O, L110P_Y |
| I/O | 4 | AC20 | - | - | I/O | I/O |
| I/O, L109N_YY | 4 | AB20 | All | - | I/O, L109N_YY | I/O, L109N_YY |
| I/O, VREF Bank 4, L109P_YY | 4 | AA20 | All | All | I/O, VREF Bank 4, L109P_YY | I/O, VREF Bank 4, L109P_YY |
| I/O | 4 | Y20 | - | - | I/O | I/O |
| I/O, L108N | 4 | AF21 | - | - | I/O, L108N | I/O, L108N |
| I/O, L108P | 4 | AE21 | - | - | I/O, L108P | I/O, L108P |
| I/O, L107N | 4 | AD21 | - | - | I/O, L107N | I/O, L107N |
| I/O, L107P | 4 | AC21 | - | - | I/O, L107P | I/O, L107P |
| I/O | 4 | AC22 | - | - | - | I/O |
| I/O, L106N_YY | 4 | AF22 | All | - | I/O, L106N_YY | I/O, L106N_YY |
| I/O, VREF Bank 4, L106P_YY | 4 | AE22 | All | All | I/O, VREF Bank 4, L106P_YY | I/O, VREF Bank 4, L106P_YY |
| I/O, L105N_YY | 4 | AB21 | All | - | I/O, L105N_YY | I/O, L105N_YY |
| I/O, L105P_YY | 4 | AA21 | All | - | I/O, L105P_YY | I/O, L105P_YY |
| I/O, L104N_YY | 4 | AF23 | All | - | I/O, L104N_YY | I/O, L104N_YY |
| I/O, L104P_YY | 4 | AE23 | All | - | I/O, L104P_YY | I/O, L104P_YY |
| I/O, L103N | 4 | AD23 | XC2S600E | - | I/O | I/O, L103N_Y |
| I/O, L103P | 4 | AE24 | XC2S600E | - | - | I/O, L103P_Y |
| I/O, L102N_YY | 4 | AF24 | All | - | I/O, L102N_YY | I/O, L102N_YY |
| I/O, L102P_YY | 4 | AF25 | All | - | I/O, L102P_YY | I/O, L102P_YY |

## Additional FG676 Package Pins *(Continued)*

| | | | | | | |
|---|---|---|---|---|---|---|
| **GND Pins** | | | | | | |
| A1 | A26 | B2 | B25 | C3 | C12 | C15 |
| C24 | D4 | D8 | D19 | D23 | F10 | F17 |
| H4 | H23 | K6 | K21 | L11 | L12 | L13 |
| L14 | L15 | L16 | M3 | M11 | M12 | M13 |
| M14 | M15 | M16 | M24 | N11 | N12 | N13 |
| N14 | N15 | N16 | P11 | P12 | P13 | P14 |
| P15 | P16 | R3 | R11 | R12 | R13 | R14 |
| R15 | R16 | R24 | T11 | T12 | T13 | T14 |
| T15 | T16 | U6 | U21 | W4 | W23 | AA10 |
| AA17 | AC4 | AC8 | AC19 | AC23 | AD3 | AD12 |
| AD15 | AD24 | AE2 | AE25 | AF1 | AF26 | - |
| **Not Connected Pins (XC2S400E Only)** | | | | | | |
| A12 | A16 | A23 | B3 | C1 | C2 | C10 |
| C11 | C25 | D2 | D15 | D18 | D24 | D25 |
| E7 | E13 | E19 | F2 | F6 | F8 | F12 |
| F20 | F22 | G10 | G14 | G15 | G16 | G26 |
| H10 | H13 | H16 | H25 | J6 | J8 | J12 |
| J13 | K1 | K4 | K22 | K24 | L3 | L19 |
| L22 | L26 | M4 | M9 | M22 | N1 | N4 |
| N9 | N18 | N19 | N23 | P4 | P5 | P18 |
| P19 | P24 | R4 | R7 | R19 | T3 | T24 |
| U1 | U4 | U7 | U24 | U25 | V8 | V12 |
| V13 | V21 | W12 | W13 | W14 | W16 | Y3 |
| Y7 | Y21 | AA7 | AA9 | AA22 | AB15 | AB16 |
| AB17 | AB22 | AC1 | AC15 | AC22 | AC25 | AC26 |
| AD1 | AD2 | AD10 | AD11 | AD13 | AD14 | AE5 |
| AE19 | AE24 | AF4 | AF16 | AF18 | AF20 | - |