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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

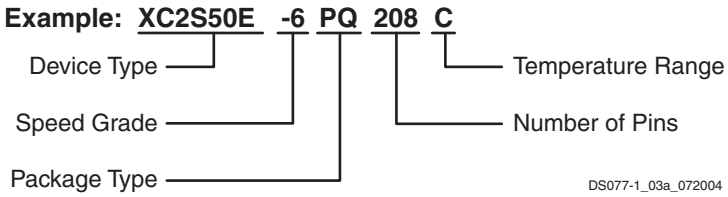
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	384
Number of Logic Elements/Cells	1728
Total RAM Bits	32768
Number of I/O	102
Number of Gates	50000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s50e-6tq144c

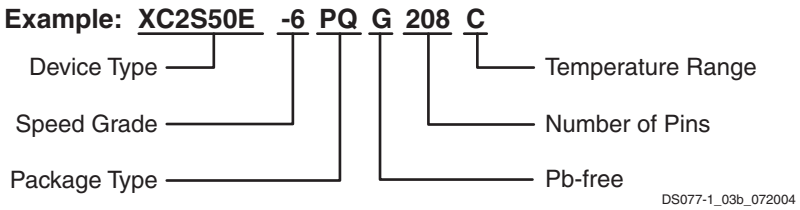
Ordering Information

Spartan-IIE devices are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a special "G" character in the ordering code.

Standard Packaging



Pb-Free Packaging



Device Ordering Options

Device
XC2S50E
XC2S100E
XC2S150E
XC2S200E
XC2S300E
XC2S400E
XC2S600E

Speed Grade	
-6	Standard Performance
-7	Higher Performance(1)

Package Type / Number of Pins	
TQ(G)144	144-pin Plastic Thin QFP
PQ(G)208	208-pin Plastic QFP
FT(G)256	256-ball Fine Pitch BGA
FG(G)456	456-ball Fine Pitch BGA
FG(G)676	676-ball Fine Pitch BGA

Temperature Range (T_J)(2)	
C = Commercial	0°C to +85°C
I = Industrial	40°C to +100°C

Notes:
1. The -7 speed grade is exclusively available in the Commercial temperature range.
2. See www.xilinx.com for information on automotive temperature range devices.

Device Part Marking

Figure 2 is a top marking example for Spartan-IIE FPGAs in the quad-flat packages. The markings for BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator.

The "7C" and "6I" Speed Grade/Temperature Range part combinations may be dual marked as "7C/6I". Devices with the dual mark can be used as either -7C or -6I devices. Devices with a single mark are only guaranteed for the marked speed grade and temperature range.

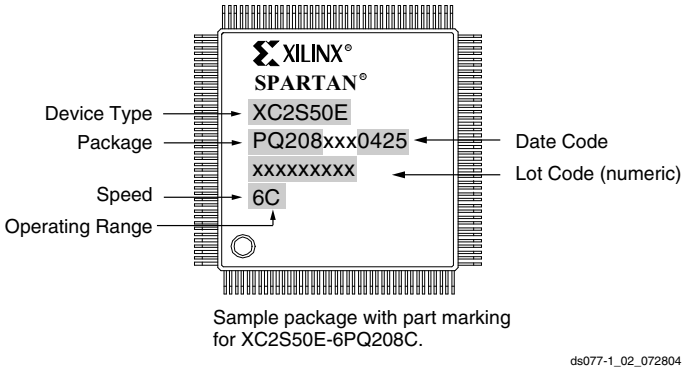


Figure 2: Spartan-IIE QFP Marking Example

Revision History

Date	Version	Description
06/27/2002	1.1	Updated -7 availability.
11/18/2002	2.0	Added XC2S400E and XC2S600E. Corrected XC2S150E max I/O count and XC2S50E differential I/O count and updated availability.
07/09/2003	2.1	Noted hot-swap capability. Updated Table 2 to show that all products are available. Clarified device part marking.
07/28/2004	2.2	Added information on Pb-free packaging options.
06/18/2008	2.3	Added dual mark information in Device Part Marking. Updated all modules for continuous page, figure, and table numbering. Updated links. Synchronized all modules to v2.3.
08/09/2013	3.0	This product is obsolete/discontinued per XCN12026.

Configurable Logic Block

The basic building block of the Spartan-IIE FPGA CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and storage element. The output from the function generator in each LC drives the CLB output or the D input of the flip-flop. Each Spartan-IIE FPGA CLB contains four LCs, organized in two similar slices; a single slice is shown in Figure 6.

In addition to the four basic LCs, the Spartan-IIE FPGA CLB contains logic that combines function generators to provide functions of five or six inputs.

Look-Up Tables

Spartan-IIE FPGA function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16 x 1-bit dual-port synchronous RAM.

The Spartan-IIE FPGA LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

Storage Elements

Storage elements in the Spartan-IIE FPGA slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals may be configured to operate asynchronously.

All control signals are independently invertible, and are shared by the two flip-flops within the slice.

Dedicated Routing

Some classes of signal require dedicated routing resources to maximize performance. In the Spartan-IIE FPGA architecture, dedicated routing resources are provided for two classes of signal.

Horizontal routing resources are provided for on-chip 3-state busses. Four partitionable bus lines are provided per CLB row, permitting multiple busses within a row, as shown in Figure 10.

Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.

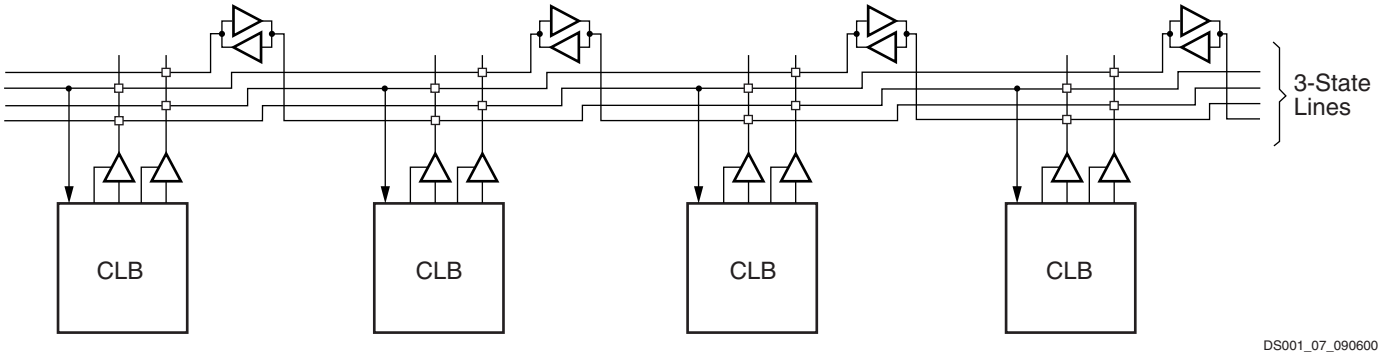


Figure 10: BUFT Connections to Dedicated Horizontal Bus Lines

Global Routing

Global Routing resources distribute clocks and other signals with very high fanout throughout the device. Spartan-IIE devices include two tiers of global routing resources referred to as primary and secondary global routing resources.

The primary global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The primary global nets may only be driven by global buffers. There are four global buffers, one for each global net.

The secondary global routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across the bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These secondary resources are more flexible than the primary resources since they are not restricted to routing only to clock pins.

Clock Distribution

The Spartan-IIE family provides high-speed, low-skew clock distribution through the primary global routing resources described above. A typical clock distribution net is shown in Figure 11.

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four primary global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing.

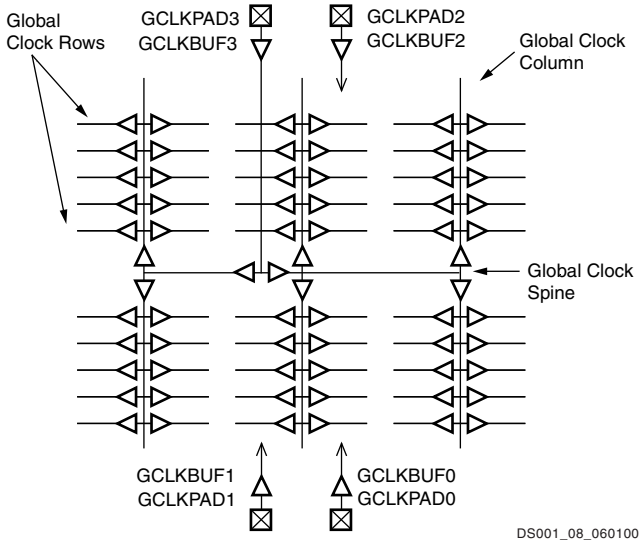


Figure 11: Global Clock Distribution Network

Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element (Figure 12). Additional delay is introduced such that clock edges reach internal flip-flops exactly one clock period after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock

Table 8: Boundary-Scan Instructions (Continued)

Boundary-Scan Command	Binary Code[4:0]	Description
INTEST	00111	Enables boundary-scan INTEST operation
USERCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIGHZ	01010	Disables output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions

The public boundary-scan instructions are available prior to configuration, except for USER1 and USER2. After configuration, the public instructions remain available together with any USERCODE instructions installed during the configuration. While the SAMPLE/PRELOAD and BYPASS instructions are available during configuration, it is recommended that boundary-scan operations not be performed during this transitional period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

To facilitate internal scan chains, the User Register provides three outputs (Reset, Update, and Shift) that represent the corresponding states in the boundary-scan internal state machine.

Figure 14 is a diagram of the Spartan-IIE family boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

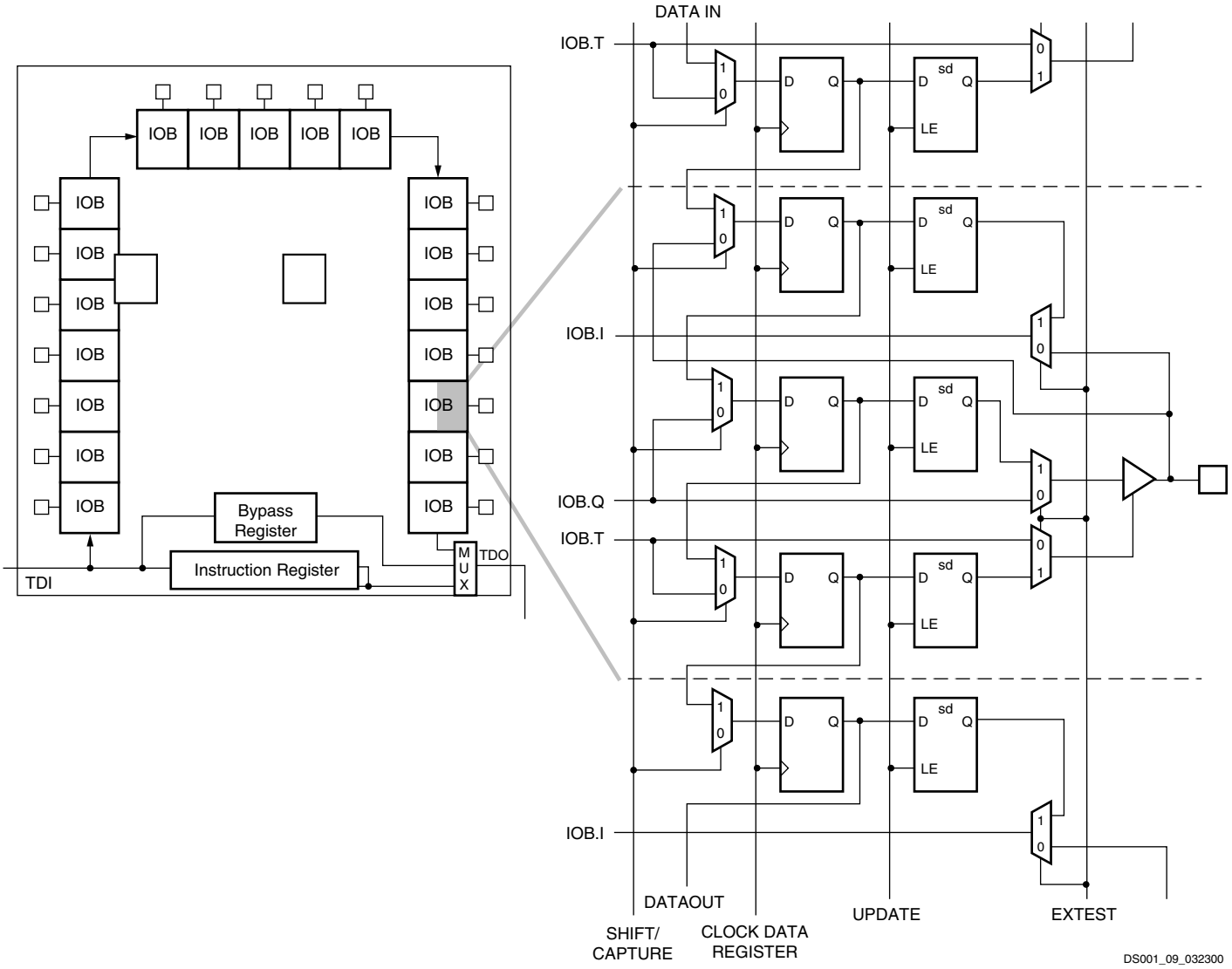


Figure 14: Spartan-IIE Family Boundary Scan Logic

During start-up, the device performs four operations:

1. The assertion of DONE. The failure of DONE to go High may indicate the unsuccessful loading of configuration data.
2. The release of the Global Three State (GTS). This activates all the I/Os to which signals are assigned. The remaining I/Os stay in a high-impedance state with internal weak pull-up resistors present.
3. The release of the Global Set Reset (GSR). This allows all flip-flops to change state.
4. The assertion of Global Write Enable (GWE). This allows all RAMs and flip-flops to change state.

By default, these operations are synchronized to CCLK. The entire start-up sequence lasts eight cycles, called C0-C7, after which the loaded design is fully functional. The four operations can be selected to switch on any CCLK cycle C1-C6 through settings in the Xilinx Development Software. The default timing for start-up is shown in the top half of Figure 17; heavy lines show default settings.

The default Start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The bottom half of Figure 17 shows another commonly used version of the start-up timing known as Sync-to-DONE. This version makes the GTS, GSR, and GWE events conditional upon the DONE pin going High. This timing is important for a daisy chain of multiple FPGAs in serial mode, since it ensures that all FPGAs go through start-up together, after all their DONE pins have gone High.

Sync-to-DONE timing is selected by setting the GTS, GSR, and GWE cycles to a value of DONE in the configuration options. This causes these signals to transition one clock cycle after DONE externally transitions High.

The sequence can also be paused at any stage until lock has been achieved on any or all DLLs.

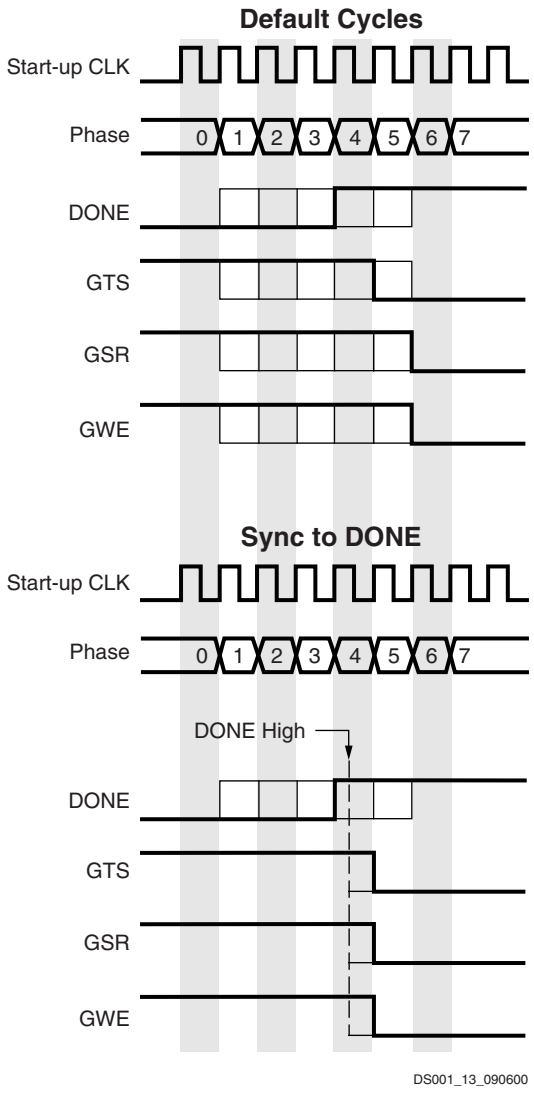


Figure 17: Start-Up Waveforms

Serial Modes

There are two serial configuration modes. In Master Serial mode, the FPGA controls the configuration process by driving CCLK as an output. In Slave Serial mode, the FPGA passively receives CCLK as an input from an external agent (e.g., a microprocessor, CPLD, or second FPGA in master mode) that is controlling the configuration process. In both modes, the FPGA is configured by loading one bit per CCLK cycle. The MSB of each configuration data byte is always written to the DIN pin first.

See Figure 18 for the sequence for loading data into the Spartan-IIE FPGA serially. This is an expansion of the "Load Configuration Data Frames" block in Figure 16, page 23. Note that $\overline{CS}$ and $\overline{WRITE}$ are not normally used during serial configuration. To ensure successful loading of the FPGA, do not toggle $\overline{WRITE}$ with $\overline{CS}$ Low during serial configuration.

If CCLK is slower than F_{CCNH}, the FPGA will never assert BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

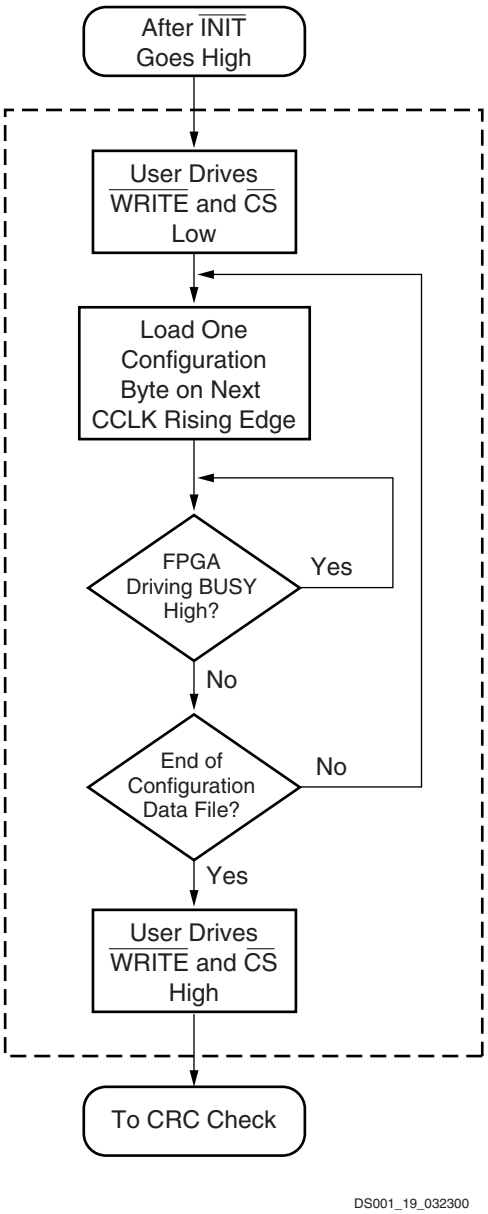


Figure 21: Loading Configuration Data for the Slave Parallel Mode

A configuration packet does not have to be written in one continuous stretch, rather it can be split into many write sequences. Each sequence would involve assertion of $\overline{CS}$.

In applications where multiple clock cycles may be required to access the configuration data before each byte can be loaded into the Slave Parallel interface, a new byte of data may not be ready for each consecutive CCLK edge. In such a case the $\overline{CS}$ signal may be deasserted until the next byte is valid on D0-D7. While $\overline{CS}$ is High, the Slave Parallel interface does not expect any data and ignores all CCLK transitions. However, to avoid aborting configuration, $\overline{WRITE}$ must continue to be asserted while $\overline{CS}$ is asserted during CCLK transitions.

Abort

To abort configuration during a write sequence, deassert $\overline{WRITE}$ while holding $\overline{CS}$ Low. The abort operation is initiated at the rising edge of CCLK. The device will remain BUSY until the aborted operation is complete. After aborting configuration, data is assumed to be unaligned to word boundaries and the FPGA requires a new synchronization word prior to accepting any new packets.

Boundary-Scan Configuration Mode

In the boundary-scan mode, no nondedicated pins are required, configuration being done entirely through the IEEE 1149.1 Test Access Port (TAP).

Configuration through the TAP uses the special CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port.

1. Load the CFG_IN instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a standard configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the JSTART instruction into IR
6. Enter the SDR state
7. Clock TCK (if selected) through the startup sequence (the length is programmable)
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode simply locks out the other modes. The boundary-scan mode is selected by a <10x> on the mode pins (M0, M1, M2). Note that the $\overline{PROGRAM}$ pin must be pulled High prior to reconfiguration. A Low on the $\overline{PROGRAM}$ pin resets the TAP controller and no boundary scan operations can be performed. See Xilinx Application Note XAPP188 for more information on boundary-scan configuration.

Readback

The configuration data stored in the Spartan-IIE FPGA configuration memory can be read back for verification. Along with the configuration data it is possible to read back the contents of all flip-flops/latches, LUT RAMs, and block RAMs. This capability is used for real-time debugging.

For more detailed information see Xilinx Application Note XAPP176, Configuration and Readback of the Spartan-II and Spartan-IIE FPGA Families.

DLL Timing Parameters

Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Symbol	Description	F_{CLKIN}	Speed Grade				Units
			-7		-6		
			Min	Max	Min	Max	
$F_{CLKINHF}$	Input clock frequency (CLKDLLHF)	-	60	320	60	275	MHz
$F_{CLKINLF}$	Input clock frequency (CLKDLL)	-	25	160	25	135	MHz
T_{DLLPW}	Input clock pulse width	25 MHz	5.0	-	5.0	-	ns
		50 MHz	3.0	-	3.0	-	ns
		100 MHz	2.4	-	2.4	-	ns
		150 MHz	2.0	-	2.0	-	ns
		200 MHz	1.8	-	1.8	-	ns
		250 MHz	1.5	-	1.5	-	ns
		300 MHz	1.3	-	NA	-	

DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications were determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers. Figure 22, page 44, provides definitions for various parameters in the table below.

Symbol	Description	F_{CLKIN}	CLKDLLHF		CLKDLL		Units
			Min	Max	Min	Max	
T_{IPTOL}	Input clock period tolerance		-	1.0	-	1.0	ns
T_{IJITCC}	Input clock jitter tolerance (cycle-to-cycle)		-	–150	-	–300	ps
T_{LOCK}	Time required for DLL to acquire lock(1)	> 60 MHz	-	20	-	20	µs
		50-60 MHz	-	-	-	25	µs
		40-50 MHz	-	-	-	50	µs
		30-40 MHz	-	-	-	90	µs
		25-30 MHz	-	-	-	120	µs
T_{OJITCC}	Output jitter (cycle-to-cycle) for any DLL clock output(2)		-	–60	-	–60	ps
T_{PHIO}	Phase offset between CLKIN and CLKO(3)		-	–100	-	–100	ps
T_{PHOO}	Phase offset between clock outputs on the DLL(4)		-	–140	-	–140	ps
T_{PHIOM}	Phase difference between CLKIN and CLKO(5)		-	–160	-	–160	ps
T_{PHOOM}	Phase difference between clock outputs on the DLL(6)		-	–200	-	–200	ps

Notes:
1. Commercial operating conditions. Add 30% for Industrial operating conditions.
2. Output Jitter is cycle-to-cycle jitter measured on the DLL output clock, excluding input clock jitter.
3. Phase Offset between CLKIN and CLKO is the worst-case fixed time difference between rising edges of CLKIN and CLKO, excluding output jitter and input clock jitter.
4. Phase Offset between Clock Outputs on the DLL is the worst-case fixed time difference between rising edges of any two DLL outputs, excluding output jitter and input clock jitter.
5. Maximum Phase Difference between CLKIN and CLKO is the sum of output jitter and phase offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (excluding input clock jitter).
6. Maximum Phase Difference between Clock Outputs on the DLL is the sum of output jitter and phase offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (excluding input clock jitter).