AMD Xilinx - XC2S50E-6TQG144C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	384
Number of Logic Elements/Cells	1728
Total RAM Bits	32768
Number of I/O	102
Number of Gates	50000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s50e-6tqg144c

Spartan-IIE FPGA Family: Introduction and Ordering Information

DS077-1 (v3.0) August 9, 2013

Product Specification

Introduction

The Spartan®-IIE Field-Programmable Gate Array family gives users high performance, abundant logic resources, and a rich feature set, all at an exceptionally low price. The seven-member family offers densities ranging from 50,000 to 600,000 system gates, as shown in Table 1. System performance is supported beyond 200 MHz.

Features include block RAM (to 288K bits), distributed RAM (to 221,184 bits), 19 selectable I/O standards, and four DLLs (Delay-Locked Loops). Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

The Spartan-IIE family is a superior alternative to mask-programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary (impossible with ASICs).

Features

- Second generation ASIC replacement technology
    - Densities as high as 15,552 logic cells with up to 600,000 system gates
    - Streamlined features based on Virtex®-E FPGA architecture
    - Unlimited in-system reprogrammability
    - Very low cost
    - Cost-effective 0.15 micron technology
- System level features
    - SelectRAM™ hierarchical memory:
        - 16 bits/LUT distributed RAM
        - Configurable 4K-bit true dual-port block RAM
        - Fast interfaces to external RAM
    - Fully 3.3V PCI compliant to 64 bits at 66 MHz and CardBus compliant
    - Low-power segmented routing architecture
    - Dedicated carry logic for high-speed arithmetic
    - Efficient multiplier support
    - Cascade chain for wide-input functions
    - Abundant registers/latches with enable, set, reset
    - Four dedicated DLLs for advanced clock control
        - Eliminate clock distribution delay
        - Multiply, divide, or phase shift
    - Four primary low-skew global clock distribution nets
    - IEEE 1149.1 compatible boundary scan logic
- Versatile I/O and packaging
    - Pb-free package options
    - Low-cost packages available in all densities
    - Family footprint compatibility in common packages
    - 19 high-performance interface standards
        - LVTTL, LVCMOS, HSTL, SSTL, AGP, CTT, GTL
        - LVDS and LVPECL differential I/O
    - Up to 205 differential I/O pairs that can be input, output, or bidirectional
    - Hot swap I/O (CompactPCI friendly)
- Core logic powered at 1.8V and I/Os powered at 1.5V, 2.5V, or 3.3V
- Fully supported by powerful Xilinx® ISE® development system
    - Fully automatic mapping, placement, and routing
    - Integrated with design entry and verification tools
    - Extensive IP library including DSP functions and soft processors

Table 1: **Spartan-IIE FPGA Family Members**

Device	Logic Cells	Typical System Gate Range (Logic and RAM)	CLB Array (R x C)	Total CLBs	Maximum Available User I/O(1)	Maximum Differential I/O Pairs	Distributed RAM Bits	Block RAM Bits
XC2S50E	1,728	23,000 - 50,000	16 x 24	384	182	83	24,576	32K
XC2S100E	2,700	37,000 - 100,000	20 x 30	600	202	86	38,400	40K
XC2S150E	3,888	52,000 - 150,000	24 x 36	864	265	114	55,296	48K
XC2S200E	5,292	71,000 - 200,000	28 x 42	1,176	289	120	75,264	56K
XC2S300E	6,912	93,000 - 300,000	32 x 48	1,536	329	120	98,304	64K
XC2S400E	10,800	145,000 - 400,000	40 x 60	2,400	410	172	153,600	160K
XC2S600E	15,552	210,000 - 600,000	48 x 72	3,456	514	205	221,184	288K

Notes:

1. User I/O counts include the four global clock/user input pins. See details in Table 2, page 5

Revision History

Date	Version	Description
06/27/2002	1.1	Updated -7 availability.
11/18/2002	2.0	Added XC2S400E and XC2S600E. Corrected XC2S150E max I/O count and XC2S50E differential I/O count and updated availability.
07/09/2003	2.1	Noted hot-swap capability. Updated Table 2 to show that all products are available. Clarified device part marking.
07/28/2004	2.2	Added information on Pb-free packaging options.
06/18/2008	2.3	Added dual mark information in Device Part Marking. Updated all modules for continuous page, figure, and table numbering. Updated links. Synchronized all modules to v2.3.
08/09/2013	3.0	This product is obsolete/discontinued per XCN12026.

Optional pull-up and pull-down resistors and an optional weak-keeper circuit are attached to each user I/O pad. Prior to configuration all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but inputs may optionally be pulled up. The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins will float. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. After configuration, clamping diodes are connected to V_{CCO} for LVTTL, PCI, HSTL, SSTL, CTT, and AGP standards.

All Spartan-IIE FPGA IOBs support IEEE 1149.1-compatible boundary scan testing.

Input Path

A buffer in the IOB input path routes the input signal directly to internal logic and through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF} The need to supply V_{REF} imposes constraints on which standards can used in close proximity to each other. See I/O Banking.

There are optional pull-up and pull-down resistors at each input for use after configuration.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. Each output buffer can source up to 24 mA and sink up to 48 mA. Drive strength and slew rate controls minimize bus transients. The default output driver is LVTTL with 12 mA drive strength and slow slew rate.

In most signaling standards, the output high voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See I/O Banking.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way helps eliminate bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signaling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks (see Figure 5). The pinout tables show the bank affiliation of each I/O (see Pinout Tables, page 53). Each bank has multiple V_{CCO} pins which must be connected to the same voltage. Voltage requirements are determined by the output standards in use.

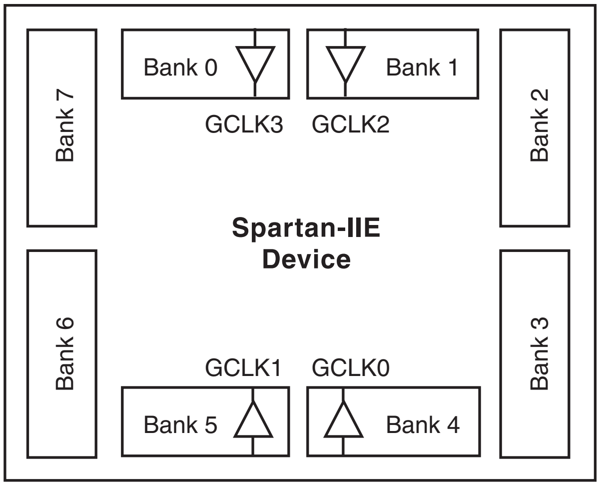

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Figure 5: **Spartan-IIE I/O Banks**

In the TQ144 and PQ208 packages, the eight banks have V_{CCO} connected together. Thus, only one V_{CCO} level is allowed in these packages, although different V_{REF} values are allowed in each of the eight banks.

Within a bank, standards may be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 4. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO}. Note that V_{CCO}

Configurable Logic Block

The basic building block of the Spartan-IIE FPGA CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and storage element. The output from the function generator in each LC drives the CLB output or the D input of the flip-flop. Each Spartan-IIE FPGA CLB contains four LCs, organized in two similar slices; a single slice is shown in Figure 6.

In addition to the four basic LCs, the Spartan-IIE FPGA CLB contains logic that combines function generators to provide functions of five or six inputs.

Look-Up Tables

Spartan-IIE FPGA function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16 x 1-bit dual-port synchronous RAM.

The Spartan-IIE FPGA LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

Storage Elements

Storage elements in the Spartan-IIE FPGA slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals may be configured to operate asynchronously.

All control signals are independently invertible, and are shared by the two flip-flops within the slice.

Table 7 shows the depth and width aspect ratios for the block RAM.

Table 7: **Block RAM Port Aspect Ratios**

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

The Spartan-IIE FPGA block RAM also includes dedicated routing to provide an efficient interface with both CLBs and other block RAMs. See Xilinx Application Note XAPP173 for more information on block RAM.

Programmable Routing

It is the longest delay path that limits the speed of any design. Consequently, the Spartan-IIE FPGA routing architecture and its place-and-route software were defined jointly to minimize long-path delays and yield the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

The software automatically uses the best available routing based on user timing requirements. The details are provided here for reference.

Local Routing

The local routing resources, as shown in Figure 9, provide the following three types of connections:

- Interconnections among the LUTs, flip-flops, and General Routing Matrix (GRM), described below.
- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM

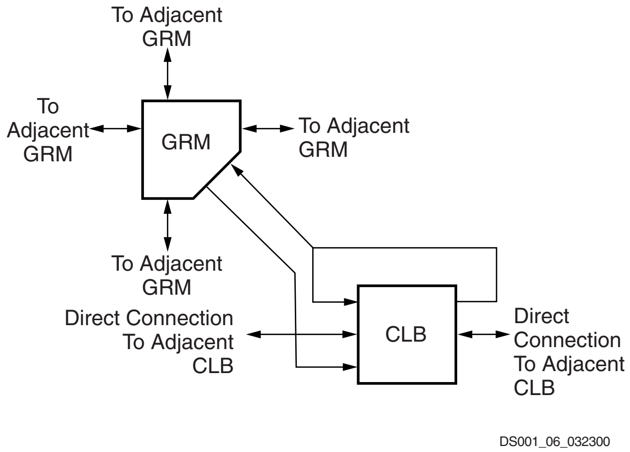


Figure 9: **Spartan-IIE Local Routing**

General Purpose Routing

Most Spartan-IIE FPGA signals are routed on the general purpose routing, and consequently, the majority of interconnect resources are associated with this level of the routing hierarchy. The general routing resources are located in horizontal and vertical routing channels associated with the rows and columns of CLBs. The general-purpose routing resources are listed below.

- Adjacent to each CLB is a General Routing Matrix (GRM). The GRM is the switch matrix through which horizontal and vertical routing resources connect, and is also the means by which the CLB gains access to the general purpose routing.
- 24 single-length lines route GRM signals to adjacent GRMs in each of the four directions.
- 96 buffered Hex lines route GRM signals to other GRMs six blocks away in each one of the four directions. Organized in a staggered pattern, Hex lines may be driven only at their endpoints. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source). One third of the Hex lines are bidirectional, while the remaining ones are unidirectional.
- 12 Longlines are buffered, bidirectional wires that distribute signals across the device quickly and efficiently. Vertical Longlines span the full height of the device, and horizontal ones span the full width of the device.

I/O Routing

Spartan-IIE devices have additional routing resources around their periphery that form an interface between the CLB array and the IOBs. This additional routing, called the VersaRing™ routing, facilitates pin-swapping and pin-locking, such that logic redesigns can adapt to existing PCB layouts. Time-to-market is reduced, since PCBs and other system components can be manufactured while the logic design is still in progress.

Dedicated Routing

Some classes of signal require dedicated routing resources to maximize performance. In the Spartan-IIE FPGA architecture, dedicated routing resources are provided for two classes of signal.

- Horizontal routing resources are provided for on-chip 3-state busses. Four partitionable bus lines are provided per CLB row, permitting multiple busses within a row, as shown in Figure 10.
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.

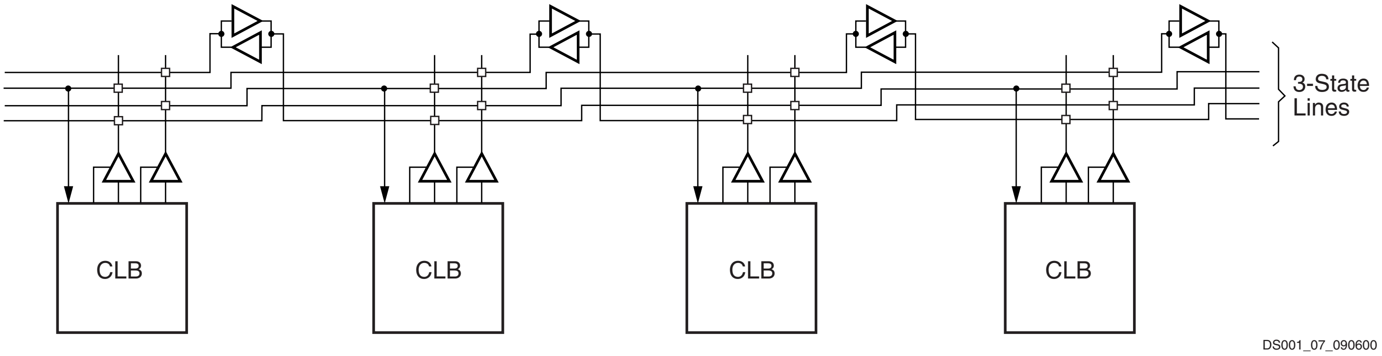


Figure 10: **BUFT Connections to Dedicated Horizontal Bus Lines**

Global Routing

Global Routing resources distribute clocks and other signals with very high fanout throughout the device. Spartan-IIE devices include two tiers of global routing resources referred to as primary and secondary global routing resources.

- The primary global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The primary global nets may only be driven by global buffers. There are four global buffers, one for each global net.
- The secondary global routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across the bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These secondary resources are more flexible than the primary resources since they are not restricted to routing only to clock pins.

Clock Distribution

The Spartan-IIE family provides high-speed, low-skew clock distribution through the primary global routing resources described above. A typical clock distribution net is shown in Figure 11.

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four primary global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing.

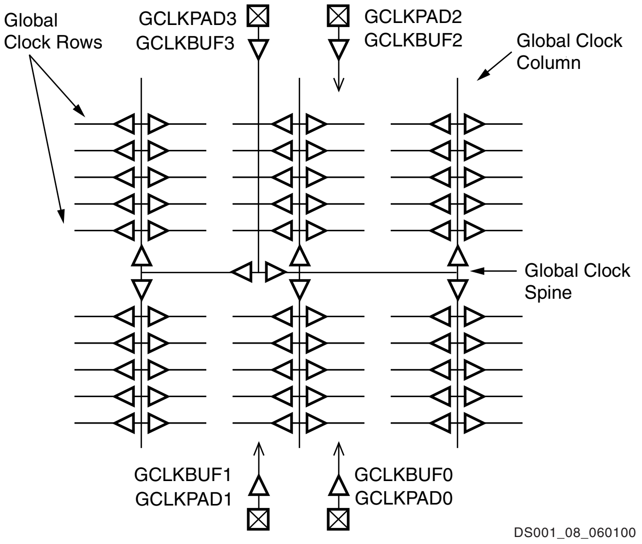


Figure 11: **Global Clock Distribution Network**

Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element (Figure 12). Additional delay is introduced such that clock edges reach internal flip-flops exactly one clock period after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock

During start-up, the device performs four operations:

1. The assertion of DONE. The failure of DONE to go High may indicate the unsuccessful loading of configuration data.
2. The release of the Global Three State (GTS). This activates all the I/Os to which signals are assigned. The remaining I/Os stay in a high-impedance state with internal weak pull-up resistors present.
3. The release of the Global Set Reset (GSR). This allows all flip-flops to change state.
4. The assertion of Global Write Enable (GWE). This allows all RAMs and flip-flops to change state.

By default, these operations are synchronized to CCLK. The entire start-up sequence lasts eight cycles, called C0-C7, after which the loaded design is fully functional. The four operations can be selected to switch on any CCLK cycle C1-C6 through settings in the Xilinx Development Software. The default timing for start-up is shown in the top half of Figure 17; heavy lines show default settings.

The default Start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The bottom half of Figure 17 shows another commonly used version of the start-up timing known as Sync-to-DONE. This version makes the GTS, GSR, and GWE events conditional upon the DONE pin going High. This timing is important for a daisy chain of multiple FPGAs in serial mode, since it ensures that all FPGAs go through start-up together, after all their DONE pins have gone High.

Sync-to-DONE timing is selected by setting the GTS, GSR, and GWE cycles to a value of DONE in the configuration options. This causes these signals to transition one clock cycle after DONE externally transitions High.

The sequence can also be paused at any stage until lock has been achieved on any or all DLLs.

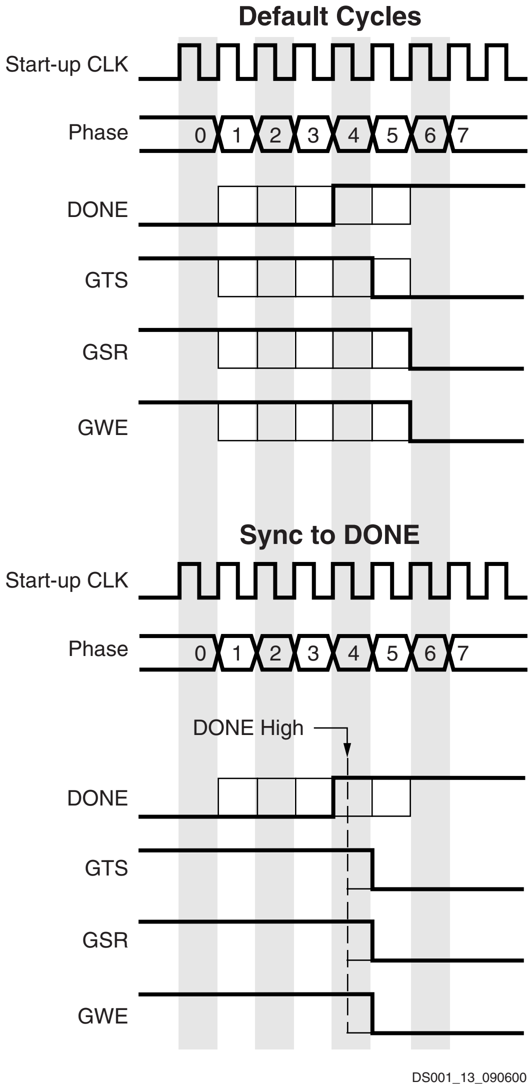


Figure 17: **Start-Up Waveforms**

Serial Modes

There are two serial configuration modes. In Master Serial mode, the FPGA controls the configuration process by driving CCLK as an output. In Slave Serial mode, the FPGA passively receives CCLK as an input from an external agent (e.g., a microprocessor, CPLD, or second FPGA in master mode) that is controlling the configuration process. In both modes, the FPGA is configured by loading one bit per CCLK cycle. The MSB of each configuration data byte is always written to the DIN pin first.

See Figure 18 for the sequence for loading data into the Spartan-IIE FPGA serially. This is an expansion of the "Load Configuration Data Frames" block in Figure 16, page 23. Note that $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$ are not normally used during serial configuration. To ensure successful loading of the FPGA, do not toggle $\overline{\text{WRITE}}$ with $\overline{\text{CS}}$ Low during serial configuration.

Revision History

Date	Version	Description
11/15/2001	1.0	Initial Xilinx release.
11/18/2002	2.0	Added XC2S400E and XC2S600E. Removed Preliminary designation. Clarified details of I/O standards, boundary scan, and configuration.
07/09/2003	2.1	Added hot swap description (see Hot Swap, Hot Insertion, Hot Socketing Support). Added Table 9 containing JTAG IDCODE values. Clarified configuration PROM support.
06/18/2008	2.3	Added note that TDI, TMS, and TCK have a default pull-up resistor. Add note on maximum daisy-chain limit. Updated Figure 19 since Mode pins can be pulled up to either 2.5V or 3.3V. Updated all modules for continuous page, figure, and table numbering. Updated links. Synchronized all modules to v2.3.
08/09/2013	3.0	This product is obsolete/discontinued per XCN12026.

Spartan-IIE FPGA Family: DC and Switching Characteristics

DS077-3 (v3.0) August 9, 2013

Product Specification

Definition of Terms

In this document, some specifications may be designated as Advance or Preliminary. These designations are based on the more detailed timing information used by the development system and reported in the output files. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. All specifications are subject to change without notice.

DC Specifications

Absolute Maximum Ratings(1)

Symbol	Description	Min	Max	Units
V_{CCINT}	Supply voltage relative to GND	–0.5	2.0	V
V_{CCO}	Supply voltage relative to GND	–0.5	4.0	V
V_{REF}	Input reference voltage	–0.5	4.0	V
V_{IN}	Input voltage relative to GND(2,3)	–0.5	4.0	V
V_{TS}	Voltage applied to 3-state output(3)	–0.5	4.0	V
T_{STG}	Storage temperature (ambient)	–65	+150	°C
T_J	Junction temperature	-	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. V_{IN} should not exceed V_{CCO} by more than 3.6V over extended periods of time (e.g., longer than a day).
3. Maximum DC overshoot must be limited to either V_{CCO} + 0.5V or 10 mA, and undershoot must be limited to –0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to –2.0V or overshoot to V_{CCO} + 2.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
4. For soldering guidelines, see the Packaging Information on the Xilinx® website.

Clock Distribution Switching Characteristics

T_{GPIO} is specified for LVTTL levels. For other standards, adjust T_{GPIO} with the values shown in I/O Standard Global Clock Input Adjustments.

Symbol	Description	Speed Grade -7 Max	Speed Grade -6 Max	Units
GCLK IOB and Buffer				
T_{GPIO}	Global clock pad to output	0.7	0.7	ns
T_{GIO}	Global clock buffer I input to O output	0.45	0.5	ns

I/O Standard Global Clock Input Adjustments

Delays associated with a global clock input pad are specified for LVTTL levels. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade -7	Speed Grade -6	Units
Data Input Delay Adjustments					
$T_{GPLVTTL}$	Standard-specific global clock input delay adjustments	LVTTL	0	0	ns
$T_{GPLVCMOS2}$		LVCMOS2	0	0	ns
$T_{GPLVCMOS18}$		LVCMOS18	0.2	0.2	ns
$T_{GPLVCDS}$		LVDS	0.38	0.38	ns
$T_{GPLVPECL}$		LVCPECL	0.38	0.38	ns
$T_{GPPCI33\_3}$		PCI, 33 MHz, 3.3V	0.08	0.08	ns
$T_{GPPCI66\_3}$		PCI, 66 MHz, 3.3V	–0.11	–0.11	ns
T_{GPGTL}		GTL	0.37	0.37	ns
T_{GPGTLP}		GTL+	0.37	0.37	ns
T_{GPHSTL}		HSTL	0.27	0.27	ns
$T_{GPSSTL2}$		SSTL2	0.27	0.27	ns
$T_{GPSSTL3}$		SSTL3	0.27	0.27	ns
T_{GPCTT}		CTT	0.33	0.33	ns
T_{GPAGP}		AGP	0.27	0.27	ns

Notes:

1. Input timing for GPLVTTL is measured at 1.4V. For other I/O standards, see the table Delay Measurement Methodology, page 41.

DLL Timing Parameters

Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

			Speed Grade				
			-7		-6		
Symbol	**Description**	**F_{CLKIN}**	**Min**	**Max**	**Min**	**Max**	**Units**
$F_{CLKINHF}$	Input clock frequency (CLKDLLHF)	-	60	320	60	275	MHz
$F_{CLKINLF}$	Input clock frequency (CLKDLL)	-	25	160	25	135	MHz
T_{DLLPW}	Input clock pulse width	≥25 MHz	5.0	-	5.0	-	ns
		≥50 MHz	3.0	-	3.0	-	ns
		≥100 MHz	2.4	-	2.4	-	ns
		≥150 MHz	2.0	-	2.0	-	ns
		≥200 MHz	1.8	-	1.8	-	ns
		≥250 MHz	1.5	-	1.5	-	ns
		≥300 MHz	1.3	-	NA	-	

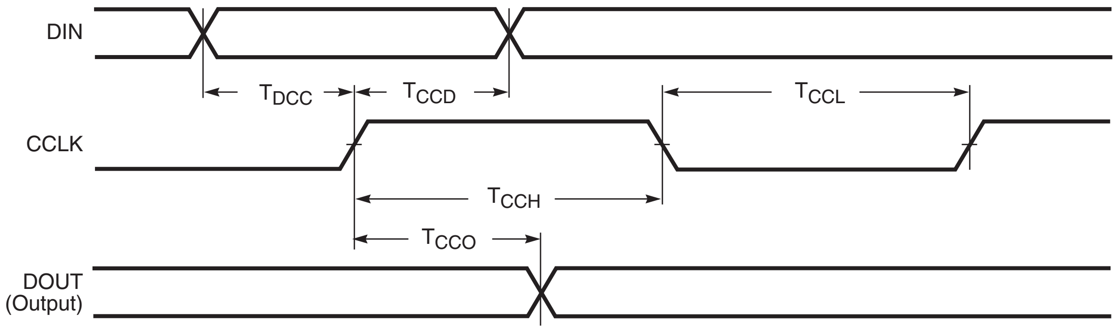
DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications were determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers. Figure 22, page 44, provides definitions for various parameters in the table below.

			CLKDLLHF		CLKDLL		
Symbol	**Description**	**F_{CLKIN}**	**Min**	**Max**	**Min**	**Max**	**Units**
T_{IPTOL}	Input clock period tolerance		-	1.0	-	1.0	ns
T_{IJITCC}	Input clock jitter tolerance (cycle-to-cycle)		-	±150	-	±300	ps
T_{LOCK}	Time required for DLL to acquire lock(1)	> 60 MHz	-	20	-	20	µs
		50-60 MHz	-	-	-	25	µs
		40-50 MHz	-	-	-	50	µs
		30-40 MHz	-	-	-	90	µs
		25-30 MHz	-	-	-	120	µs
T_{OJITCC}	Output jitter (cycle-to-cycle) for any DLL clock output(2)		-	±60	-	±60	ps
T_{PHIO}	Phase offset between CLKIN and CLKO(3)		-	±100	-	±100	ps
T_{PHOO}	Phase offset between clock outputs on the DLL(4)		-	±140	-	±140	ps
T_{PHIOM}	Phase difference between CLKIN and CLKO(5)		-	±160	-	±160	ps
T_{PHOOM}	Phase difference between clock outputs on the DLL(6)		-	±200	-	±200	ps

Notes:

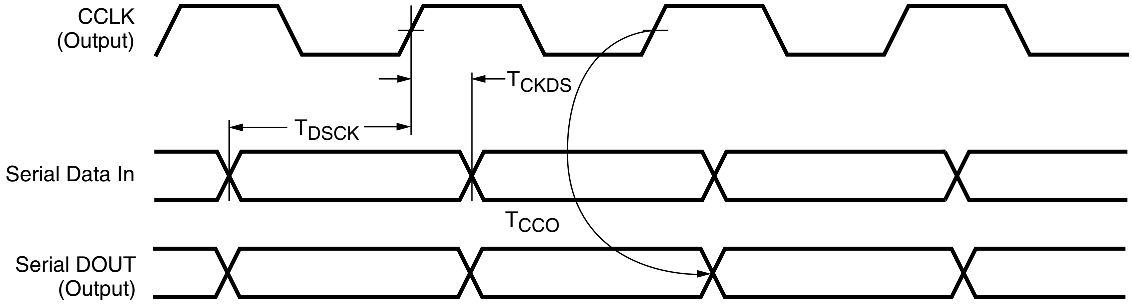
1. Commercial operating conditions. Add 30% for Industrial operating conditions.
2. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
3. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* output jitter and input clock jitter.
4. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* output jitter and input clock jitter.
5. **Maximum Phase Difference between CLKIN and CLKO** is the sum of output jitter and phase offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
6. **Maximum Phase Difference between Clock Outputs on the DLL** is the sum of output jitter and phase offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).



DS001_16_032300

Symbol		Description	All Devices		Units
			Min	Max	
T_{DCC} / T_{CCD}	CCLK	DIN setup/hold	5 / 0	-	ns
T_{CCO}		DOUT	-	12	ns
T_{CCH}		High time	5	-	ns
T_{CCL}		Low time	5	-	ns
F_{CC}		Maximum frequency	-	66	MHz

Figure 24: **Slave Serial Mode Timing**



DS001_17_110101

Symbol		Description	All Devices		Units
			Min	Max	
T_{DSCK} / T_{CKDS}	CCLK	DIN setup/hold	5 / 0	-	ns
T_{CCO}		DOUT	-	12	ns
F_{CC}		Frequency tolerance with respect to nominal	–30%	+45%	-

Figure 25: **Master Serial Mode Timing**

Package Thermal Characteristics

Table 14 provides the thermal characteristics for the various Spartan-II FPGA package offerings. This information is also available using the Thermal Query tool on xilinx.com (www.xilinx.com/cgi-bin/thermal/thermal.pl).

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board (θ_{JB}) value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The "Still Air (0 LFM)" column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 14: **Spartan-IIE Package Thermal Characteristics**

Package	Device	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
TQ144 TQG144	XC2S50E	5.8	N/A	32.3	25.1	21.5	20.1	°C/Watt
	XC2S100E	5.3	N/A	31.4	24.4	20.8	19.6	°C/Watt
PQ208 PQG208	XC2S50E	7.1	N/A	35.1	25.9	22.9	21.2	°C/Watt
	XC2S100E	6.1	N/A	34.2	25.2	22.3	20.7	°C/Watt
	XC2S150E	6.0	N/A	34.1	25.2	22.2	20.6	°C/Watt
	XC2S200E	4.6	N/A	32.4	23.9	21.2	19.6	°C/Watt
	XC2S300E	4.0	N/A	31.6	23.3	20.6	19.1	°C/Watt
FT256 FTG256	XC2S50E	7.3	17.8	27.4	21.6	20.4	20.0	°C/Watt
	XC2S100E	5.8	15.1	25.0	19.5	18.2	17.8	°C/Watt
	XC2S150E	5.7	14.8	24.8	19.3	18.0	17.6	°C/Watt
	XC2S200E	3.9	11.4	21.9	16.6	15.2	14.7	°C/Watt
	XC2S300E	3.2	10.1	20.8	15.6	14.2	13.7	°C/Watt
	XC2S400E	2.5	8.8	19.7	14.5	13.2	12.6	°C/Watt
FG456 FGG456	XC2S100E	8.4	14.9	24.3	19.2	18.1	17.4	°C/Watt
	XC2S150E	8.2	14.6	24.1	19.0	17.9	17.1	°C/Watt
	XC2S200E	6.3	11.6	21.0	16.1	15.0	14.3	°C/Watt
	XC2S300E	5.6	10.4	19.9	15.1	13.9	13.2	°C/Watt
	XC2S400E	3.6	6.5	17.7	11.7	10.5	10.0	°C/Watt
	XC2S600E	2.7	5.0	17.3	11.2	10.0	9.5	°C/Watt
FG676 FGG676	XC2S400E	4.1	7.9	15.6	11.1	9.8	9.2	°C/Watt
	XC2S600E	3.4	6.9	14.5	9.9	8.6	7.9	°C/Watt

Pinout Tables

The following device-specific pinout tables include all packages available for each Spartan-IIE device. They follow the pad locations around the die. In the TQ144 package, all VCCO pins must be connected to the same voltage.

TQ144 Pinouts (XC2S50E and XC2S100E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
GND	-	P1	-	-
TMS	-	P2	-	-
I/O	7	P3	-	-
I/O	7	P4	-	-
I/O, VREF Bank 7	7	P5	-	All
I/O	7	P6	-	-
I/O, L27P	7	P7	XC2S50E	XC2S100E
I/O, L27N	7	P8	XC2S50E	-
GND	-	P9	-	-
I/O, L26P_YY	7	P10	All	-
I/O, L26N_YY	7	P11	All	-
I/O, VREF Bank 7, L25P	7	P12	XC2S50E	All
I/O, L25N	7	P13	XC2S50E	-
I/O	7	P14	-	-
I/O (IRDY)	7	P15	-	-
GND	-	P16	-	-
VCCO	-	P17	-	-
I/O (TRDY)	6	P18	-	-
VCCINT	-	P19	-	-
I/O	6	P20	-	-
I/O, L24P	6	P21	XC2S50E	-
I/O, VREF Bank 6, L24N	6	P22	XC2S50E	All
I/O, L23P_YY	6	P23	All	-
I/O, L23N_YY	6	P24	All	-
GND	-	P25	-	-
I/O, L22P	6	P26	XC2S50E	-

TQ144 Pinouts (XC2S50E and XC2S100E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L22N	6	P27	XC2S50E	XC2S100E
I/O	6	P28	-	-
I/O, VREF Bank 6	6	P29	-	All
I/O	6	P30	-	-
I/O, L21P_YY	6	P31	All	-
I/O, L21N_YY	6	P32	All	-
M1	-	P33	-	-
GND	-	P34	-	-
M0	-	P35	-	-
VCCO	-	P36	-	-
M2	-	P37	-	-
I/O, L20N_YY	5	P38	All	-
I/O, L20P_YY	5	P39	All	-
I/O	5	P40	-	-
I/O, VREF Bank 5	5	P41	-	All
I/O	5	P42	-	-
I/O, L19N_YY	5	P43	All	XC2S100E
I/O, L19P_YY	5	P44	All	-
GND	-	P45	-	-
VCCINT	-	P46	-	-
I/O, L18N_YY	5	P47	All	-
I/O, L18P_YY	5	P48	All	-
I/O, VREF Bank 5	5	P49	-	All
I/O (DLL), L17N	5	P50	-	-
VCCINT	-	P51	-	-
GCK1, I	5	P52	-	-
VCCO	5	P53	-	-
GND	-	P54	-	-
GCK0, I	4	P55	-	-

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O	7	H5	-	-	-	-	-	I/O	I/O	I/O
I/O, VREF Bank 7, L#P_Y	7	H3	XC2S300E, 400E, 600E	All	I/O, VREF Bank 7, L81P	I/O, VREF Bank 7, L106P	I/O, VREF Bank 7, L113P	I/O, VREF Bank 7, L113P_Y	I/O, VREF Bank 7, L113P_Y	I/O, VREF Bank 7, L113P_Y
I/O, L#N_Y	7	H4	XC2S300E, 400E, 600E	-	I/O, L81N	I/O, L106N	I/O, L113N	I/O, L113N_Y	I/O, L113N_Y	I/O, L113N_Y
I/O, L#P_YY	7	H2	All	-	I/O, L80P_YY	I/O, L105P_YY	I/O, L112P_YY	I/O, L112P_YY	I/O, L112P_YY	I/O, L112P_YY
I/O, L#N_YY	7	H1	All	-	I/O, L80N_YY	I/O, L105N_YY	I/O, L112N_YY	I/O, L112N_YY	I/O, L112N_YY	I/O, L112N_YY
I/O	7	J6	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	J4	XC2S150E, 200E, 300E, 400E	-	-	I/O, L104P_Y	I/O, L111P_Y	I/O, L111P_Y	I/O, L111P_Y	I/O, L111P
I/O, L#N_Y	7	J5	XC2S100E, 150E, 200E, 300E, 400E	-	I/O, L79P_Y	I/O, L104N_Y	I/O, L111N_Y	I/O, L111N_Y	I/O, L111N_Y	I/O, L111N
I/O, L#P_Y	7	J3	XC2S100E, 150E, 200E, 300E, 600E	-	I/O, L79N_Y	I/O, L103P_Y	I/O, L110P_Y	I/O, L110P_Y	I/O, L110P	I/O, L110P_Y
I/O, L#N_Y	7	J2	XC2S150E, 200E, 300E, 600E	-	-	I/O, L103N_Y	I/O, L110N_Y	I/O, L110N_Y	I/O, L110N	I/O, L110N_Y
I/O	7	J1	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#P	7	K5	XC2S100E, 150E, 200E, 300E, 600E(1)	-	I/O, L78P_YY	I/O, L102P_YY	I/O, L109P_YY	I/O, L109P_YY	I/O, L109P	I/O, L109P_Y
I/O, L#N	7	K6	XC2S100E, 150E, 200E, 300E, 600E(1)	-	I/O, L78N_YY	I/O, L102N_YY	I/O, L109N_YY	I/O, L109N_YY	I/O, L109N	I/O, L109N_Y
I/O, VREF Bank 7, L#P_Y	7	K3	XC2S300E, 400E, 600E	All	I/O, VREF Bank 7, L77P	I/O, VREF Bank 7, L101P	I/O, VREF Bank 7, L108P	I/O, VREF Bank 7, L108P_Y	I/O, VREF Bank 7, L108P_Y	I/O, VREF Bank 7, L108P_Y
I/O, L#N_Y	7	K4	XC2S300E, 400E, 600E	-	I/O, L77N	I/O, L101N	I/O, L108N	I/O, L108N_Y	I/O, L108N_Y	I/O, L108N_Y
I/O	7	K2	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P_Y	7	K1	XC2S300E, 400E	-	-	-	I/O, L107P	I/O, L107P_Y	I/O, L107P_Y	I/O, L107P
I/O, L#N_Y	7	L1	XC2S100E, 150E, 300E, 400E	-	I/O, L76P_Y	I/O, L100P_Y	I/O, L107N	I/O, L107N_Y	I/O, L107N_Y	I/O, L107N
I/O, L#P_Y	7	L3	XC2S100E, 150E, 200E, 300E, 600E	XC2S400E, 600E	I/O, L76N_Y	I/O, L100N_Y	I/O, L106P_Y	I/O, L106P_Y	I/O, VREF Bank 7, L106P	I/O, VREF Bank 7, L106P_Y
I/O, L#N_Y	7	L2	XC2S200E, 300E, 600E	-	-	I/O	I/O, L106N_Y	I/O, L106N_Y	I/O, L106N	I/O, L106N_Y
I/O	7	L4	-	-	-	-	-	I/O	I/O	I/O

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name					Device-Specific Pinouts: XC2S					
Function	**Bank**	**Pin**	**LVDS Async. Output Option**	**V_{REF} Option**	**100E**	**150E**	**200E**	**300E**	**400E**	**600E**
I/O, L#P_YY	7	L5	All	-	I/O, L75P_YY	I/O, L99P_YY	I/O, L105P_YY	I/O, L105P_YY	I/O, L105P_YY	I/O, L105P_YY
I/O (IRDY), L#N_YY	7	L6	All	-	I/O (IRDY), L75N_YY	I/O (IRDY), L99N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY
I/O (TRDY)	6	M1	-	-	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)
I/O	6	M2	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P_Y	6	M3	XC2S200E, 300E, 600E	-	-	I/O	I/O, L104P_Y	I/O, L104P_Y	I/O, L104P	I/O, L104P_Y
I/O, L#N_Y	6	M4	XC2S100E, 150E, 200E, 300E, 600E	XC2S400E, 600E	I/O, L74P_Y	I/O, L98P_Y	I/O, L104N_Y	I/O, L104N_Y	I/O, VREF Bank 6, L104N	I/O, VREF Bank 6, L104N_Y
I/O, L#P_Y	6	M5	XC2S100E, 150E, 300E, 400E	-	I/O, L74N_Y	I/O, L98N_Y	I/O, L103P	I/O, L103P_Y	I/O, L103P_Y	I/O, L103P
I/O, L#N_Y	6	M6	XC2S300E, 400E	-	-	-	I/O, L103N	I/O, L103N_Y	I/O, L103N_Y	I/O, L103N
I/O	6	N1	-	-	-	-	-	I/O	I/O	I/O
I/O	6	N2	-	-	I/O, L73P	I/O, L97P	I/O	I/O	I/O	I/O
I/O, VREF Bank 6, L#P	6	N3	XC2S200E, 400E	All	I/O, VREF Bank 6, L73N	I/O, VREF Bank 6, L97N	I/O, VREF Bank 6, L102P_Y	I/O, VREF Bank 6, L102P	I/O, VREF Bank 6, L102P_Y	I/O, VREF Bank 6, L102P
I/O, L#N	6	N4	XC2S100E, 150E, 200E, 400E	-	I/O, L72P_Y	I/O, L96P_Y	I/O, L102N_Y	I/O, L102N	I/O, L102N_Y	I/O, L102N
I/O, L#P_Y	6	N5	XC2S100E, 150E, 300E, 600E	-	I/O, L72N_Y	I/O, L96N_Y	I/O, L101P	I/O, L101P_Y	I/O, L101P	I/O, L101P_Y
I/O, L#N_Y	6	N6	XC2S300E, 600E	-	-	-	I/O, L101N	I/O, L101N_Y	I/O, L101N	I/O, L101N_Y
I/O, L#P_Y	6	P1	XC2S150E, 200E, 300E, 600E	-	-	I/O, L95P_Y	I/O, L100P_Y	I/O, L100P_Y	I/O, L100P	I/O, L100P_Y
I/O, L#N_Y	6	P2	XC2S100E, 150E, 200E, 300E, 600E	-	I/O, L71P_Y	I/O, L95N_Y	I/O, L100N_Y	I/O, L100N_Y	I/O, L100N	I/O, L100N_Y
I/O	6	R1	XC2S100E, 150E	-	I/O, L71N_Y	I/O, L94P_Y	I/O	I/O	I/O	I/O
I/O, L#P_Y	6	P3	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L94N_Y	I/O, L99P_Y	I/O, L99P_Y	I/O, L99P_Y	I/O, L99P_Y
I/O, L#N_Y	6	P4	XC2S200E, 300E, 400E, 600E	-	-	-	I/O, L99N_Y	I/O, L99N_Y	I/O, L99N_Y	I/O, L99N_Y
I/O, L#P_YY	6	P5	All	-	I/O, L70P_YY	I/O, L93P_YY	I/O, L98P_YY	I/O, L98P_YY	I/O, L98P_YY	I/O, L98P_YY
I/O, L#N_YY	6	P6	All	-	I/O, L70N_YY	I/O, L93N_YY	I/O, L98N_YY	I/O, L98N_YY	I/O, L98N_YY	I/O, L98N_YY

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O, L#N	3	V19	XC2S150E, 200E, 300E, 400E	-	-	I/O, L54N_Y	I/O, L58N_Y	I/O, L58N_Y	I/O, L58N_Y	I/O, L58N
I/O, L#P	3	V20	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L54P_Y	I/O, L58P_Y	I/O, L58P_Y	I/O, L58P_Y	I/O, L58P
I/O, L#N	3	V22	XC2S100E, 200E, 300E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L40N_Y	I/O, L53N	I/O, VREF Bank 3, L57N_Y	I/O, VREF Bank 3, L57N_Y	I/O, VREF Bank 3, L57N	I/O, VREF Bank 3, L57N_Y
I/O, L#P	3	U22	XC2S100E, 200E, 300E, 600E	-	I/O, L40P_Y	I/O, L53P	I/O, L57P_Y	I/O, L57P_Y	I/O, L57P	I/O, L57P_Y
I/O	3	U21	-	-	-	-	-	I/O	I/O	I/O
I/O	3	U20	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N	3	U18	XC2S100E, 200E, 300E, 600E	-	I/O, L39N_Y	I/O, L52N	I/O, L56N_Y	I/O, L56N_Y	I/O, L56N	I/O, L56N_Y
I/O, L#P	3	U19	XC2S100E, 200E, 300E, 600E	-	I/O, L39P_Y	I/O, L52P	I/O, L56P_Y	I/O, L56P_Y	I/O, L56P	I/O, L56P_Y
I/O, VREF Bank 3, L#N	3	T21	XC2S150E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 3, L38N	I/O, VREF Bank 3, L51N_Y	I/O, VREF Bank 3, L55N_Y	I/O, VREF Bank 3, L55N_Y	I/O, VREF Bank 3, L55N_Y	I/O, VREF Bank 3, L55N_Y
I/O, L#P	3	T22	XC2S150E, 200E, 300E, 400E, 600E	-	I/O, L38P	I/O, L51P_Y	I/O, L55P_Y	I/O, L55P_Y	I/O, L55P_Y	I/O, L55P_Y
I/O	3	T20	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N	3	T18	XC2S150E, 200E, 300E, 400E	-	-	I/O, L50N_Y	I/O, L54N_Y	I/O, L54N_Y	I/O, L54N_Y	I/O, L54N
I/O, L#P	3	T19	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L50P_Y	I/O, L54P_Y	I/O, L54P_Y	I/O, L54P_Y	I/O, L54P
I/O, L#N	3	R21	XC2S100E, 150E, 300E, 600E	XC2S600E	I/O, L37N_Y	I/O, L49N_Y	I/O, L53N	I/O, L53N_Y	I/O, L53N	I/O, VREF Bank 3, L53N_Y
I/O, L#P	3	R22	XC2S100E, 150E, 300E, 600E	-	I/O, L37P_Y	I/O, L49P_Y	I/O, L53P	I/O, L53P_Y	I/O, L53P	I/O, L53P_Y
I/O	3	R20	-	-	-	-	-	I/O	I/O	I/O
I/O, VREF Bank 3, L#N	3	R18	XC2S300E, 400E, 600E	All	I/O, VREF Bank 3, L36N	I/O, VREF Bank 3, L48N	I/O, VREF Bank 3, L52N	I/O, VREF Bank 3, L52N_Y	I/O, VREF Bank 3, L52N_Y	I/O, VREF Bank 3, L52N_Y
I/O (D6), L#P	3	R19	XC2S300E, 400E, 600E	-	I/O (D6), L36P	I/O (D6), L48P	I/O (D6), L52P	I/O (D6), L52P_Y	I/O (D6), L52P_Y	I/O (D6), L52P_Y
I/O (D5), L#N_YY	3	P22	All	-	I/O (D5), L35N_YY	I/O (D5), L47N_YY	I/O (D5), L51N_YY	I/O (D5), L51N_YY	I/O (D5) L51N_YY	I/O (D5), L51N_YY
I/O, L#P_YY	3	P21	All	-	I/O, L35P_YY	I/O, L47P_YY	I/O, L51P_YY	I/O, L51P_YY	I/O, L51P_YY	I/O, L51P_YY

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name					Device-Specific Pinouts: XC2S					
Function	**Bank**	**Pin**	**LVDS Async. Output Option**	**V_{REF} Option**	**100E**	**150E**	**200E**	**300E**	**400E**	**600E**
I/O ($\overline{\text{WRITE}}$), L#N_YY	1	A20	All	-	I/O ($\overline{\text{WRITE}}$), L20N_YY	I/O ($\overline{\text{WRITE}}$), L26N_YY	I/O ($\overline{\text{WRITE}}$), L28N_YY	I/O ($\overline{\text{WRITE}}$), L28N_YY	I/O ($\overline{\text{WRITE}}$), L28N_YY	I/O ($\overline{\text{WRITE}}$), L28N_YY
I/O	1	D18	-	-	-	-	-	I/O	I/O	I/O
I/O	1	C18	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P	1	B19	XC2S200E, 300E, 400E, 600E	-	-	I/O, L25P	I/O, L27P_Y	I/O, L27P_Y	I/O, L27P_Y	I/O, L27P_Y
I/O, L#N	1	A19	XC2S200E, 300E, 400E, 600E	-	I/O	I/O, L25N	I/O, L27N_Y	I/O, L27N_Y	I/O, L27N_Y	I/O, L27N_Y
I/O, L#P	1	B18	XC2S100E, 200E, 300E, 400E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L19P_Y	I/O, L24P	I/O, VREF Bank 1, L26P_Y	I/O, VREF Bank 1, L26P_Y	I/O, VREF Bank 1, L26P_Y	I/O, VREF Bank 1, L26P_Y
I/O, L#N	1	A18	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L19N_Y	I/O, L24N	I/O, L26N_Y	I/O, L26N_Y	I/O, L26N_Y	I/O, L26N_Y
I/O	1	D17	-	-	-	-	-	I/O	I/O	I/O
I/O	1	C17	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P_YY	1	B17	All	-	I/O, L18P_YY	I/O, L23P_YY	I/O, L25P_YY	I/O, L25P_YY	I/O, L25P_YY	I/O, L25P_YY
I/O, L#N_YY	1	A17	All	-	I/O, L18N_YY	I/O, L23N_YY	I/O, L25N_YY	I/O, L25N_YY	I/O, L25N_YY	I/O, L25N_YY
I/O, VREF Bank 1, L#P_YY	1	E16	All	All	I/O, VREF Bank 1, L17P_YY	I/O, VREF Bank 1, L22P_YY	I/O, VREF Bank 1, L24P_YY	I/O, VREF Bank 1, L24P_YY	I/O, VREF Bank 1, L24P_YY	I/O, VREF Bank 1, L24P_YY
I/O, L#N_YY	1	E17	All	-	I/O, L17N_YY	I/O, L22N_YY	I/O, L24N_YY	I/O, L24N_YY	I/O, L24N_YY	I/O, L24N_YY
I/O	1	E15	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P	1	D16	XC2S300E, 600E	-	-	I/O, L21P	I/O, L23P	I/O, L23P_Y	I/O, L23P	I/O, L23P_Y
I/O, L#N	1	C16	XC2S300E, 600E	-	I/O	I/O, L21N	I/O, L23N	I/O, L23N_Y	I/O, L23N	I/O, L23N_Y
I/O, L#P	1	B16	XC2S100E, 300E, 600E	XC2S600E	I/O, L16P_Y	I/O, L20P	I/O, L22P	I/O, L22P_Y	I/O, L22P	I/O, VREF Bank 1, L22P_Y
I/O, L#N	1	A16	XC2S100E, 300E, 600E	-	I/O, L16N_Y	I/O, L20N	I/O, L22N	I/O, L22N_Y	I/O, L22N	I/O, L22N_Y
I/O	1	F14	-	-	-	-	-	I/O	I/O	I/O
I/O, VREF Bank 1, L#P	1	D15	XC2S100E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 1, L15P_Y	I/O, VREF Bank 1, L19P	I/O, VREF Bank 1, L21P_Y	I/O, VREF Bank 1, L21P_Y	I/O, VREF Bank 1, L21P_Y	I/O, VREF Bank 1, L21P_Y
I/O, L#N	1	C15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L15N_Y	I/O, L19N	I/O, L21N_Y	I/O, L21N_Y	I/O, L21N_Y	I/O, L21N_Y
I/O, L#P	1	B15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L14P_Y	I/O, L18P	I/O, L20P_Y	I/O, L20P_Y	I/O, L20P_Y	I/O, L20P_Y

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L51N	2	D24	-	-	-	I/O, L51N
I/O, L51P	2	C25	-	-	-	I/O, L51P
I/O (DIN, D0), L50N_YY	2	C26	All	-	I/O (DIN, D0), L50N_YY	I/O (DIN, D0), L50N_YY
I/O (DOUT, BUSY), L50P_YY	2	B26	All	-	I/O (DOUT, BUSY), L50P_YY	I/O (DOUT, BUSY), L50P_YY
CCLK	2	A25	-	-	CCLK	CCLK
TDO	2	C23	-	-	TDO	TDO
TDI	-	D22	-	-	TDI	TDI
I/O ($\overline{\text{CS}}$), L49P_YY	1	B24	All	-	I/O ($\overline{\text{CS}}$), L49P_YY	I/O ($\overline{\text{CS}}$), L49P_YY
I/O ($\overline{\text{WRITE}}$), L49N_YY	1	A24	All	-	I/O ($\overline{\text{WRITE}}$), L49N_YY	I/O ($\overline{\text{WRITE}}$), L49N_YY
I/O, L48P	1	B23	-	-	I/O	I/O, L48P
I/O, L48N	1	A23	-	-	-	I/O, L48N
I/O, L47P	1	B22	XC2S400E	-	I/O, L47P_Y	I/O, L47P
I/O, L47N	1	A22	XC2S400E	-	I/O, L47N_Y	I/O, L47N
I/O, L46P_YY	1	D21	All	-	I/O, L46P_YY	I/O, L46P_YY
I/O, L46N_YY	1	C21	All	-	I/O, L46N_YY	I/O, L46N_YY
I/O, VREF Bank 1, L45P_YY	1	B21	All	All	I/O, VREF Bank 1, L45P_YY	I/O, VREF Bank 1, L45P_YY
I/O, L45N_YY	1	A21	All	-	I/O, L45N_YY	I/O, L45N_YY
I/O, L44P	1	F20	XC2S600E	-	-	I/O, L44P_Y
I/O, L44N	1	E20	XC2S600E	-	I/O	I/O, L44N_Y
I/O, L43P_YY	1	D20	All	-	I/O, L43P_YY	I/O, L43P_YY
I/O, L43N_YY	1	C20	All	-	I/O, L43N_YY	I/O, L43N_YY
I/O, L42P_YY	1	B20	All	-	I/O, L42P_YY	I/O, L42P_YY
I/O, L42N_YY	1	A20	All	-	I/O, L42N_YY	I/O, L42N_YY
I/O, VREF Bank 1, L41P_YY	1	G19	All	All	I/O, VREF Bank 1, L41P_YY	I/O, VREF Bank 1, L41P_YY
I/O, L41N_YY	1	F19	All	-	I/O, L41N_YY	I/O, L41N_YY
I/O	1	E19	-	-	-	I/O
I/O, L40P_YY	1	B19	All	-	I/O, L40P_YY	I/O, L40P_YY
I/O, L40N_YY	1	A19	All	-	I/O, L40N_YY	I/O, L40N_YY
I/O	1	H18	-	-	I/O	I/O
I/O, L39P	1	G18	XC2S600E	-	I/O, L39P	I/O, L39P_Y