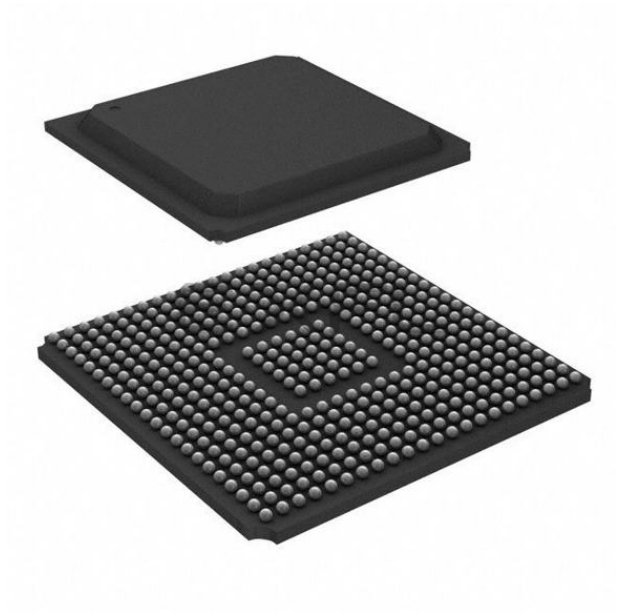

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Details	
Product Status	Obsolete
Number of LABs/CLBs	3456
Number of Logic Elements/Cells	15552
Total RAM Bits	294912
Number of I/O	329
Number of Gates	600000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s600e-6fg456q

Spartan-IIE Product Availability

Table 2 shows the maximum user I/Os available on the device and the number of user I/Os available for each device/package combination.

Table 2: **Spartan-IIE FPGA User I/O Chart**

Device	Maximum User I/O	Available User I/O According to Package Type				
		TQ144 TQG144	PQ208 PQG208	FT256 FTG256	FG456 FGG456	FG676 FGG676
XC2S50E	182	102	146	182	-	-
XC2S100E	202	102	146	182	202	-
XC2S150E	265	-	146	182	265	-
XC2S200E	289	-	146	182	289	-
XC2S300E	329	-	146	182	329	-
XC2S400E	410	-	-	182	329	410
XC2S600E	514	-	-	-	329	514

Notes:
1. User I/O counts include the four global clock/user input pins.

Optional pull-up and pull-down resistors and an optional weak-keeper circuit are attached to each user I/O pad. Prior to configuration all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but inputs may optionally be pulled up. The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins will float. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. After configuration, clamping diodes are connected to V_{CCO} for LVTTL, PCI, HSTL, SSTL, CTT, and AGP standards.

All Spartan-IIE FPGA IOBs support IEEE 1149.1-compatible boundary scan testing.

Input Path

A buffer in the IOB input path routes the input signal directly to internal logic and through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can used in close proximity to each other. See I/O Banking.

There are optional pull-up and pull-down resistors at each input for use after configuration.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. Each output buffer can source up to 24 mA and sink up to 48 mA. Drive strength and slew rate controls minimize bus transients. The default output driver is LVTTL with 12 mA drive strength and slow slew rate.

In most signaling standards, the output high voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See I/O Banking.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way helps eliminate bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signaling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks (see Figure 5). The pinout tables show the bank affiliation of each I/O (see Pinout Tables, page 53). Each bank has multiple V_{CCO} pins which must be connected to the same voltage. Voltage requirements are determined by the output standards in use.

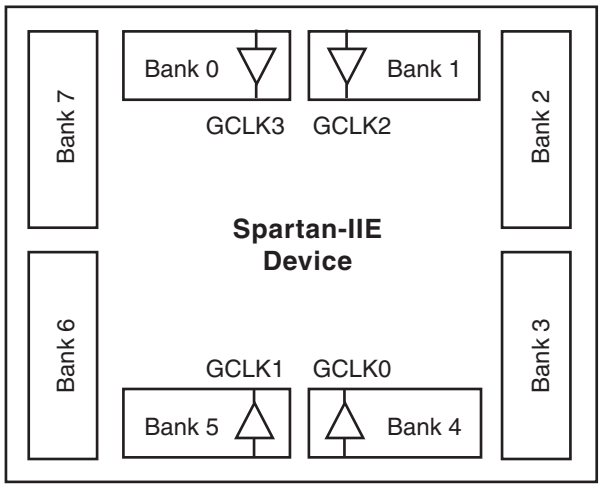


Figure 5: **Spartan-IIE I/O Banks**

In the TQ144 and PQ208 packages, the eight banks have V_{CCO} connected together. Thus, only one V_{CCO} level is allowed in these packages, although different V_{REF} values are allowed in each of the eight banks.

Within a bank, standards may be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 4. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO}. Note that V_{CCO}

Table 11: **Configuration Modes**

Configuration Mode	Preconfiguration Pull-ups	M0	M1	M2	CCLK Direction	Data Width	Serial D_{OUT}
Master Serial mode	No	0	0	0	Out	1	Yes
	Yes	0	0	1			
Slave Parallel mode (SelectMAP)	Yes	0	1	0	In	8	No
	No	0	1	1			
Boundary-Scan mode	Yes	1	0	0	N/A	1	No
	No	1	0	1			
Slave Serial mode	Yes	1	1	0	In	1	Yes
	No	1	1	1			

Notes:
1. During power-on and throughout configuration, the I/O drivers will be in a high-impedance state. After configuration, all unused I/Os (those not assigned signals) will remain in a high-impedance state. Pins used as outputs may pulse High at the end of configuration (see Answer 10504).
2. If the Mode pins are set for preconfiguration pull-ups, those resistors go into effect once the rising edge of INIT samples the Mode pins. They will stay in effect until GTS is released during startup, after which the UnusedPin bitstream generator option will determine whether the unused I/Os have a pull-up, pull-down, or no resistor.

Signals

There are two kinds of pins that are used to configure Spartan-IIE devices: Dedicated pins perform only specific configuration-related functions; the other pins can serve as general purpose I/Os once user operation has begun.

The dedicated pins comprise the mode pins (M2, M1, M0), the configuration clock pin (CCLK), the $\overline{\text{PROGRAM}}$ pin, the DONE pin and the boundary-scan pins (TDI, TDO, TMS, TCK). Depending on the selected configuration mode, CCLK may be an output generated by the FPGA, or may be generated externally, and provided to the FPGA as an input.

Note that some configuration pins can act as outputs. For correct operation, these pins require a V_{CCO} of 3.3V to drive an LVTTL signal or 2.5V to drive an LVCMOS signal. All the relevant pins fall in banks 2 or 3. The $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$ pins for Slave Parallel mode are located in bank 1.

For a more detailed description than that given below, see ***Module 1*** and XAPP176***,*** *Configuration and Readback of the Spartan-II and Spartan-IIE FPGA Families.*

The Process

The sequence of steps necessary to configure Spartan-IIE devices are shown in Figure 16. The overall flow can be divided into three different phases.

- Initiating configuration
- Configuration memory clear
- Loading data frames
- Start-up

The memory clearing and start-up phases are the same for all configuration modes; however, the steps for the loading of data frames are different. Thus, the details for data frame loading are described separately in the sections devoted to each mode.

Initiating Configuration

There are two different ways to initiate the configuration process: applying power to the device or asserting the $\overline{\text{PROGRAM}}$ input.

Configuration on power-up occurs automatically unless it is delayed by the user, as described in a separate section below. The waveform for configuration on power-up is shown in Configuration Switching Characteristics, page 48. Before configuration can begin, V_{CCO} Bank 2 must be greater than 1.0V. Furthermore, all V_{CCINT} power pins must be connected to a 1.8V supply. For more information on delaying configuration, see Clearing Configuration Memory, page 23.

Once in user operation, the device can be re-configured simply by pulling the $\overline{\text{PROGRAM}}$ pin Low. The device acknowledges the beginning of the configuration process by driving DONE Low, then enters the memory-clearing phase.

During start-up, the device performs four operations:

1. The assertion of DONE. The failure of DONE to go High may indicate the unsuccessful loading of configuration data.
2. The release of the Global Three State (GTS). This activates all the I/Os to which signals are assigned. The remaining I/Os stay in a high-impedance state with internal weak pull-up resistors present.
3. The release of the Global Set Reset (GSR). This allows all flip-flops to change state.
4. The assertion of Global Write Enable (GWE). This allows all RAMs and flip-flops to change state.

By default, these operations are synchronized to CCLK. The entire start-up sequence lasts eight cycles, called C0-C7, after which the loaded design is fully functional. The four operations can be selected to switch on any CCLK cycle C1-C6 through settings in the Xilinx Development Software. The default timing for start-up is shown in the top half of Figure 17; heavy lines show default settings.

The default Start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The bottom half of Figure 17 shows another commonly used version of the start-up timing known as Sync-to-DONE. This version makes the GTS, GSR, and GWE events conditional upon the DONE pin going High. This timing is important for a daisy chain of multiple FPGAs in serial mode, since it ensures that all FPGAs go through start-up together, after all their DONE pins have gone High.

Sync-to-DONE timing is selected by setting the GTS, GSR, and GWE cycles to a value of DONE in the configuration options. This causes these signals to transition one clock cycle after DONE externally transitions High.

The sequence can also be paused at any stage until lock has been achieved on any or all DLLs.

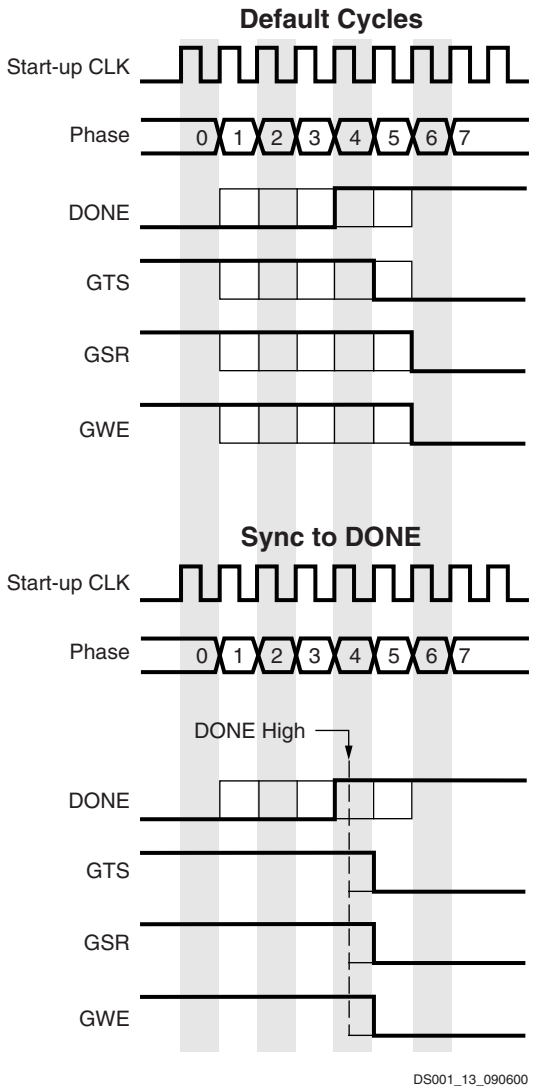


Figure 17: **Start-Up Waveforms**

Serial Modes

There are two serial configuration modes. In Master Serial mode, the FPGA controls the configuration process by driving CCLK as an output. In Slave Serial mode, the FPGA passively receives CCLK as an input from an external agent (e.g., a microprocessor, CPLD, or second FPGA in master mode) that is controlling the configuration process. In both modes, the FPGA is configured by loading one bit per CCLK cycle. The MSB of each configuration data byte is always written to the DIN pin first.

See Figure 18 for the sequence for loading data into the Spartan-IIE FPGA serially. This is an expansion of the "Load Configuration Data Frames" block in Figure 16, page 23. Note that $\overline{CS}$ and $\overline{WRITE}$ are not normally used during serial configuration. To ensure successful loading of the FPGA, do not toggle $\overline{WRITE}$ with $\overline{CS}$ Low during serial configuration.

Master Serial Mode

In Master Serial mode, the CCLK output of the FPGA drives a Xilinx PROM, which feeds a serial stream of configuration data to the FPGA's DIN input. Figure 19 shows a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-IIE device in Master Serial mode should be connected as shown for the device on the left side. Master Serial mode is selected by a <00x> on the mode pins (M0, M1, M2). The PROM RESET pin is driven by $\overline{\text{INIT}}$, and the CE input is driven by DONE. For more information on serial PROMs, see the Xilinx Configuration PROM data sheets at www.xilinx.com.

The interface is identical to the slave serial mode except that an oscillator internal to the FPGA is used to generate the configuration clock (CCLK). Any of a number of different frequencies ranging from 4 to 60 MHz can be set using the ConfigRate option in the Xilinx development software. When selecting a CCLK frequency, ensure that the serial PROM and any daisy-chained FPGAs are fast enough to support the clock rate. On power-up, while the first 60 bytes of the configuration data are being loaded, the CCLK frequency is always 2.5 MHz. This frequency is used until the ConfigRate bits, part of the configuration file, have been loaded into the FPGA, at which point the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz. The frequency of the CCLK signal created by the internal oscillator has a variance of +45%, –30% from the specified value.

The FPGA accepts one bit of configuration data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge. The timing for Master Serial mode is shown in Figure 25, page 49.

Slave Parallel Mode (SelectMAP)

The Slave Parallel mode, also known as SelectMAP, is the fastest configuration option. Byte-wide data is written into the FPGA on the D0-D7 pins. Note that D0 is the MSB of each byte for configuration. A BUSY flag is provided for controlling the flow of data at a clock frequency above 50 MHz.

Figure 20, page 27 shows the connections for two Spartan-IIE devices using the Slave Parallel mode. Slave Parallel mode is selected by a <011> on the mode pins (M0, M1, M2).

The agent controlling configuration is not shown. Typically, a processor, a microcontroller, or CPLD controls the Slave Parallel interface. The controlling agent provides byte-wide configuration data, CCLK, a Chip Select ($\overline{\text{CS}}$) signal and a Write signal ($\overline{\text{WRITE}}$). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

After configuration, the pins of the Slave Parallel port (D0-D7) can be used as additional user I/O. Alternatively, the port may be retained to permit high-speed 8-bit readback. Then data can be read by deasserting $\overline{\text{WRITE}}$. If retention is selected, prohibit the D0-D7 pins from being used as user I/O. See Readback, page 28.

If CCLK is slower than F_{CCNH}, the FPGA will never assert BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

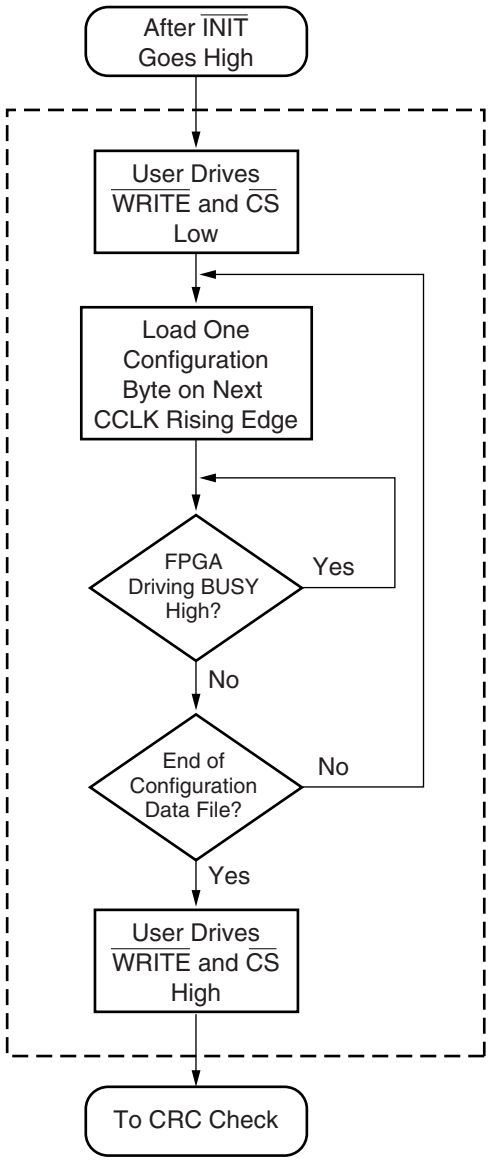


Figure 21: **Loading Configuration Data for the Slave Parallel Mode**

A configuration packet does not have to be written in one continuous stretch, rather it can be split into many write sequences. Each sequence would involve assertion of $\overline{CS}$.

In applications where multiple clock cycles may be required to access the configuration data before each byte can be loaded into the Slave Parallel interface, a new byte of data may not be ready for each consecutive CCLK edge. In such a case the $\overline{CS}$ signal may be deasserted until the next byte is valid on D0-D7. While $\overline{CS}$ is High, the Slave Parallel interface does not expect any data and ignores all CCLK transitions. However, to avoid aborting configuration, $\overline{WRITE}$ must continue to be asserted while $\overline{CS}$ is asserted during CCLK transitions.

Abort

To abort configuration during a write sequence, deassert $\overline{WRITE}$ while holding $\overline{CS}$ Low. The abort operation is initiated at the rising edge of CCLK. The device will remain BUSY until the aborted operation is complete. After aborting configuration, data is assumed to be unaligned to word boundaries and the FPGA requires a new synchronization word prior to accepting any new packets.

Boundary-Scan Configuration Mode

In the boundary-scan mode, no nondedicated pins are required, configuration being done entirely through the IEEE 1149.1 Test Access Port (TAP).

Configuration through the TAP uses the special CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port.

1. Load the CFG_IN instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a standard configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the JSTART instruction into IR
6. Enter the SDR state
7. Clock TCK (if selected) through the startup sequence (the length is programmable)
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode simply locks out the other modes. The boundary-scan mode is selected by a <10x> on the mode pins (M0, M1, M2). Note that the $\overline{PROGRAM}$ pin must be pulled High prior to reconfiguration. A Low on the $\overline{PROGRAM}$ pin resets the TAP controller and no boundary scan operations can be performed. See Xilinx Application Note XAPP188 for more information on boundary-scan configuration.

Readback

The configuration data stored in the Spartan-IIE FPGA configuration memory can be read back for verification. Along with the configuration data it is possible to read back the contents of all flip-flops/latches, LUT RAMs, and block RAMs. This capability is used for real-time debugging.

For more detailed information see Xilinx Application Note XAPP176, *Configuration and Readback of the Spartan-II and Spartan-IIE FPGA Families.*

IOB Input Delay Adjustments for Different Standards

Input delays associated with the pad are specified for LVTTL. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade		Units
			-7	-6	
Data Input Delay Adjustments					
T_{ILVTTL}	Standard-specific data input delay adjustments	LVTTL	0	0	ns
$T_{ILVCMOS2}$		LVCMOS2	0	0	ns
$T_{ILVCMOS18}$		LVCMOS18	0.20	0.20	ns
T_{ILVDS}		LVDS	0.15	0.15	ns
$T_{ILVPECL}$		LVPECL	0.15	0.15	ns
T_{IPCI33_3}		PCI, 33 MHz, 3.3V	0.08	0.08	ns
T_{IPCI66_3}		PCI, 66 MHz, 3.3V	–0.11	–0.11	ns
T_{IGTL}		GTL	0.14	0.14	ns
T_{IGTLP}		GTL+	0.14	0.14	ns
T_{IHSTL}		HSTL	0.04	0.04	ns
T_{ISSTL2}		SSTL2	0.04	0.04	ns
T_{ISSTL3}		SSTL3	0.04	0.04	ns
T_{ICTT}		CTT	0.10	0.10	ns
T_{IAGP}		AGP	0.04	0.04	ns

IOB Output Delay Adjustments for Different Standards(1)

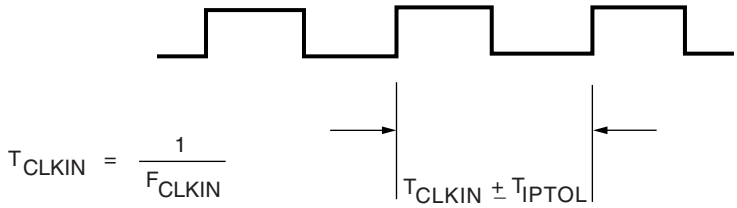
Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade		Units
			-7	-6	
Output Delay Adjustments (Adj)					
T_{OLVTTL_S2}	Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, C_{SL})	LVTTL, Slow, 2 mA	14.7	14.7	ns
T_{OLVTTL_S4}		4 mA	7.5	7.5	ns
T_{OLVTTL_S6}		6 mA	4.8	4.8	ns
T_{OLVTTL_S8}		8 mA	3.0	3.0	ns
T_{OLVTTL_S12}		12 mA	1.9	1.9	ns
T_{OLVTTL_S16}		16 mA	1.7	1.7	ns
T_{OLVTTL_S24}		24 mA	1.3	1.3	ns
T_{OLVTTL_F2}		LVTTL, Fast, 2 mA	13.1	13.1	ns
T_{OLVTTL_F4}		4 mA	5.3	5.3	ns
T_{OLVTTL_F6}		6 mA	3.1	3.1	ns
T_{OLVTTL_F8}		8 mA	1.0	1.0	ns
T_{OLVTTL_F12}		12 mA	0	0	ns
T_{OLVTTL_F16}		16 mA	–0.05	–0.05	ns
T_{OLVTTL_F24}		24 mA	–0.20	–0.20	ns
$T_{OLVCMOS2}$		LVCMOS2	0.09	0.09	ns
$T_{OLVCMOS18}$		LVCMOS18	0.7	0.7	ns
T_{OLVDS}		LVDS	–1.2	–1.2	ns
$T_{OLVPECL}$		LVPECL	–0.41	–0.41	ns
T_{OPCI33_3}		PCI, 33 MHz, 3.3V	2.3	2.3	ns
T_{OPCI66_3}		PCI, 66 MHz, 3.3V	–0.41	–0.41	ns
T_{OGTL}		GTL	0.49	0.49	ns
T_{OGTLP}		GTL+	0.8	0.8	ns
T_{OHSTL_I}		HSTL I	–0.51	–0.51	ns
T_{OHSTL_III}		HSTL III	–0.91	–0.91	ns
T_{OHSTL_IV}		HSTL IV	–1.01	–1.01	ns
T_{OSSTL2_I}		SSTL2 I	–0.51	–0.51	ns
T_{OSSLT2_II}		SSTL2 II	–0.91	–0.91	ns
T_{OSSTL3_I}		SSTL3 I	–0.51	–0.51	ns
T_{OSSTL3_II}		SSTL3 II	–1.01	–1.01	ns
T_{OCTT}		CTT	–0.61	–0.61	ns
T_{OAGP}		AGP	–0.91	–0.91	ns

Notes:

1. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see the tables Constants for Calculating T_{IOOP} and Delay Measurement Methodology, page 41.

Period Tolerance: the allowed input clock period change in nanoseconds.



Output Jitter: the difference between an ideal reference clock edge and the actual design.

Phase Offset and Maximum Phase Difference

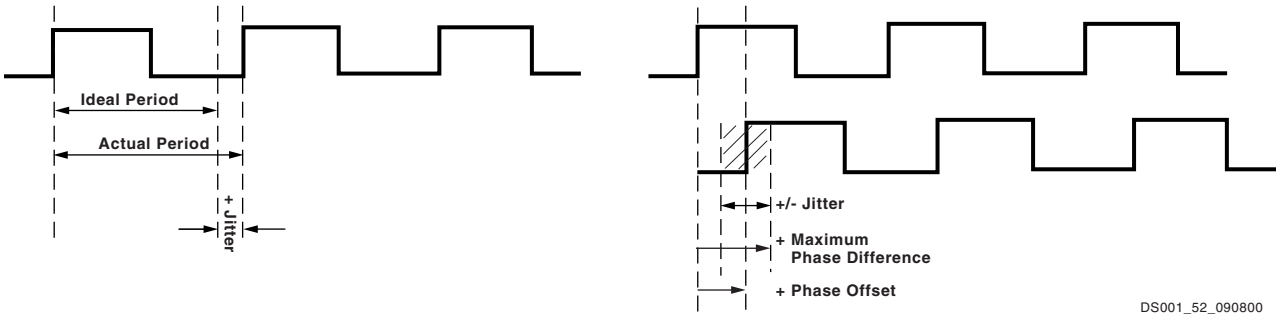
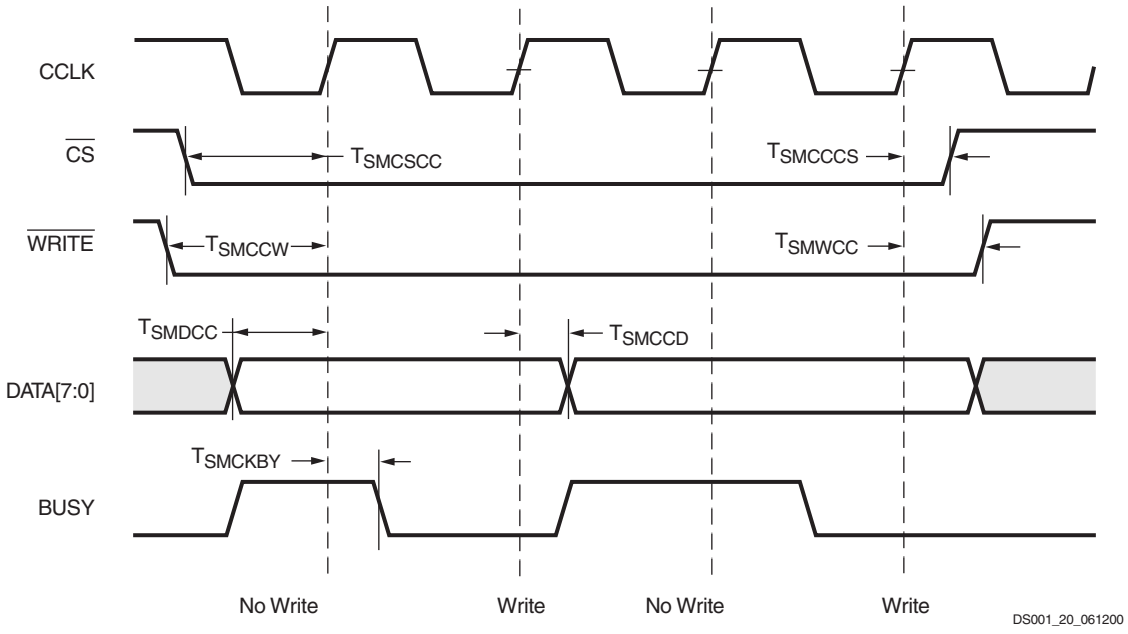


Figure 22: **Period Tolerance and Clock Jitter**

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Combinatorial Delays						
T_{ILO}	4-input function: F/G inputs to X/Y outputs	0.18	0.42	0.18	0.47	ns
T_{IF5}	5-input function: F/G inputs to F5 output	0.3	0.8	0.3	0.9	ns
T_{IF5X}	5-input function: F/G inputs to X output	0.3	0.8	0.3	0.9	ns
T_{IF6Y}	6-input function: F/G inputs to Y output via F6 MUX	0.3	0.9	0.3	1.0	ns
T_{F5INY}	6-input function: F5IN input to Y output	0.04	0.2	0.04	0.22	ns
T_{IFNCTL}	Incremental delay routing through transparent latch to XQ/YQ outputs	-	0.7	-	0.8	ns
T_{BYYB}	BY input to YB output	0.18	0.46	0.18	0.51	ns
Sequential Delays						
T_{CKO}	FF clock CLK to XQ/YQ outputs	0.3	0.9	0.3	1.0	ns
T_{CKLO}	Latch clock CLK to XQ/YQ outputs	0.3	0.9	0.3	1.0	ns
Setup/Hold Times with Respect to Clock CLK						
T_{ICK} / T_{CKI}	4-input function: F/G inputs	1.0 / 0	-	1.1 / 0	-	ns
T_{IF5CK} / T_{CKIF5}	5-input function: F/G inputs	1.4 / 0	-	1.5 / 0	-	ns
T_{F5INCK} / T_{CKF5IN}	6-input function: F5IN input	0.8 / 0	-	0.8 / 0	-	ns
T_{IF6CK} / T_{CKIF6}	6-input function: F/G inputs via F6 MUX	1.5 / 0	-	1.6 / 0	-	ns
T_{DICK} / T_{CKDI}	BX/BY inputs	0.7 / 0	-	0.8 / 0	-	ns
T_{CECK} / T_{CKCE}	CE input	0.7 / 0	-	0.7 / 0	-	ns
T_{RCK} / T_{CKR}	SR/BY inputs (synchronous)	0.52 / 0	-	0.6 / 0	-	ns
Clock CLK						
T_{CH}	Pulse width, High	1.3	-	1.4	-	ns
T_{CL}	Pulse width, Low	1.3	-	1.4	-	ns
Set/Reset						
T_{RPW}	Pulse width, SR/BY inputs	2.1	-	2.4	-	ns
T_{RQ}	Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	0.3	0.9	0.3	1.0	ns
F_{TOG}	Toggle frequency (for export control)	-	400	-	357	MHz



Symbol		Description	All Devices		Units
			Min	Max	
T_{SMDCC} / T_{SMCCD}	CCLK	D0-D7 setup/hold	5 / 1	-	ns
T_{SMCSCC} / T_{SMCCCS}		$\overline{CS}$ setup/hold	7 / 1	-	ns
T_{SMCCW} / T_{SMWCC}		$\overline{WRITE}$ setup/hold	7 / 1	-	ns
T_{SMCKBY}		BUSY propagation delay	-	12	ns
F_{CC}		Frequency	-	66	MHz
F_{CCNH}		Frequency with no handshake	-	50	MHz

Figure 26: **Slave Parallel (SelectMAP) Mode Write Timing**

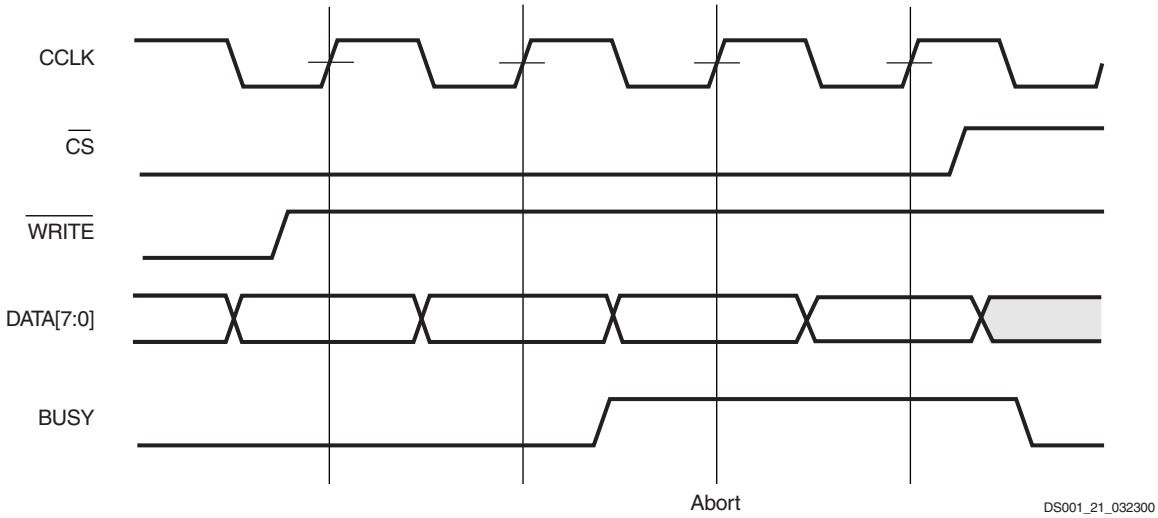


Figure 27: **Slave Parallel (SelectMAP) Mode Write Abort Waveforms**

Spartan-IIE Package Pinouts

The Spartan®-IIE family of FPGAs is available in five popular, low-cost packages, including plastic quad flat packs and fine-pitch ball grid arrays. Family members have footprint compatibility across devices provided in the same package, with minor exceptions due to the smaller number of I/O in smaller devices or due to LVDS/LVPECL pin pairing. The Spartan-IIE family is not footprint compatible with any other FPGA family. The following package-specific pinout tables indicate function, pin, and bank information for all devices available in that package. The pinouts follow the pad locations around the die, starting from pin 1 on the QFP packages.

Table 12: **Spartan-IIE Family Package Options**

Package	Leads	Type	Maximum I/O	Lead Pitch (mm)	Footprint Area (mm)	Height (mm)	Mass[1] (g)
TQ144 / TQG144	144	Thin Quad Flat Pack (TQFP)	102	0.5	22 x 22	1.60	1.4
PQ208 / PQG208	208	Plastic Quad Flat Pack (PQFP)	146	0.5	30.6 x 30.6	3.70	5.3
FT256 / FTG256	256	Fine-pitch Thin Ball Grid Array (FBGA)	182	1.0	17 x 17	1.55	1.0
FG456 / FGG456	456	Fine-pitch Ball Grid Array (FBGA)	329	1.0	23 x 23	2.60	2.2
FG676 / FGG676	676	Fine-pitch Ball Grid Array (FBGA)	514	1.0	27 x 27	2.60	3.1

Notes:

1. Package mass is ±10%.

Package Overview

Table 12 shows the five low-cost, space-saving production package styles for the Spartan-IIE family.

Each package style is available in an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra ‘G’ in the package style name. For example, the standard “TQ144” package becomes “TQG144” when ordered as the Pb-free option. Leaded (non-Pb-free) packages may be available for selected devices, with the same pin-out and without the "G" in the ordering code; contact Xilinx® sales for more information. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 13.

For additional package information, see UG112: *Device Package User Guide*.

Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx web site at the specified location in Table 13.

Material Declaration Data Sheets (MDDS) are also available on the Xilinx web site for each package.

Table 13: **Xilinx Package Documentation**

Package	Drawing	MDDS
TQ144	Package Drawing	PK169_TQ144
TQG144		PK126_TQG144
PQ208	Package Drawing	PK166_PQ208
PQG208		PK123_PQG208
FT256	Package Drawing	PK158_FT256
FTG256		PK115_FTG256
FG456	Package Drawing	PK154_FG456
FGG456		PK109_FGG456
FG676	Package Drawing	PK155_FG676
FGG676		PK111_FGG676

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 6, L39P	6	P45	XC2S100E, 150E	All
I/O, L39N	6	P46	XC2S100E, 150E	-
I/O	6	P47	-	XC2S200E, 300E
I/O, L38P_YY	6	P48	All	-
I/O, L38N_YY	6	P49	All	-
M1	-	P50	-	-
GND	-	P51	-	-
M0	-	P52	-	-
VCCO	-	P53	-	-
M2	-	P54	-	-
I/O, L37N_YY	5	P55	All	-
I/O, L37P_YY	5	P56	All	-
I/O	5	P57	-	XC2S200E, 300E
I/O	5	P58	-	-
I/O, VREF Bank 5, L36N_YY	5	P59	All	All
I/O, L36P_YY	5	P60	All	-
I/O, L35N	5	P61	XC2S50E, 100E, 300E	-
I/O, L35P	5	P62	XC2S50E, 100E, 300E	-
I/O, L34N	5	P63	XC2S50E, 100E, 200E, 300E	XC2S100E, 150E, 200E, 300E
I/O, L34P	5	P64	XC2S50E, 100E, 200E, 300E	-
GND	-	P65	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
VCCO	-	P66	-	-
VCCINT	-	P67	-	-
I/O, L33N	5	P68	XC2S50E, 100E, 200E, 300E	-
I/O, L33P	5	P69	XC2S50E, 100E, 200E, 300E	-
I/O	5	P70	-	-
I/O, L32N	5	P71	XC2S100E, 150E	-
GND	-	P72	-	-
I/O, VREF Bank 5, L32P	5	P73	XC2S100E, 150E	All
I/O	5	P74	-	-
I/O (DLL), L31N	5	P75	-	-
VCCINT	-	P76	-	-
GCK1, I	5	P77	-	-
VCCO	-	P78	-	-
GND	-	P79	-	-
GCK0, I	4	P80	-	-
I/O (DLL), L31P	4	P81	-	-
I/O	4	P82	-	-
I/O, L30N	4	P83	XC2S50E, 200E, 300E	-
I/O, VREF Bank 4, L30P	4	P84	XC2S50E, 200E, 300E	All
GND	-	P85	-	-
I/O, L29N	4	P86	XC2S50E, 200E, 300E	-
I/O, L29P	4	P87	XC2S50E, 200E, 300E	-
I/O, L28N	4	P88	XC2S50E, 100E, 200E, 300E	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L28P	4	P89	XC2S50E, 100E, 200E, 300E	-
VCCINT	-	P90	-	-
VCCO	-	P91	-	-
GND	-	P92	-	-
I/O, L27N	4	P93	XC2S50E, 100E, 200E, 300E	-
I/O, L27P	4	P94	XC2S50E, 100E, 200E, 300E	XC2S100E, 150E, 200E, 300E
I/O	4	P95	-	-
I/O	4	P96	-	-
I/O, L26N_YY	4	P97	All	-
I/O, VREF Bank 4, L26P_YY	4	P98	All	All
I/O	4	P99	-	-
I/O	4	P100	-	XC2S200E, 300E
I/O, L25N_YY	4	P101	All	-
I/O, L25P_YY	4	P102	All	-
GND	-	P103	-	-
DONE	3	P104	-	-
VCCO	-	P105	-	-
$\overline{\text{PROGRAM}}$	-	P106	-	-
I/O ($\overline{\text{INIT}}$), L24N_YY	3	P107	All	-
I/O (D7), L24P_YY	3	P108	All	-
I/O	3	P109	-	XC2S200E, 300E
I/O	3	P110	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 3, L23N	3	P111	XC2S50E, 150E, 200E, 300E	All
I/O, L23P	3	P112	XC2S50E, 150E, 200E, 300E	-
I/O	3	P113	-	-
I/O	3	P114	-	-
I/O, L22N	3	P115	XC2S50E, 300E	XC2S100E, 150E, 200E, 300E
I/O (D6), L22P	3	P116	XC2S50E, 300E	-
GND	-	P117	-	-
VCCO	-	P118	-	-
VCCINT	-	P119	-	-
I/O (D5), L21N_YY	3	P120	All	-
I/O, L21P_YY	3	P121	All	-
I/O, L20N_YY	3	P122	All	-
I/O, L20P_YY	3	P123	All	-
GND	-	P124	-	-
I/O, VREF Bank 3, L19N	3	P125	XC2S50E, 300E	All
I/O (D4), L19P	3	P126	XC2S50E, 300E	-
I/O	3	P127	-	-
VCCINT	-	P128	-	-
I/O (TRDY)	3	P129	-	-
VCCO	-	P130	-	-
GND	-	P131	-	-
I/O (IRDY), L18N_YY	2	P132	All	-
I/O, L18P_YY	2	P133	All	-

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O	7	H5	-	-	-	-	-	I/O	I/O	I/O
I/O, VREF Bank 7, L#P_Y	7	H3	XC2S300E, 400E, 600E	All	I/O, VREF Bank 7, L81P	I/O, VREF Bank 7, L106P	I/O, VREF Bank 7, L113P	I/O, VREF Bank 7, L113P_Y	I/O, VREF Bank 7, L113P_Y	I/O, VREF Bank 7, L113P_Y
I/O, L#N_Y	7	H4	XC2S300E, 400E, 600E	-	I/O, L81N	I/O, L106N	I/O, L113N	I/O, L113N_Y	I/O, L113N_Y	I/O, L113N_Y
I/O, L#P_YY	7	H2	All	-	I/O, L80P_YY	I/O, L105P_YY	I/O, L112P_YY	I/O, L112P_YY	I/O, L112P_YY	I/O, L112P_YY
I/O, L#N_YY	7	H1	All	-	I/O, L80N_YY	I/O, L105N_YY	I/O, L112N_YY	I/O, L112N_YY	I/O, L112N_YY	I/O, L112N_YY
I/O	7	J6	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	J4	XC2S150E, 200E, 300E, 400E	-	-	I/O, L104P_Y	I/O, L111P_Y	I/O, L111P_Y	I/O, L111P_Y	I/O, L111P
I/O, L#N_Y	7	J5	XC2S100E, 150E, 200E, 300E, 400E	-	I/O, L79P_Y	I/O, L104N_Y	I/O, L111N_Y	I/O, L111N_Y	I/O, L111N_Y	I/O, L111N
I/O, L#P_Y	7	J3	XC2S100E, 150E, 200E, 300E, 600E	-	I/O, L79N_Y	I/O, L103P_Y	I/O, L110P_Y	I/O, L110P_Y	I/O, L110P	I/O, L110P_Y
I/O, L#N_Y	7	J2	XC2S150E, 200E, 300E, 600E	-	-	I/O, L103N_Y	I/O, L110N_Y	I/O, L110N_Y	I/O, L110N	I/O, L110N_Y
I/O	7	J1	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#P	7	K5	XC2S100E, 150E, 200E, 300E, 600E[1]	-	I/O, L78P_YY	I/O, L102P_YY	I/O, L109P_YY	I/O, L109P_YY	I/O, L109P	I/O, L109P_Y
I/O, L#N	7	K6	XC2S100E, 150E, 200E, 300E, 600E[1]	-	I/O, L78N_YY	I/O, L102N_YY	I/O, L109N_YY	I/O, L109N_YY	I/O, L109N	I/O, L109N_Y
I/O, VREF Bank 7, L#P_Y	7	K3	XC2S300E, 400E, 600E	All	I/O, VREF Bank 7, L77P	I/O, VREF Bank 7, L101P	I/O, VREF Bank 7, L108P	I/O, VREF Bank 7, L108P_Y	I/O, VREF Bank 7, L108P_Y	I/O, VREF Bank 7, L108P_Y
I/O, L#N_Y	7	K4	XC2S300E, 400E, 600E	-	I/O, L77N	I/O, L101N	I/O, L108N	I/O, L108N_Y	I/O, L108N_Y	I/O, L108N_Y
I/O	7	K2	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P_Y	7	K1	XC2S300E, 400E	-	-	-	I/O, L107P	I/O, L107P_Y	I/O, L107P_Y	I/O, L107P
I/O, L#N_Y	7	L1	XC2S100E, 150E, 300E, 400E	-	I/O, L76P_Y	I/O, L100P_Y	I/O, L107N	I/O, L107N_Y	I/O, L107N_Y	I/O, L107N
I/O, L#P_Y	7	L3	XC2S100E, 150E, 200E, 300E, 600E	XC2S400E, 600E	I/O, L76N_Y	I/O, L100N_Y	I/O, L106P_Y	I/O, L106P_Y	I/O, VREF Bank 7, L106P	I/O, VREF Bank 7, L106P_Y
I/O, L#N_Y	7	L2	XC2S200E, 300E, 600E	-	-	I/O	I/O, L106N_Y	I/O, L106N_Y	I/O, L106N	I/O, L106N_Y
I/O	7	L4	-	-	-	-	-	I/O	I/O	I/O

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O, L#N	4	AA16	XC2S150E, 200E, 400E	XC2S600E	I/O, L46N	I/O, L62N_Y	I/O, L66N_Y	I/O, L66N	I/O, L66N_Y	I/O, VREF Bank 4, L66N
I/O, L#P	4	Y16	XC2S150E, 200E, 400E	-	I/O, L46P	I/O, L62P_Y	I/O, L66P_Y	I/O, L66P	I/O, L66P_Y	I/O, L66P
I/O, L#N	4	W16	XC2S150E, 200E	-	-	I/O, L61N_Y	I/O, L65N_Y	I/O, L65N	I/O, L65N	I/O, L65N
I/O, L#P	4	V16	XC2S150E, 200E	-	-	I/O, L61P_Y	I/O, L65P_Y	I/O, L65P	I/O, L65P	I/O, L65P
I/O, L#N_YY	4	AA17	All	-	I/O, L45N_YY	I/O, L60N_YY	I/O, L64N_YY	I/O, L64N_YY	I/O, L64N_YY	I/O, L64N_YY
I/O, VREF Bank 4, L#P_YY	4	Y17	All	All	I/O, VREF Bank 4, L45P_YY	I/O, VREF Bank 4, L60P_YY	I/O, VREF Bank 4, L64P_YY	I/O, VREF Bank 4, L64P_YY	I/O, VREF Bank 4, L64P_YY	I/O, VREF Bank 4, L64P_YY
I/O	4	AB18	XC2S100E	-	I/O, L44N_Y	I/O	I/O	I/O	I/O	I/O
I/O, L#N	4	W17	XC2S100E, 400E, 600E	-	I/O, L44P_Y	I/O, L59N	I/O, L63N	I/O, L63N	I/O, L63N_Y	I/O, L63N_Y
I/O, L#P	4	V17	XC2S400E, 600E	-	-	I/O, L59P	I/O, L63P	I/O, L63P	I/O, L63P_Y	I/O, L63P_Y
I/O	4	AA18	-	-	-	-	-	I/O	I/O	I/O
I/O, L#N	4	Y18	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L43N_Y	I/O, L58N	I/O, L62N_Y	I/O, L62N_Y	I/O, L62N_Y	I/O, L62N_Y
I/O, L#P	4	W18	XC2S100E, 200E, 300E, 400E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L43P_Y	I/O, L58P	I/O, VREF Bank 4, L62P_Y	I/O, VREF Bank 4, L62P_Y	I/O, VREF Bank 4, L62P_Y	I/O, VREF Bank 4, L62P_Y
I/O	4	AB19	-	-	I/O	I/O	I/O	I/O	I/O	I/O
I/O, L#N	4	AA19	XC2S150E, 400E	-	-	I/O, L57N_Y	I/O, L61N	I/O, L61N	I/O, L61N_Y	I/O, L61N
I/O, L#P	4	Y19	XC2S150E, 400E	-	-	I/O, L57P_Y	I/O, L61P	I/O, L61P	I/O, L61P_Y	I/O, L61P
I/O	4	AB21	-	-	-	-	-	I/O	I/O	I/O
I/O, L#N_YY	4	AB20	All	-	I/O, L42N_YY	I/O, L56N_YY	I/O, L60N_YY	I/O, L60N_YY	I/O, L60N_YY	I/O, L60N_YY
I/O, L#P_YY	4	AA20	All	-	I/O, L42P_YY	I/O, L56P_YY	I/O, L60P_YY	I/O, L60P_YY	I/O, L60P_YY	I/O, L60P_YY
DONE	3	W20	-	-	DONE	DONE	DONE	DONE	DONE	DONE
$\overline{\text{PROGRAM}}$	-	Y21	-	-	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$
I/O ($\overline{\text{INIT}}$), L#N_YY	3	W21	All	-	I/O ($\overline{\text{INIT}}$), L41N_YY	I/O ($\overline{\text{INIT}}$), L55N_YY	I/O ($\overline{\text{INIT}}$), L59N_YY	I/O ($\overline{\text{INIT}}$), L59N_YY	I/O ($\overline{\text{INIT}}$), L59N_YY	I/O ($\overline{\text{INIT}}$), L59N_YY
I/O (D7), L#P_YY	3	Y22	All	-	I/O (D7), L41P_YY	I/O (D7), L55P_YY	I/O (D7), L59P_YY	I/O (D7), L59P_YY	I/O (D7), L59P_YY	I/O (D7), L59P_YY
I/O	3	W22	-	-	-	-	-	I/O	I/O	I/O
I/O	3	V21	-	-	-	I/O	I/O	I/O	I/O	I/O

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O (WRITE), L#N_YY	1	A20	All	-	I/O (WRITE), L20N_YY	I/O (WRITE), L26N_YY	I/O (WRITE), L28N_YY	I/O (WRITE), L28N_YY	I/O (WRITE), L28N_YY	I/O (WRITE), L28N_YY
I/O	1	D18	-	-	-	-	-	I/O	I/O	I/O
I/O	1	C18	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P	1	B19	XC2S200E, 300E, 400E, 600E	-	-	I/O, L25P	I/O, L27P_Y	I/O, L27P_Y	I/O, L27P_Y	I/O, L27P_Y
I/O, L#N	1	A19	XC2S200E, 300E, 400E, 600E	-	I/O	I/O, L25N	I/O, L27N_Y	I/O, L27N_Y	I/O, L27N_Y	I/O, L27N_Y
I/O, L#P	1	B18	XC2S100E, 200E, 300E, 400E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L19P_Y	I/O, L24P	I/O, VREF Bank 1, L26P_Y	I/O, VREF Bank 1, L26P_Y	I/O, VREF Bank 1, L26P_Y	I/O, VREF Bank 1, L26P_Y
I/O, L#N	1	A18	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L19N_Y	I/O, L24N	I/O, L26N_Y	I/O, L26N_Y	I/O, L26N_Y	I/O, L26N_Y
I/O	1	D17	-	-	-	-	-	I/O	I/O	I/O
I/O	1	C17	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P_YY	1	B17	All	-	I/O, L18P_YY	I/O, L23P_YY	I/O, L25P_YY	I/O, L25P_YY	I/O, L25P_YY	I/O, L25P_YY
I/O, L#N_YY	1	A17	All	-	I/O, L18N_YY	I/O, L23N_YY	I/O, L25N_YY	I/O, L25N_YY	I/O, L25N_YY	I/O, L25N_YY
I/O, VREF Bank 1, L#P_YY	1	E16	All	All	I/O, VREF Bank 1, L17P_YY	I/O, VREF Bank 1, L22P_YY	I/O, VREF Bank 1, L24P_YY	I/O, VREF Bank 1, L24P_YY	I/O, VREF Bank 1, L24P_YY	I/O, VREF Bank 1, L24P_YY
I/O, L#N_YY	1	E17	All	-	I/O, L17N_YY	I/O, L22N_YY	I/O, L24N_YY	I/O, L24N_YY	I/O, L24N_YY	I/O, L24N_YY
I/O	1	E15	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P	1	D16	XC2S300E, 600E	-	-	I/O, L21P	I/O, L23P	I/O, L23P_Y	I/O, L23P	I/O, L23P_Y
I/O, L#N	1	C16	XC2S300E, 600E	-	I/O	I/O, L21N	I/O, L23N	I/O, L23N_Y	I/O, L23N	I/O, L23N_Y
I/O, L#P	1	B16	XC2S100E, 300E, 600E	XC2S600E	I/O, L16P_Y	I/O, L20P	I/O, L22P	I/O, L22P_Y	I/O, L22P	I/O, VREF Bank 1, L22P_Y
I/O, L#N	1	A16	XC2S100E, 300E, 600E	-	I/O, L16N_Y	I/O, L20N	I/O, L22N	I/O, L22N_Y	I/O, L22N	I/O, L22N_Y
I/O	1	F14	-	-	-	-	-	I/O	I/O	I/O
I/O, VREF Bank 1, L#P	1	D15	XC2S100E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 1, L15P_Y	I/O, VREF Bank 1, L19P	I/O, VREF Bank 1, L21P_Y	I/O, VREF Bank 1, L21P_Y	I/O, VREF Bank 1, L21P_Y	I/O, VREF Bank 1, L21P_Y
I/O, L#N	1	C15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L15N_Y	I/O, L19N	I/O, L21N_Y	I/O, L21N_Y	I/O, L21N_Y	I/O, L21N_Y
I/O, L#P	1	B15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L14P_Y	I/O, L18P	I/O, L20P_Y	I/O, L20P_Y	I/O, L20P_Y	I/O, L20P_Y

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
GCK0, I	4	AF14	-	-	GCK0, I	GCK0, I
I/O (DLL), L126P	4	AE14	-	-	I/O (DLL), L126P	I/O (DLL), L126P
I/O	4	AD14	-	-	-	I/O
I/O, L125N	4	AC14	-	-	I/O, L125N	I/O, L125N
I/O, L125P	4	AB14	-	-	I/O, L125P	I/O, L125P
I/O	4	AC15	-	-	-	I/O
I/O, L124N	4	AA14	XC2S600E	-	I/O, L124N	I/O, L124N_Y
I/O, VREF Bank 4, L124P	4	Y14	XC2S600E	All	I/O, VREF Bank 4, L124P	I/O, VREF Bank 4, L124P_Y
I/O, L123N	4	AF15	XC2S600E	-	I/O, L123N	I/O, L123N_Y
I/O, L123P	4	AE15	XC2S600E	-	I/O, L123P	I/O, L123P_Y
I/O	4	AB15	-	-	-	I/O
I/O, L122N_YY	4	AA15	All	-	I/O, L122N_YY	I/O, L122N_YY
I/O, L122P_YY	4	Y15	All	-	I/O, L122P_YY	I/O, L122P_YY
I/O	4	AF16	-	-	-	I/O
I/O, L121N_YY	4	W15	All	-	I/O, L121N_YY	I/O, L121N_YY
I/O, VREF Bank 4, L121P_YY	4	V15	All	All	I/O, VREF Bank 4, L121P_YY	I/O, VREF Bank 4, L121P_YY
I/O, L120N_YY	4	AE16	All	-	I/O, L120N_YY	I/O, L120N_YY
I/O, L120P_YY	4	AD16	All	-	I/O, L120P_YY	I/O, L120P_YY
I/O	4	AB16	-	-	-	I/O
I/O, L119N	4	AA16	-	-	I/O, L119N	I/O, L119N
I/O, L119P	4	Y16	-	-	I/O, L119P	I/O, L119P
I/O	4	W16	-	-	-	I/O
I/O, L118N_YY	4	AF17	All	-	I/O, L118N_YY	I/O, L118N_YY
I/O, L118P_YY	4	AE17	All	-	I/O, L118P_YY	I/O, L118P_YY
I/O, L117N_YY	4	AD17	All	-	I/O, L117N_YY	I/O, L117N_YY
I/O, L117P_YY	4	AC17	All	-	I/O, L117P_YY	I/O, L117P_YY
I/O	4	AB17	-	-	-	I/O
I/O, L116N	4	Y17	XC2S600E	-	I/O, L116N	I/O, L116N_Y
I/O, L116P	4	W17	XC2S600E	-	I/O, L116P	I/O, L116P_Y
I/O	4	AF18	-	-	-	I/O
I/O, L115N_YY	4	AE18	All	-	I/O, L115N_YY	I/O, L115N_YY
I/O, L115P_YY	4	AD18	All	-	I/O, L115P_YY	I/O, L115P_YY

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O	4	AC18	-	-	I/O	I/O
I/O, VREF Bank 4, L114N	4	AB18	-	All	I/O, VREF Bank 4, L114N	I/O, VREF Bank 4, L114N
I/O, L114P	4	AA18	-	-	I/O, L114P	I/O, L114P
I/O, L113N	4	Y18	-	-	I/O, L113N	I/O, L113N
I/O, L113P	4	W18	-	-	I/O, L113P	I/O, L113P
I/O	4	AB19	-	-	I/O	I/O
I/O, L112N	4	AF19	XC2S600E	-	I/O	I/O, L112N_Y
I/O, L112P	4	AE19	XC2S600E	XC2S600E	-	I/O, VREF Bank 4, L112P_Y
I/O, L111N	4	AA19	XC2S600E	-	I/O, L111N	I/O, L111N_Y
I/O, L111P	4	Y19	XC2S600E	-	I/O, L111P	I/O, L111P_Y
I/O	4	AF20	-	-	-	I/O
I/O, L110N	4	AE20	XC2S600E	-	I/O, L110N	I/O, L110N_Y
I/O, L110P	4	AD20	XC2S600E	-	I/O, L110P	I/O, L110P_Y
I/O	4	AC20	-	-	I/O	I/O
I/O, L109N_YY	4	AB20	All	-	I/O, L109N_YY	I/O, L109N_YY
I/O, VREF Bank 4, L109P_YY	4	AA20	All	All	I/O, VREF Bank 4, L109P_YY	I/O, VREF Bank 4, L109P_YY
I/O	4	Y20	-	-	I/O	I/O
I/O, L108N	4	AF21	-	-	I/O, L108N	I/O, L108N
I/O, L108P	4	AE21	-	-	I/O, L108P	I/O, L108P
I/O, L107N	4	AD21	-	-	I/O, L107N	I/O, L107N
I/O, L107P	4	AC21	-	-	I/O, L107P	I/O, L107P
I/O	4	AC22	-	-	-	I/O
I/O, L106N_YY	4	AF22	All	-	I/O, L106N_YY	I/O, L106N_YY
I/O, VREF Bank 4, L106P_YY	4	AE22	All	All	I/O, VREF Bank 4, L106P_YY	I/O, VREF Bank 4, L106P_YY
I/O, L105N_YY	4	AB21	All	-	I/O, L105N_YY	I/O, L105N_YY
I/O, L105P_YY	4	AA21	All	-	I/O, L105P_YY	I/O, L105P_YY
I/O, L104N_YY	4	AF23	All	-	I/O, L104N_YY	I/O, L104N_YY
I/O, L104P_YY	4	AE23	All	-	I/O, L104P_YY	I/O, L104P_YY
I/O, L103N	4	AD23	XC2S600E	-	I/O	I/O, L103N_Y
I/O, L103P	4	AE24	XC2S600E	-	-	I/O, L103P_Y
I/O, L102N_YY	4	AF24	All	-	I/O, L102N_YY	I/O, L102N_YY
I/O, L102P_YY	4	AF25	All	-	I/O, L102P_YY	I/O, L102P_YY

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L2N_YY	0	E5	All	-	I/O, L2N_YY	I/O, L2N_YY
I/O, L1P_YY	0	B4	All	-	I/O, L1P_YY	I/O, L1P_YY
I/O, L1N_YY	0	C4	All	-	I/O, L1N_YY	I/O, L1N_YY
I/O, L0P	0	A3	XC2S600E	-	I/O	I/O, L0P_Y
I/O, L0N	0	B3	XC2S600E	-	-	I/O, L0N_Y
I/O	0	A4	-	-	I/O	I/O
TCK	-	A2	-	-	TCK	TCK

FG676 Differential Clock Pins

Clock	Bank	P Input		N Input	
		Pin	Name	Pin	Name
GCK0	4	AF14	GCK0, I	AE14	I/O (DLL), L126P
GCK1	5	AF13	GCK1, I	AE13	I/O (DLL), L126N
GCK2	1	A14	GCK2, I	B14	I/O (DLL), L23P
GCK3	0	A13	GCK3, I	B13	I/O (DLL), L23N

Additional FG676 Package Pins

VCCINT Pins						
H8	H19	J9	J18	K10	K11	K16
K17	L10	L17	T10	T17	U10	U11
U16	U17	V9	V18	W8	W19	-
VCCO Bank 0 Pins						
C5	C8	D11	J10	J11	K12	K13
VCCO Bank 1 Pins						
C19	C22	D16	J16	J17	K14	K15
VCCO Bank 2 Pins						
E24	H24	K18	L18	L23	M17	N17
VCCO Bank 3 Pins						
P17	R17	T18	T23	U18	W24	AB24
VCCO Bank 4 Pins						
U14	U15	V16	V17	AC16	AD19	AD22
VCCO Bank 5 Pins						
U12	U13	V10	V11	AC11	AD5	AD8
VCCO Bank 6 Pins						
P10	R10	T4	T9	U9	W3	AB3
VCCO Bank 7 Pins						
H3	K9	L4	L9	M10	N10	E3