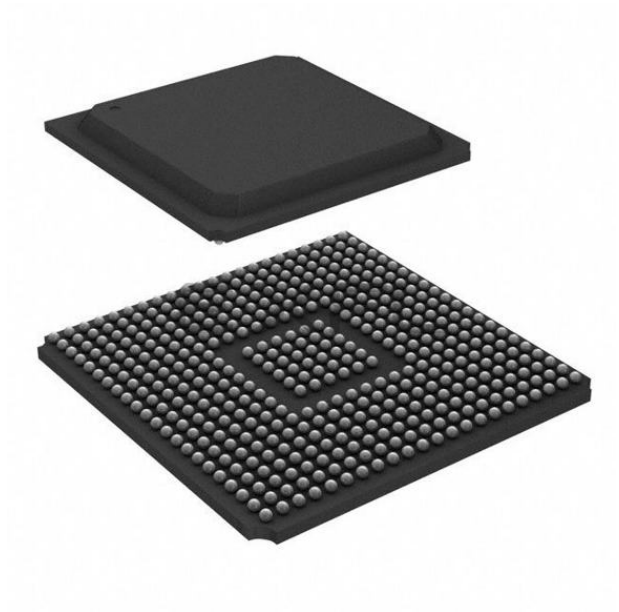
AMD Xilinx - XC2S600E-6FGG456C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3456
Number of Logic Elements/Cells	15552
Total RAM Bits	294912
Number of I/O	329
Number of Gates	600000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s600e-6fgg456c

General Overview

The Spartan-IIE family of FPGAs have a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), surrounded by a perimeter of programmable Input/Output Blocks (IOBs). There are four Delay-Locked Loops (DLLs), one at each corner of the die. Two columns of block RAM lie on opposite sides of the die, between the CLBs and the IOB columns. The XC2S400E has four columns and the XC2S600E has six columns of block RAM. These functional elements are interconnected by a powerful hierarchy of versatile routing channels (see Figure 1).

Spartan-IIE FPGAs are customized by loading configuration data into internal static memory cells. Unlimited reprogramming cycles are possible with this approach. Stored values in these cells determine logic functions and interconnections implemented in the FPGA. Configuration data can be read from an external serial PROM (master serial mode), or written into the FPGA in slave serial, slave parallel, or Boundary Scan modes. Xilinx offers multiple types of low-cost configuration solutions including the Platform Flash in-system programmable configuration PROMs.

Spartan-IIE FPGAs are typically used in high-volume applications where the versatility of a fast programmable solution adds benefits. Spartan-IIE FPGAs are ideal for shortening product development cycles while offering a cost-effective solution for high volume production.

Spartan-IIE FPGAs achieve high-performance, low-cost operation through advanced architecture and semiconductor technology. Spartan-IIE devices provide system clock rates beyond 200 MHz. In addition to the conventional benefits of high-volume programmable logic solutions, Spartan-IIE FPGAs also offer on-chip synchronous single-port and dual-port RAM (block and distributed form), DLL clock drivers, programmable set and reset on all flip-flops, fast carry logic, and many other features.

Spartan-IIE Family Compared to Spartan-II Family

- Higher density and more I/O
- Higher performance
- Unique pinouts in cost-effective packages
- Differential signaling
  - LVDS, Bus LVDS, LVPECL
- V_{CCINT} = 1.8V
  - Lower power
  - 5V tolerance with external resistor
  - 3V tolerance directly
- PCI, LVTTL, and LVCMOS2 input buffers powered by V_{CCO} instead of V_{CCINT}
- Unique larger bitstream

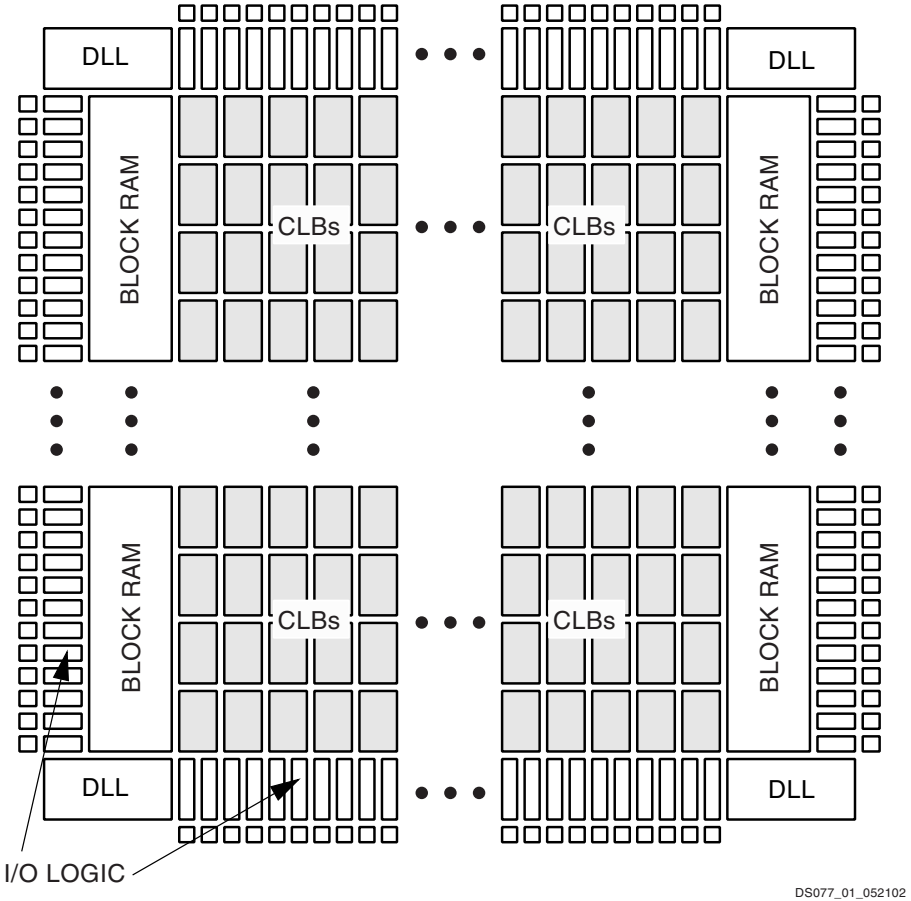

Figure 1: **Basic Spartan-IIE Family FPGA Block Diagram**

Optional pull-up and pull-down resistors and an optional weak-keeper circuit are attached to each user I/O pad. Prior to configuration all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but inputs may optionally be pulled up. The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins will float. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. After configuration, clamping diodes are connected to V_{CCO} for LVTTL, PCI, HSTL, SSTL, CTT, and AGP standards.

All Spartan-IIE FPGA IOBs support IEEE 1149.1-compatible boundary scan testing.

Input Path

A buffer in the IOB input path routes the input signal directly to internal logic and through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can used in close proximity to each other. See I/O Banking.

There are optional pull-up and pull-down resistors at each input for use after configuration.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. Each output buffer can source up to 24 mA and sink up to 48 mA. Drive strength and slew rate controls minimize bus transients. The default output driver is LVTTL with 12 mA drive strength and slow slew rate.

In most signaling standards, the output high voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See I/O Banking.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way helps eliminate bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signaling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks (see Figure 5). The pinout tables show the bank affiliation of each I/O (see Pinout Tables, page 53). Each bank has multiple V_{CCO} pins which must be connected to the same voltage. Voltage requirements are determined by the output standards in use.

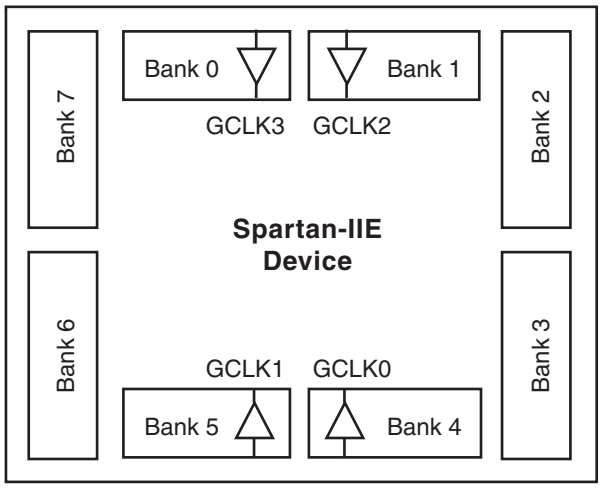

Figure 5: **Spartan-IIE I/O Banks**

In the TQ144 and PQ208 packages, the eight banks have V_{CCO} connected together. Thus, only one V_{CCO} level is allowed in these packages, although different V_{REF} values are allowed in each of the eight banks.

Within a bank, standards may be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 4. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO}. Note that V_{CCO}

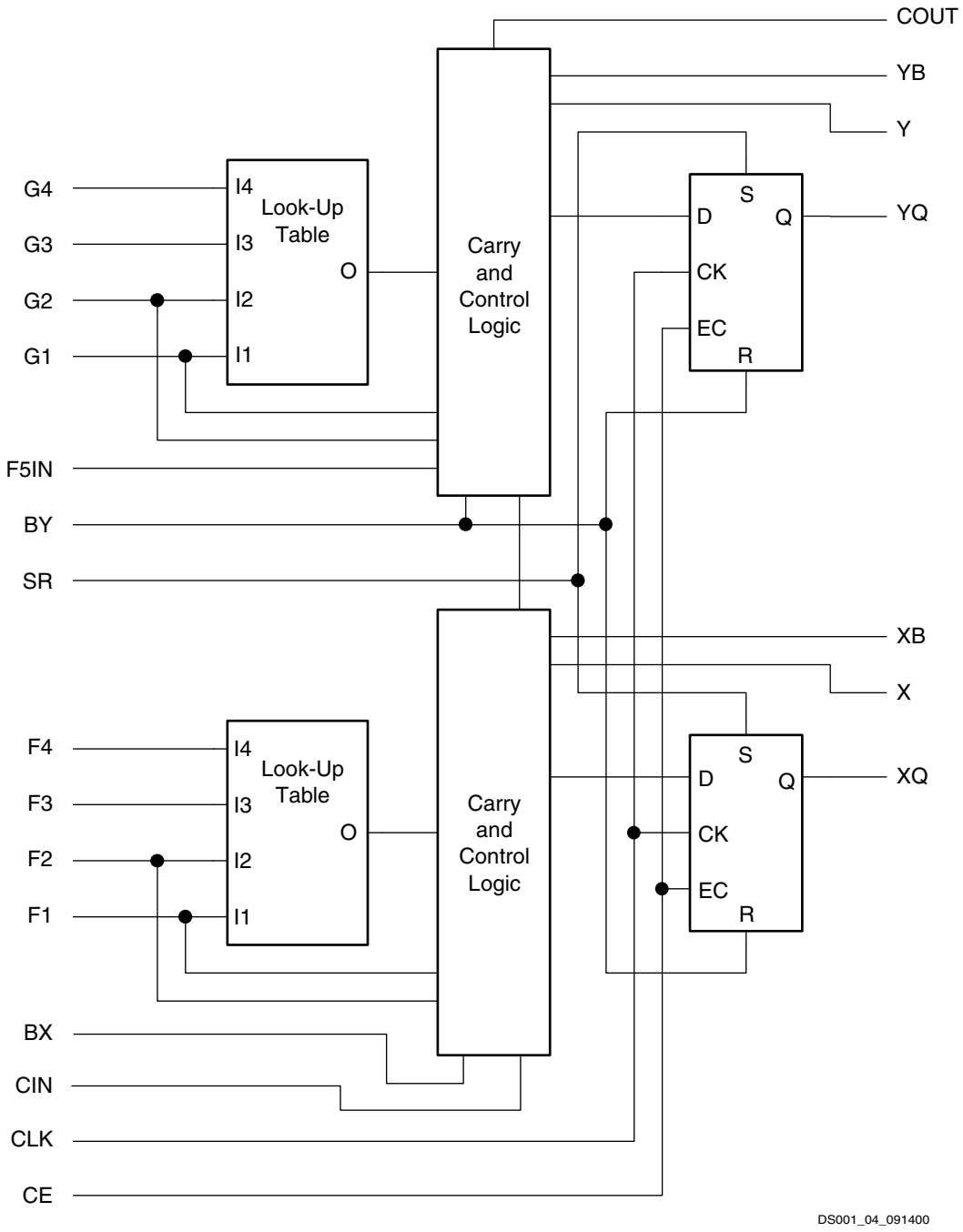

Figure 6: **Spartan-IIE CLB Slice** (two identical slices in each CLB)

Additional Logic

The F5 multiplexer in each slice combines the function generator outputs (Figure 7). This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the two F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Dedicated Routing

Some classes of signal require dedicated routing resources to maximize performance. In the Spartan-IIE FPGA architecture, dedicated routing resources are provided for two classes of signal.

- Horizontal routing resources are provided for on-chip 3-state busses. Four partitionable bus lines are provided per CLB row, permitting multiple busses within a row, as shown in Figure 10.
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.

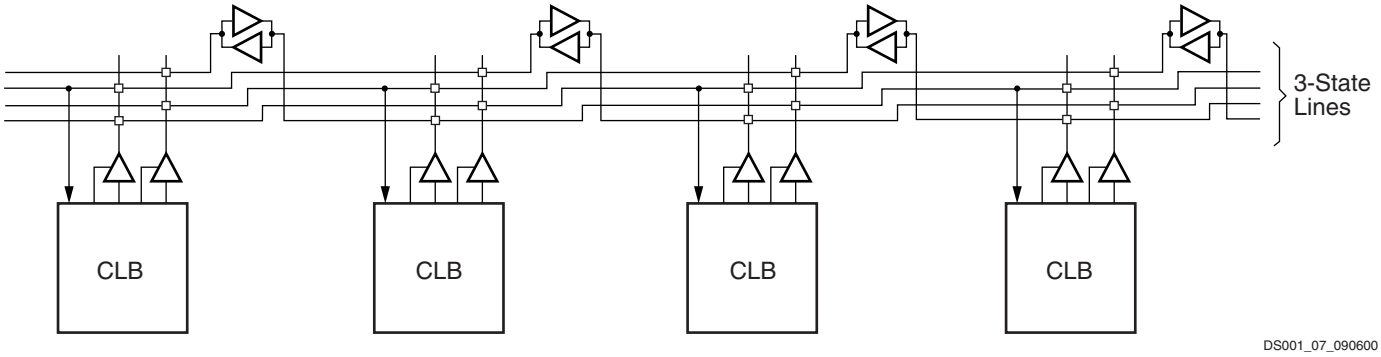

Figure 10: **BUFT Connections to Dedicated Horizontal Bus Lines**

Global Routing

Global Routing resources distribute clocks and other signals with very high fanout throughout the device. Spartan-IIE devices include two tiers of global routing resources referred to as primary and secondary global routing resources.

- The primary global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The primary global nets may only be driven by global buffers. There are four global buffers, one for each global net.
- The secondary global routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across the bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These secondary resources are more flexible than the primary resources since they are not restricted to routing only to clock pins.

Clock Distribution

The Spartan-IIE family provides high-speed, low-skew clock distribution through the primary global routing resources described above. A typical clock distribution net is shown in Figure 11.

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four primary global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing.

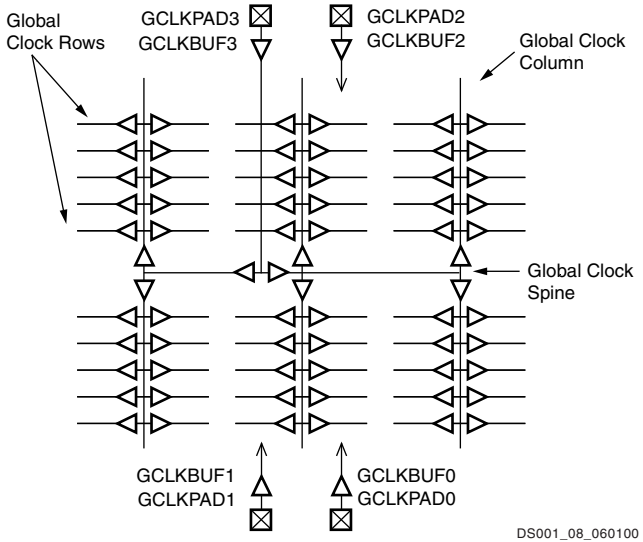

Figure 11: **Global Clock Distribution Network**

Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element (Figure 12). Additional delay is introduced such that clock edges reach internal flip-flops exactly one clock period after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock

Table 11: **Configuration Modes**

Configuration Mode	Preconfiguration Pull-ups	M0	M1	M2	CCLK Direction	Data Width	Serial D_{OUT}
Master Serial mode	No	0	0	0	Out	1	Yes
	Yes	0	0	1			
Slave Parallel mode (SelectMAP)	Yes	0	1	0	In	8	No
	No	0	1	1			
Boundary-Scan mode	Yes	1	0	0	N/A	1	No
	No	1	0	1			
Slave Serial mode	Yes	1	1	0	In	1	Yes
	No	1	1	1			

Notes:
1. During power-on and throughout configuration, the I/O drivers will be in a high-impedance state. After configuration, all unused I/Os (those not assigned signals) will remain in a high-impedance state. Pins used as outputs may pulse High at the end of configuration (see Answer 10504).
2. If the Mode pins are set for preconfiguration pull-ups, those resistors go into effect once the rising edge of INIT samples the Mode pins. They will stay in effect until GTS is released during startup, after which the UnusedPin bitstream generator option will determine whether the unused I/Os have a pull-up, pull-down, or no resistor.

Signals

There are two kinds of pins that are used to configure Spartan-IIE devices: Dedicated pins perform only specific configuration-related functions; the other pins can serve as general purpose I/Os once user operation has begun.

The dedicated pins comprise the mode pins (M2, M1, M0), the configuration clock pin (CCLK), the $\overline{\text{PROGRAM}}$ pin, the DONE pin and the boundary-scan pins (TDI, TDO, TMS, TCK). Depending on the selected configuration mode, CCLK may be an output generated by the FPGA, or may be generated externally, and provided to the FPGA as an input.

Note that some configuration pins can act as outputs. For correct operation, these pins require a V_{CCO} of 3.3V to drive an LVTTL signal or 2.5V to drive an LVCMOS signal. All the relevant pins fall in banks 2 or 3. The $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$ pins for Slave Parallel mode are located in bank 1.

For a more detailed description than that given below, see ***Module 1*** and XAPP176***,*** *Configuration and Readback of the Spartan-II and Spartan-IIE FPGA Families.*

The Process

The sequence of steps necessary to configure Spartan-IIE devices are shown in Figure 16. The overall flow can be divided into three different phases.

- Initiating configuration
- Configuration memory clear
- Loading data frames
- Start-up

The memory clearing and start-up phases are the same for all configuration modes; however, the steps for the loading of data frames are different. Thus, the details for data frame loading are described separately in the sections devoted to each mode.

Initiating Configuration

There are two different ways to initiate the configuration process: applying power to the device or asserting the $\overline{\text{PROGRAM}}$ input.

Configuration on power-up occurs automatically unless it is delayed by the user, as described in a separate section below. The waveform for configuration on power-up is shown in Configuration Switching Characteristics, page 48. Before configuration can begin, V_{CCO} Bank 2 must be greater than 1.0V. Furthermore, all V_{CCINT} power pins must be connected to a 1.8V supply. For more information on delaying configuration, see Clearing Configuration Memory, page 23.

Once in user operation, the device can be re-configured simply by pulling the $\overline{\text{PROGRAM}}$ pin Low. The device acknowledges the beginning of the configuration process by driving DONE Low, then enters the memory-clearing phase.

IOB Input Switching Characteristics(1)

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in IOB Input Delay Adjustments for Different Standards, page 38.

Symbol	Description	Device	Speed Grade				Units
			-7		-6		
			Min	Max	Min	Max	
Propagation Delays							
T_{IOPI}	Pad to I output, no delay	All	0.4	0.8	0.4	0.8	ns
T_{IOPID}	Pad to I output, with delay	All	0.5	1.0	0.5	1.0	ns
T_{IOPLI}	Pad to output IQ via transparent latch, no delay	All	0.7	1.5	0.7	1.6	ns
T_{IOPLID}	Pad to output IQ via transparent latch, with delay	XC2S50E	1.3	3.0	1.3	3.1	ns
		XC2S100E	1.3	3.0	1.3	3.1	ns
		XC2S150E	1.3	3.2	1.3	3.3	ns
		XC2S200E	1.3	3.2	1.3	3.3	ns
		XC2S300E	1.3	3.2	1.3	3.3	ns
		XC2S400E	1.4	3.2	1.4	3.4	ns
		XC2S600E	1.5	3.5	1.5	3.7	ns
Sequential Delays							
T_{IOCKIQ}	Clock CLK to output IQ	All	0.1	0.7	0.1	0.7	ns
Setup/Hold Times with Respect to Clock CLK							
T_{IOPICK} / T_{IOICKP}	Pad, no delay	All	1.4 / 0	-	1.5 / 0	-	ns
$T_{IOPICKD}$ / $T_{IOICKPD}$	Pad, with delay	XC2S50E	2.9 / 0	-	2.9 / 0	-	ns
		XC2S100E	2.9 / 0	-	2.9 / 0	-	ns
		XC2S150E	3.1 / 0	-	3.1 / 0	-	ns
		XC2S200E	3.1 / 0	-	3.1 / 0	-	ns
		XC2S300E	3.1 / 0	-	3.1 / 0	-	ns
		XC2S400E	3.2 / 0	-	3.2 / 0	-	ns
		XC2S600E	3.5 / 0	-	3.5 / 0	-	ns
$T_{IOICECK}$ / $T_{IOCKICE}$	ICE input	All	0.7 / 0.01	-	0.7 / 0.01	-	ns
Set/Reset Delays							
$T_{IOSRCKI}$	SR input (IFF, synchronous)	All	0.9	-	1.0	-	ns
T_{IOSRIQ}	SR input to IQ (asynchronous)	All	0.5	1.2	0.5	1.4	ns
T_{GSRQ}	GSR to output IQ	All	3.8	8.5	3.8	9.7	ns

Notes:
1. Input timing for LVTTL is measured at 1.4V. For other I/O standards, see the table Delay Measurement Methodology, page 41.

IOB Output Delay Adjustments for Different Standards(1)

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade		Units
			-7	-6	
Output Delay Adjustments (Adj)					
T_{OLVTTL_S2}	Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, C_{SL})	LVTTL, Slow, 2 mA	14.7	14.7	ns
T_{OLVTTL_S4}		4 mA	7.5	7.5	ns
T_{OLVTTL_S6}		6 mA	4.8	4.8	ns
T_{OLVTTL_S8}		8 mA	3.0	3.0	ns
T_{OLVTTL_S12}		12 mA	1.9	1.9	ns
T_{OLVTTL_S16}		16 mA	1.7	1.7	ns
T_{OLVTTL_S24}		24 mA	1.3	1.3	ns
T_{OLVTTL_F2}		LVTTL, Fast, 2 mA	13.1	13.1	ns
T_{OLVTTL_F4}		4 mA	5.3	5.3	ns
T_{OLVTTL_F6}		6 mA	3.1	3.1	ns
T_{OLVTTL_F8}		8 mA	1.0	1.0	ns
T_{OLVTTL_F12}		12 mA	0	0	ns
T_{OLVTTL_F16}		16 mA	–0.05	–0.05	ns
T_{OLVTTL_F24}		24 mA	–0.20	–0.20	ns
$T_{OLVCMOS2}$		LVCMOS2	0.09	0.09	ns
$T_{OLVCMOS18}$		LVCMOS18	0.7	0.7	ns
T_{OLVDS}		LVDS	–1.2	–1.2	ns
$T_{OLVPECL}$		LVPECL	–0.41	–0.41	ns
T_{OPCI33_3}		PCI, 33 MHz, 3.3V	2.3	2.3	ns
T_{OPCI66_3}		PCI, 66 MHz, 3.3V	–0.41	–0.41	ns
T_{OGTL}		GTL	0.49	0.49	ns
T_{OGTLP}		GTL+	0.8	0.8	ns
T_{OHSTL_I}		HSTL I	–0.51	–0.51	ns
T_{OHSTL_III}		HSTL III	–0.91	–0.91	ns
T_{OHSTL_IV}		HSTL IV	–1.01	–1.01	ns
T_{OSSTL2_I}		SSTL2 I	–0.51	–0.51	ns
T_{OSSLT2_II}		SSTL2 II	–0.91	–0.91	ns
T_{OSSTL3_I}		SSTL3 I	–0.51	–0.51	ns
T_{OSSTL3_II}		SSTL3 II	–1.01	–1.01	ns
T_{OCTT}		CTT	–0.61	–0.61	ns
T_{OAGP}		AGP	–0.91	–0.91	ns

Notes:

1. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see the tables Constants for Calculating T_{IOOP} and Delay Measurement Methodology, page 41.

CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Combinatorial Delays						
T_{OPX}	F operand inputs to X via XOR	-	0.8	-	0.8	ns
T_{OPXB}	F operand input to XB output	-	0.8	-	0.9	ns
T_{OPY}	F operand input to Y via XOR	-	1.4	-	1.5	ns
T_{OPYB}	F operand input to YB output	-	1.1	-	1.3	ns
T_{OPCYF}	F operand input to COUT output	-	0.9	-	1.0	ns
T_{OPGY}	G operand inputs to Y via XOR	-	0.8	-	0.9	ns
T_{OPGYB}	G operand input to YB output	-	1.2	-	1.3	ns
T_{OPCYG}	G operand input to COUT output	-	0.9	-	1.0	ns
T_{BXCY}	BX initialization input to COUT	-	0.51	-	0.6	ns
T_{CINX}	CIN input to X output via XOR	-	0.6	-	0.7	ns
T_{CINXB}	CIN input to XB	-	0.07	-	0.1	ns
T_{CINY}	CIN input to Y via XOR	-	0.7	-	0.7	ns
T_{CINYB}	CIN input to YB	-	0.4	-	0.5	ns
T_{BYP}	CIN input to COUT output	-	0.14	-	0.15	ns
Multiplier Operation						
T_{FANDXB}	F1/2 operand inputs to XB output via AND	-	0.35	-	0.4	ns
T_{FANDYB}	F1/2 operand inputs to YB output via AND	-	0.7	-	0.8	ns
T_{FANDCY}	F1/2 operand inputs to COUT output via AND	-	0.5	-	0.6	ns
T_{GANDYB}	G1/2 operand inputs to YB output via AND	-	0.6	-	0.7	ns
T_{GANDCY}	G1/2 operand inputs to COUT output via AND	-	0.3	-	0.4	ns
Setup/Hold Times with Respect to Clock CLK						
T_{CCKX} / T_{CKCX}	CIN input to FFX	1.2 / 0	-	1.3 / 0	-	ns
T_{CCKY} / T_{CKCY}	CIN input to FFY	1.2 / 0	-	1.3 / 0	-	ns

Revision History

Date	Version	Description
11/15/2001	1.0	Initial Xilinx release.
06/28/2002	1.1	Added -7 speed grade and extended DLL specs to Industrial.
11/18/2002	2.0	Added XC2S400E and XC2S600E. Added minimum specifications. Added reference to XAPP450 for Power-On Requirements. Removed Preliminary designation.
07/09/2003	2.1	Added I_{CCINTQ} typical values. Reduced ICCPO power-on current requirements. Relaxed TCCPO power-on ramp requirements. Added IHSPO to describe current in hot-swap applications. Updated TPSFD / TPHFD description to indicate use of delay element.
06/18/2008	2.3	Updated I/O measurement thresholds. Updated all modules for continuous page, figure, and table numbering. Updated links. Synchronized all modules to v2.3.
08/09/2013	3.0	This product is obsolete/discontinued per XCN12026.

Package Thermal Characteristics

Table 14 provides the thermal characteristics for the various Spartan-II FPGA package offerings. This information is also available using the Thermal Query tool on xilinx.com (www.xilinx.com/cgi-bin/thermal/thermal.pl).

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board (θ_{JB}) value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The "Still Air (0 LFM)" column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 14: **Spartan-IIE Package Thermal Characteristics**

Package	Device	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
TQ144 TQG144	XC2S50E	5.8	N/A	32.3	25.1	21.5	20.1	°C/Watt
	XC2S100E	5.3	N/A	31.4	24.4	20.8	19.6	°C/Watt
PQ208 PQG208	XC2S50E	7.1	N/A	35.1	25.9	22.9	21.2	°C/Watt
	XC2S100E	6.1	N/A	34.2	25.2	22.3	20.7	°C/Watt
	XC2S150E	6.0	N/A	34.1	25.2	22.2	20.6	°C/Watt
	XC2S200E	4.6	N/A	32.4	23.9	21.2	19.6	°C/Watt
	XC2S300E	4.0	N/A	31.6	23.3	20.6	19.1	°C/Watt
FT256 FTG256	XC2S50E	7.3	17.8	27.4	21.6	20.4	20.0	°C/Watt
	XC2S100E	5.8	15.1	25.0	19.5	18.2	17.8	°C/Watt
	XC2S150E	5.7	14.8	24.8	19.3	18.0	17.6	°C/Watt
	XC2S200E	3.9	11.4	21.9	16.6	15.2	14.7	°C/Watt
	XC2S300E	3.2	10.1	20.8	15.6	14.2	13.7	°C/Watt
	XC2S400E	2.5	8.8	19.7	14.5	13.2	12.6	°C/Watt
FG456 FGG456	XC2S100E	8.4	14.9	24.3	19.2	18.1	17.4	°C/Watt
	XC2S150E	8.2	14.6	24.1	19.0	17.9	17.1	°C/Watt
	XC2S200E	6.3	11.6	21.0	16.1	15.0	14.3	°C/Watt
	XC2S300E	5.6	10.4	19.9	15.1	13.9	13.2	°C/Watt
	XC2S400E	3.6	6.5	17.7	11.7	10.5	10.0	°C/Watt
	XC2S600E	2.7	5.0	17.3	11.2	10.0	9.5	°C/Watt
FG676 FGG676	XC2S400E	4.1	7.9	15.6	11.1	9.8	9.2	°C/Watt
	XC2S600E	3.4	6.9	14.5	9.9	8.6	7.9	°C/Watt

In the PQ208 package, all VCCO pins must be connected to the same voltage.

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
GND	-	P1	-	-
TMS	-	P2	-	-
I/O	7	P3	-	-
I/O	7	P4	-	XC2S200E, 300E
I/O	7	P5	-	-
I/O, VREF Bank 7, L49P	7	P6	XC2S50E, 150E, 200E, 300E	All
I/O, L49N	7	P7	XC2S50E, 150E, 200E, 300E	-
I/O	7	P8	-	-
I/O	7	P9	-	-
I/O, L48P	7	P10	XC2S50E, 300E	XC2S100E, 150E, 200E, 300E
I/O, L48N	7	P11	XC2S50E, 300E	-
GND	-	P12	-	-
VCCO	-	P13	-	-
VCCINT	-	P14	-	-
I/O, L47P_YY	7	P15	All	-
I/O, L47N_YY	7	P16	All	-
I/O, L46P_YY	7	P17	All	-
I/O, L46N_YY	7	P18	All	-
GND	-	P19	-	-
I/O, VREF Bank 7, L45P	7	P20	XC2S50E, 300E	All
I/O, L45N	7	P21	XC2S50E, 300E	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O	7	P22	-	-
I/O, L44P_YY	7	P23	All	-
I/O (IRDY), L44N_YY	7	P24	All	-
GND	-	P25	-	-
VCCO	-	P26	-	-
I/O (TRDY)	6	P27	-	-
VCCINT	-	P28	-	-
I/O	6	P29	-	-
I/O, L43P	6	P30	XC2S50E, 300E	-
I/O, VREF Bank 6, L43N	6	P31	XC2S50E, 300E	All
GND	-	P32	-	-
I/O, L42P_YY	6	P33	All	-
I/O, L42N_YY	6	P34	All	-
I/O, L41P_YY	6	P35	All	-
I/O, L41N_YY	6	P36	All	-
VCCINT	-	P37	-	-
VCCO	-	P38	-	-
GND	-	P39	-	-
I/O, L40P	6	P40	XC2S50E, 300E	-
I/O, L40N	6	P41	XC2S50E, 300E	XC2S100E, 150E, 200E, 300E
I/O	6	P42	-	-
I/O	6	P43	-	-
I/O	6	P44	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O	2	P134	-	-
I/O (D3), L17N	2	P135	XC2S50E, 300E	-
I/O, VREF Bank 2, L17P	2	P136	XC2S50E, 300E	All
GND	-	P137	-	-
I/O, L16N_YY	2	P138	All	-
I/O, L16P_YY	2	P139	All	-
I/O, L15N_YY	2	P140	All	-
I/O (D2), L15P_YY	2	P141	All	-
VCCINT	-	P142	-	-
VCCO	-	P143	-	-
GND	-	P144	-	-
I/O (D1), L14N	2	P145	XC2S50E, 300E	-
I/O, L14P	2	P146	XC2S50E, 300E	XC2S100E, 150E, 200E, 300E
I/O	2	P147	-	-
I/O	2	P148	-	-
I/O	2	P149	-	-
I/O, VREF Bank 2, L13N	2	P150	XC2S100E, 150E	All
I/O, L13P	2	P151	XC2S100E, 150E	-
I/O	2	P152	-	XC2S200E, 300E
I/O (DIN, D0), L12N_YY	2	P153	All	-
I/O (DOUT, BUSY), L12P_YY	2	P154	All	-
CCLK	2	P155	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
VCCO	-	P156	-	-
TDO	2	P157	-	-
GND	-	P158	-	-
TDI	-	P159	-	-
I/O ($\overline{CS}$), L11P_YY	1	P160	All	-
I/O ($\overline{WRITE}$), L11N_YY	1	P161	All	-
I/O	1	P162	-	XC2S200E, 300E
I/O	1	P163	-	-
I/O, VREF Bank 1, L10P_YY	1	P164	All	All
I/O, L10N_YY	1	P165	All	-
I/O	1	P166	-	-
I/O	1	P167	-	-
I/O, L9P	1	P168	XC2S50E, 100E, 200E, 300E	XC2S100E, 150E, 200E, 300E
I/O, L9N	1	P169	XC2S50E, 100E, 200E, 300E	-
GND	-	P170	-	-
VCCO	-	P171	-	-
VCCINT	-	P172	-	-
I/O, L8P	1	P173	XC2S50E, 100E, 200E, 300E	-
I/O, L8N	1	P174	XC2S50E, 100E, 200E, 300E	-
I/O, L7P	1	P175	XC2S50E, 200E, 300E	-
I/O, L7N	1	P176	XC2S50E, 200E, 300E	-
GND	-	P177	-	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O (D5), L35N_YY	3	L13	All	-
I/O, L35P_YY	3	K14	All	-
I/O, L34N	3	K15	XC2S100E, 150E, 400E	-
I/O, L34P	3	K16	XC2S100E, 150E, 400E	-
I/O, L33N	3	L12	XC2S50E, 100E, 150E, 200E, 300E(1)	-
I/O, L33P	3	K12	XC2S50E, 100E, 150E, 200E, 300E(1)	-
I/O, VREF Bank 3, L32N	3	K13	XC2S50E, 300E, 400E	All
I/O (D4), L32P	3	J14	XC2S50E, 300E, 400E	-
I/O, L31N	3	J15	XC2S100E, 150E, 200E, 400E	-
I/O, L31P	3	J16	XC2S100E, 150E, 200E, 400E	XC2S400E
I/O (TRDY)	3	J13	-	-
I/O (IRDY), L30N_YY	2	H16	All	-
I/O, L30P_YY	2	G16	All	-
I/O, L29N	2	H14	XC2S100E, 150E, 200E, 400E	XC2S400E
I/O, L29P	2	H15	XC2S100E, 150E, 200E, 400E	-
I/O (D3), L28N	2	G15	XC2S50E, 300E, 400E	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 2, L28P	2	F16	XC2S50E, 300E, 400E	All
I/O, L27N	2	H13	XC2S50E, 100E, 150E, 200E, 300E(1)	-
I/O, L27P	2	G14	XC2S50E, 100E, 150E, 200E, 300E(2)	-
I/O, L26N	2	F15	XC2S100E, 150E, 400E	-
I/O, L26P	2	E16	XC2S100E, 150E, 400E	-
I/O, L25N_YY	2	G13	All	-
I/O (D2), L25P_YY	2	F14	All	-
I/O (D1), L24N	2	E15	XC2S50E, 300E, 400E	-
I/O, L24P	2	D16	XC2S50E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L23N	2	F13	XC2S150E, 200E, 400E	-
I/O, L23P	2	E14	XC2S150E, 200E, 400E	-
I/O, L22N	2	D15	XC2S50E, 150E, 200E, 300E, 400E	-
I/O, VREF Bank 2, L22P	2	C16	XC2S50E, 150E, 200E, 300E, 400E	All
I/O, L21N	2	G12	XC2S50E, 100E, 200E, 300E	-
I/O, L21P	2	F12	XC2S50E, 100E, 200E, 300E	-
I/O, L20N	2	E13	XC2S100E, 200E, 300E	-

Additional FT256 Package Pins *(Continued)*

VCCO Bank 5 Pins				
L7	L8	M8	-	-
VCCO Bank 6 Pins				
J5	J6	K6	-	-
VCCO Bank 7 Pins				
G6	H5	H6	-	-
GND Pins				
A1	A16	B2	B15	F6
F11	G7	G8	G9	G10
H7	H8	H9	H10	J7
J8	J9	J10	K7	K8
K9	K10	L6	L11	R2
R15	T1	T16	-	-

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O	7	H5	-	-	-	-	-	I/O	I/O	I/O
I/O, VREF Bank 7, L#P_Y	7	H3	XC2S300E, 400E, 600E	All	I/O, VREF Bank 7, L81P	I/O, VREF Bank 7, L106P	I/O, VREF Bank 7, L113P	I/O, VREF Bank 7, L113P_Y	I/O, VREF Bank 7, L113P_Y	I/O, VREF Bank 7, L113P_Y
I/O, L#N_Y	7	H4	XC2S300E, 400E, 600E	-	I/O, L81N	I/O, L106N	I/O, L113N	I/O, L113N_Y	I/O, L113N_Y	I/O, L113N_Y
I/O, L#P_YY	7	H2	All	-	I/O, L80P_YY	I/O, L105P_YY	I/O, L112P_YY	I/O, L112P_YY	I/O, L112P_YY	I/O, L112P_YY
I/O, L#N_YY	7	H1	All	-	I/O, L80N_YY	I/O, L105N_YY	I/O, L112N_YY	I/O, L112N_YY	I/O, L112N_YY	I/O, L112N_YY
I/O	7	J6	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	J4	XC2S150E, 200E, 300E, 400E	-	-	I/O, L104P_Y	I/O, L111P_Y	I/O, L111P_Y	I/O, L111P_Y	I/O, L111P
I/O, L#N_Y	7	J5	XC2S100E, 150E, 200E, 300E, 400E	-	I/O, L79P_Y	I/O, L104N_Y	I/O, L111N_Y	I/O, L111N_Y	I/O, L111N_Y	I/O, L111N
I/O, L#P_Y	7	J3	XC2S100E, 150E, 200E, 300E, 600E	-	I/O, L79N_Y	I/O, L103P_Y	I/O, L110P_Y	I/O, L110P_Y	I/O, L110P	I/O, L110P_Y
I/O, L#N_Y	7	J2	XC2S150E, 200E, 300E, 600E	-	-	I/O, L103N_Y	I/O, L110N_Y	I/O, L110N_Y	I/O, L110N	I/O, L110N_Y
I/O	7	J1	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#P	7	K5	XC2S100E, 150E, 200E, 300E, 600E[1]	-	I/O, L78P_YY	I/O, L102P_YY	I/O, L109P_YY	I/O, L109P_YY	I/O, L109P	I/O, L109P_Y
I/O, L#N	7	K6	XC2S100E, 150E, 200E, 300E, 600E[1]	-	I/O, L78N_YY	I/O, L102N_YY	I/O, L109N_YY	I/O, L109N_YY	I/O, L109N	I/O, L109N_Y
I/O, VREF Bank 7, L#P_Y	7	K3	XC2S300E, 400E, 600E	All	I/O, VREF Bank 7, L77P	I/O, VREF Bank 7, L101P	I/O, VREF Bank 7, L108P	I/O, VREF Bank 7, L108P_Y	I/O, VREF Bank 7, L108P_Y	I/O, VREF Bank 7, L108P_Y
I/O, L#N_Y	7	K4	XC2S300E, 400E, 600E	-	I/O, L77N	I/O, L101N	I/O, L108N	I/O, L108N_Y	I/O, L108N_Y	I/O, L108N_Y
I/O	7	K2	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P_Y	7	K1	XC2S300E, 400E	-	-	-	I/O, L107P	I/O, L107P_Y	I/O, L107P_Y	I/O, L107P
I/O, L#N_Y	7	L1	XC2S100E, 150E, 300E, 400E	-	I/O, L76P_Y	I/O, L100P_Y	I/O, L107N	I/O, L107N_Y	I/O, L107N_Y	I/O, L107N
I/O, L#P_Y	7	L3	XC2S100E, 150E, 200E, 300E, 600E	XC2S400E, 600E	I/O, L76N_Y	I/O, L100N_Y	I/O, L106P_Y	I/O, L106P_Y	I/O, VREF Bank 7, L106P	I/O, VREF Bank 7, L106P_Y
I/O, L#N_Y	7	L2	XC2S200E, 300E, 600E	-	-	I/O	I/O, L106N_Y	I/O, L106N_Y	I/O, L106N	I/O, L106N_Y
I/O	7	L4	-	-	-	-	-	I/O	I/O	I/O

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O, L#P_YY	7	L5	All	-	I/O, L75P_YY	I/O, L99P_YY	I/O, L105P_YY	I/O, L105P_YY	I/O, L105P_YY	I/O, L105P_YY
I/O (IRDY), L#N_YY	7	L6	All	-	I/O (IRDY), L75N_YY	I/O (IRDY), L99N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY
I/O (TRDY)	6	M1	-	-	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)
I/O	6	M2	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P_Y	6	M3	XC2S200E, 300E, 600E	-	-	I/O	I/O, L104P_Y	I/O, L104P_Y	I/O, L104P	I/O, L104P_Y
I/O, L#N_Y	6	M4	XC2S100E, 150E, 200E, 300E, 600E	XC2S400E, 600E	I/O, L74P_Y	I/O, L98P_Y	I/O, L104N_Y	I/O, L104N_Y	I/O, VREF Bank 6, L104N	I/O, VREF Bank 6, L104N_Y
I/O, L#P_Y	6	M5	XC2S100E, 150E, 300E, 400E	-	I/O, L74N_Y	I/O, L98N_Y	I/O, L103P	I/O, L103P_Y	I/O, L103P_Y	I/O, L103P
I/O, L#N_Y	6	M6	XC2S300E, 400E	-	-	-	I/O, L103N	I/O, L103N_Y	I/O, L103N_Y	I/O, L103N
I/O	6	N1	-	-	-	-	-	I/O	I/O	I/O
I/O	6	N2	-	-	I/O, L73P	I/O, L97P	I/O	I/O	I/O	I/O
I/O, VREF Bank 6, L#P	6	N3	XC2S200E, 400E	All	I/O, VREF Bank 6, L73N	I/O, VREF Bank 6, L97N	I/O, VREF Bank 6, L102P_Y	I/O, VREF Bank 6, L102P	I/O, VREF Bank 6, L102P_Y	I/O, VREF Bank 6, L102P
I/O, L#N	6	N4	XC2S100E, 150E, 200E, 400E	-	I/O, L72P_Y	I/O, L96P_Y	I/O, L102N_Y	I/O, L102N	I/O, L102N_Y	I/O, L102N
I/O, L#P_Y	6	N5	XC2S100E, 150E, 300E, 600E	-	I/O, L72N_Y	I/O, L96N_Y	I/O, L101P	I/O, L101P_Y	I/O, L101P	I/O, L101P_Y
I/O, L#N_Y	6	N6	XC2S300E, 600E	-	-	-	I/O, L101N	I/O, L101N_Y	I/O, L101N	I/O, L101N_Y
I/O, L#P_Y	6	P1	XC2S150E, 200E, 300E, 600E	-	-	I/O, L95P_Y	I/O, L100P_Y	I/O, L100P_Y	I/O, L100P	I/O, L100P_Y
I/O, L#N_Y	6	P2	XC2S100E, 150E, 200E, 300E, 600E	-	I/O, L71P_Y	I/O, L95N_Y	I/O, L100N_Y	I/O, L100N_Y	I/O, L100N	I/O, L100N_Y
I/O	6	R1	XC2S100E, 150E	-	I/O, L71N_Y	I/O, L94P_Y	I/O	I/O	I/O	I/O
I/O, L#P_Y	6	P3	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L94N_Y	I/O, L99P_Y	I/O, L99P_Y	I/O, L99P_Y	I/O, L99P_Y
I/O, L#N_Y	6	P4	XC2S200E, 300E, 400E, 600E	-	-	-	I/O, L99N_Y	I/O, L99N_Y	I/O, L99N_Y	I/O, L99N_Y
I/O, L#P_YY	6	P5	All	-	I/O, L70P_YY	I/O, L93P_YY	I/O, L98P_YY	I/O, L98P_YY	I/O, L98P_YY	I/O, L98P_YY
I/O, L#N_YY	6	P6	All	-	I/O, L70N_YY	I/O, L93N_YY	I/O, L98N_YY	I/O, L98N_YY	I/O, L98N_YY	I/O, L98N_YY

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O, L#P_Y	6	R2	XC2S300E, 400E, 600E	-	I/O, L69P	I/O, L92P	I/O, L97P	I/O, L97P_Y	I/O, L97P_Y	I/O, L97P_Y
I/O, VREF Bank 6, L#N_Y	6	R3	XC2S300E, 400E, 600E	All	I/O, VREF Bank 6, L69N	I/O, VREF Bank 6, L92N	I/O, VREF Bank 6, L97N	I/O, VREF Bank 6, L97N_Y	I/O, VREF Bank 6, L97N_Y	I/O, VREF Bank 6, L97N_Y
I/O	6	R4	-	-	-	-	-	I/O	I/O	I/O
I/O	6	R5	-	-	I/O	I/O	I/O	I/O	I/O	I/O
I/O, L#P	6	T2	XC2S200E, 400E, 600E	XC2S600E	I/O, L68P	I/O, L91P	I/O, L96P_Y	I/O, L96P	I/O, L96P_Y	I/O, VREF Bank 6, L96P_Y
I/O, L#N	6	T3	XC2S200E, 400E, 600E	-	I/O, L68N	I/O, L91N	I/O, L96N_Y	I/O, L96N	I/O, L96N_Y	I/O, L96N_Y
I/O, L#P_Y	6	T4	XC2S150E, 300E, 400E	-	-	I/O, L90P_Y	I/O, L95P	I/O, L95P_Y	I/O, L95P_Y	I/O, L95P
I/O, L#N_Y	6	T5	XC2S150E, 300E, 400E	-	-	I/O, L90N_Y	I/O, L95N	I/O, L95N_Y	I/O, L95N_Y	I/O, L95N
I/O, L#P_Y	6	T1	XC2S150E, 200E, 300E, 400E, 600E	-	I/O, L67P	I/O, L89P_Y	I/O, L94P_Y	I/O, L94P_Y	I/O, L94P_Y	I/O, L94P_Y
I/O, VREF Bank 6, L#N_Y	6	U1	XC2S150E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 6, L67N	I/O, VREF Bank 6, L89N_Y	I/O, VREF Bank 6, L94N_Y	I/O, VREF Bank 6, L94N_Y	I/O, VREF Bank 6, L94N_Y	I/O, VREF Bank 6, L94N_Y
I/O	6	U2	XC2S100E	-	I/O, L66P_Y	I/O	I/O	I/O	I/O	I/O
I/O, L#P_Y	6	U3	XC2S100E, 150E, 200E, 300E, 400E, 600E	-	I/O, L66N_Y	I/O, L88P_Y	I/O, L93P_Y	I/O, L93P_Y	I/O, L93P_Y	I/O, L93P_Y
I/O, L#N_Y	6	U4	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L88N_Y	I/O, L93N_Y	I/O, L93N_Y	I/O, L93N_Y	I/O, L93N_Y
I/O	6	V1	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P_Y	6	W1	XC2S100E, 200E, 300E, 600E	-	I/O, L65P_Y	I/O, L87P	I/O, L92P_Y	I/O, L92P_Y	I/O, L92P	I/O, L92P_Y
I/O, L#N_Y	6	V2	XC2S100E, 200E, 300E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L65N_Y	I/O, L87N	I/O, VREF Bank 6, L92N_Y	I/O, VREF Bank 6, L92N_Y	I/O, VREF Bank 6, L92N	I/O, VREF Bank 6, L92N_Y
I/O	6	W2	-	-	I/O	I/O	I/O	I/O	I/O	I/O
I/O, L#P_Y	6	V3	XC2S200E, 300E, 400E	-	-	I/O, L86P	I/O, L91P_Y	I/O, L91P_Y	I/O, L91P_Y	I/O, L91P
I/O, L#N_Y	6	V4	XC2S200E, 300E, 400E	-	-	I/O, L86N	I/O, L91N_Y	I/O, L91N_Y	I/O, L91N_Y	I/O, L91N
I/O	6	Y1	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P_YY	6	Y2	All	-	I/O, L64P_YY	I/O, L85P_YY	I/O, L90P_YY	I/O, L90P_YY	I/O, L90P_YY	I/O, L90P_YY
I/O, L#N_YY	6	W3	All	-	I/O, L64N_YY	I/O, L85N_YY	I/O, L90N_YY	I/O, L90N_YY	I/O, L90N_YY	I/O, L90N_YY
M1	-	U5	-	-	M1	M1	M1	M1	M1	M1

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O	5	AC5	-	-	I/O	I/O
I/O, L152N	5	AE4	-	-	I/O	I/O, L152N
I/O, L152P	5	AF4	-	-	-	I/O, L152P
I/O, L151N	5	AE5	-	-	-	I/O, L151N
I/O, L151P	5	AF5	-	-	I/O	I/O, L151P
I/O, L150N	5	AA6	XC2S400E	-	I/O, L150N_Y	I/O, L150N
I/O, L150P	5	AB6	XC2S400E	-	I/O, L150P_Y	I/O, L150P
I/O, L149N_YY	5	AC6	All	-	I/O, L149N_YY	I/O, L149N_YY
I/O, L149P_YY	5	AD6	All	-	I/O, L149P_YY	I/O, L149P_YY
I/O, VREF Bank 5, L148N_YY	5	AE6	All	All	I/O, VREF Bank 5, L148N_YY	I/O, VREF Bank 5, L148N_YY
I/O, L148P_YY	5	AF6	All	-	I/O, L148P_YY	I/O, L148P_YY
I/O, L147N	5	AA7	XC2S600E	-	-	I/O, L147N_Y
I/O, L147P	5	AB7	XC2S600E	-	I/O	I/O, L147P_Y
I/O, L146N_YY	5	AC7	All	-	I/O, L146N_YY	I/O, L146N_YY
I/O, L146P_YY	5	AD7	All	-	I/O, L146P_YY	I/O, L146P_YY
I/O, L145N_YY	5	AE7	All	-	I/O, L145N_YY	I/O, L145N_YY
I/O, L145P_YY	5	AF7	All	-	I/O, L145P_YY	I/O, L145P_YY
I/O, VREF Bank 5, L144N_YY	5	Y8	All	All	I/O, VREF Bank 5, L144N_YY	I/O, VREF Bank 5, L144N_YY
I/O, L144P_YY	5	AA8	All	-	I/O, L144P_YY	I/O, L144P_YY
I/O, L143N_YY	5	AE8	All	-	I/O, L143N_YY	I/O, L143N_YY
I/O, L143P_YY	5	AF8	All	-	I/O, L143P_YY	I/O, L143P_YY
I/O	5	AB8	-	-	I/O	I/O
I/O, L142N	5	W9	XC2S600E	-	I/O, L142N	I/O, L142N_Y
I/O, L142P	5	Y9	XC2S600E	-	I/O, L142P	I/O, L142P_Y
I/O, L141N	5	AA9	XC2S600E	XC2S600E	-	I/O, VREF Bank 5, L141N_Y
I/O, L141P	5	AB9	XC2S600E	-	I/O	I/O, L141P_Y
I/O, L140N_YY	5	AC9	All	-	I/O, L140N_YY	I/O, L140N_YY
I/O, L140P_YY	5	AD9	All	-	I/O, L140P_YY	I/O, L140P_YY
I/O, L139N_YY	5	AE9	All	-	I/O, L139N_YY	I/O, L139N_YY
I/O, L139P_YY	5	AF9	All	-	I/O, L139P_YY	I/O, L139P_YY
I/O, VREF Bank 5, L138N_YY	5	W10	All	All	I/O, VREF Bank 5, L138N_YY	I/O, VREF Bank 5, L138N_YY

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L39N	1	F18	XC2S600E	-	I/O, L39N	I/O, L39N_Y
I/O, L38P	1	D18	XC2S600E	XC2S600E	-	I/O, VREF Bank 1, L38P_Y
I/O, L38N	1	C18	XC2S600E	-	I/O	I/O, L38N_Y
I/O, L37P_YY	1	B18	All	-	I/O, L37P_YY	I/O, L37P_YY
I/O, L37N_YY	1	A18	All	-	I/O, L37N_YY	I/O, L37N_YY
I/O, L36P_YY	1	H17	All	-	I/O, L36P_YY	I/O, L36P_YY
I/O, L36N_YY	1	G17	All	-	I/O, L36N_YY	I/O, L36N_YY
I/O, VREF Bank 1, L35P_YY	1	E18	All	All	I/O, VREF Bank 1, L35P_YY	I/O, VREF Bank 1, L35P_YY
I/O, L35N_YY	1	E17	All	-	I/O, L35N_YY	I/O, L35N_YY
I/O, L34P_YY	1	D17	All	-	I/O, L34P_YY	I/O, L34P_YY
I/O, L34N_YY	1	C17	All	-	I/O, L34N_YY	I/O, L34N_YY
I/O	1	H16	-	-	-	I/O
I/O, L33P	1	B17	XC2S600E	-	I/O, L33P	I/O, L33P_Y
I/O, L33N	1	A17	XC2S600E	-	I/O, L33N	I/O, L33N_Y
I/O	1	G16	-	-	-	I/O
I/O, L32P_YY	1	F16	All	-	I/O, L32P_YY	I/O, L32P_YY
I/O, L32N_YY	1	E16	All	-	I/O, L32N_YY	I/O, L32N_YY
I/O, L31P_YY	1	C16	All	-	I/O, L31P_YY	I/O, L31P_YY
I/O, L31N_YY	1	B16	All	-	I/O, L31N_YY	I/O, L31N_YY
I/O	1	A16	-	-	-	I/O
I/O, L30P	1	J15	-	-	I/O, L30P	I/O, L30P
I/O, L30N	1	H15	-	-	I/O, L30N	I/O, L30N
I/O	1	G15	-	-	-	I/O
I/O, L29P_YY	1	F15	All	-	I/O, L29P_YY	I/O, L29P_YY
I/O, L29N_YY	1	E15	All	-	I/O, L29N_YY	I/O, L29N_YY
I/O, VREF Bank 1, L28P_YY	1	B15	All	All	I/O, VREF Bank 1, L28P_YY	I/O, VREF Bank 1, L28P_YY
I/O, L28N_YY	1	A15	All	-	I/O, L28N_YY	I/O, L28N_YY
I/O	1	D15	-	-	-	I/O
I/O, L27P_YY	1	J14	All	-	I/O, L27P_YY	I/O, L27P_YY
I/O, L27N_YY	1	H14	All	-	I/O, L27N_YY	I/O, L27N_YY
I/O	1	G14	-	-	-	I/O
I/O, L26P	1	F14	XC2S600E	-	I/O, L26P	I/O, L26P_Y
I/O, L26N	1	E14	XC2S600E	-	I/O, L26N	I/O, L26N_Y

Additional FG676 Package Pins *(Continued)*

GND Pins						
A1	A26	B2	B25	C3	C12	C15
C24	D4	D8	D19	D23	F10	F17
H4	H23	K6	K21	L11	L12	L13
L14	L15	L16	M3	M11	M12	M13
M14	M15	M16	M24	N11	N12	N13
N14	N15	N16	P11	P12	P13	P14
P15	P16	R3	R11	R12	R13	R14
R15	R16	R24	T11	T12	T13	T14
T15	T16	U6	U21	W4	W23	AA10
AA17	AC4	AC8	AC19	AC23	AD3	AD12
AD15	AD24	AE2	AE25	AF1	AF26	-
Not Connected Pins (XC2S400E Only)						
A12	A16	A23	B3	C1	C2	C10
C11	C25	D2	D15	D18	D24	D25
E7	E13	E19	F2	F6	F8	F12
F20	F22	G10	G14	G15	G16	G26
H10	H13	H16	H25	J6	J8	J12
J13	K1	K4	K22	K24	L3	L19
L22	L26	M4	M9	M22	N1	N4
N9	N18	N19	N23	P4	P5	P18
P19	P24	R4	R7	R19	T3	T24
U1	U4	U7	U24	U25	V8	V12
V13	V21	W12	W13	W14	W16	Y3
Y7	Y21	AA7	AA9	AA22	AB15	AB16
AB17	AB22	AC1	AC15	AC22	AC25	AC26
AD1	AD2	AD10	AD11	AD13	AD14	AE5
AE19	AE24	AF4	AF16	AF18	AF20	-