Infineon Technologies - MB96F673RBPMC-GSE1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f673rbpmc-gse1

- A/D converter
  - SAR-type
  - 8/10-bit resolution
  - Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger, reload timers and PPGs
  - Range Comparator Function
  - Scan Disable Function
  - ADC Pulse Detection Function
- Source Clock Timers

  Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)
- Hardware Watchdog Timer
  - Hardware watchdog timer is active after reset
  - Window function of Watchdog Timer is used to select the lower window limit of the watchdog interval
- Reload Timers
  - 16-bit wide
  - Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
  - Event count function
- Free-Running Timers
  - Signals an interrupt on overflow
  - Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency
- Input Capture Units
  - 16-bit wide
  - Signals an interrupt upon external event
  - Rising edge, Falling edge or Both (rising & falling) edges sensitive
- Programmable Pulse Generator
  - 16-bit down counter, cycle and duty setting registers
  - Can be used as 2 × 8-bit PPG
  - Interrupt at trigger, counter borrow and/or duty match
  - PWM operation and one-shot operation
  - Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock or of selected Reload timer underflow as clock input
  - Can be triggered by software or reload timer
  - Can trigger ADC conversion
  - Timing point capture
- Stepping Motor Controller
  - Stepping Motor Controller with integrated high current output drivers
  - Four high current outputs for each channel
  - Two synchronized 8/10-bit PWMs per channel
  - Internal prescaling for PWM clock: 1, 1/4, 1/5, 1/6, 1/8, 1/10, 1/12, 1/16 of peripheral clock
  - Dedicated power supply for high current output drivers
- LCD Controller
  - LCD controller with up to 4COM × 24SEG
  - Internal or external voltage generation
  - Duty cycle: Selectable from options: 1/2, 1/3 and 1/4
  - Fixed 1/3 bias
  - Programmable frame period
  - Clock source selectable from four options (main clock, peripheral clock, subclock or RC oscillator clock)
  - Internal divider resistors or external divider resistors
  - On-chip data memory for display
  - LCD display can be operated in Timer Mode
  - Blank display: selectable
  - All SEG, COM and V pins can be switched between general and specialized purposes
- Sound Generator
  - 8-bit PWM signal is mixed with tone frequency from 16-bit reload counter
  - PWM clock by internal prescaler: 1, 1/2, 1/4, 1/8 of peripheral clock
- Real Time Clock
  - Operational on main oscillation (4MHz), sub oscillation (32kHz) or RC oscillation (100kHz/2MHz)
  - Capable to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
  - Read/write accessible second/minute/hour registers
  - Can signal interrupts every half second/second/minute/hour/day
  - Internal clock divider and prescaler provide exact 1s clock
- External Interrupts
  - Edge or Level sensitive
  - Interrupt mask bit per channel
  - Each available CAN channel RX has an external interrupt for wake-up
  - Selected USART channels SIN have an external interrupt for wake-up
- Non Maskable Interrupt
  - Disabled after reset, can be enabled by Boot-ROM depending on ROM configuration block
  - Once enabled, can not be disabled other than by reset
  - High or Low level sensitive
  - Pin shared with external interrupt 0
- I/O Ports
  - Most of the external pins can be used as general purpose I/O
  - All push-pull outputs (except when used as I2C SDA/SCL line)
  - Bit-wise programmable as input/output or peripheral signal
  - Bit-wise programmable input enable
  - One input level per GPIO-pin (either Automotive or CMOS hysteresis)
  - Bit-wise programmable pull-up resistor

1. Product Lineup

Features			MB96670	Remark
Product Type			Flash Memory Product	
Subclock			Subclock can be set by software	
Dual Operation Flash Memory		RAM	-	
64.5KB + 32KB		4KB	MB96F673R, MB96F673A	Product Options R: MCU with CAN A: MCU without CAN
128.5KB + 32KB		4KB	MB96F675R, MB96F675A	
Package			LQFP-64 FPT-64P-M23/M24	
DMA			2ch	
USART			2ch	LIN-USART 0/1
	with automatic LIN-Header transmission/reception		Yes (only 1ch)	LIN-USART 0
	with 16 byte RX- and TX-FIFO		No	
I^2C			1ch	I^2C 0
8/10-bit A/D Converter			12ch	AN 8/9/12/13/16 to 23
	with Data Buffer		No	
	with Range Comparator		Yes	
	with Scan Disable		Yes	
	with ADC Pulse Detection		Yes	
16-bit Reload Timer (RLT)			3ch	RLT 1/2/6
16-bit Free-Running Timer (FRT)			2ch	FRT 0/1
16-bit Input Capture Unit (ICU)			4ch (2 channels for LIN-USART)	ICU 0/1/4/5 ICU 0/1 for LIN-USART
8/16-bit Programmable Pulse Generator (PPG)			4ch (16-bit) / 8ch (8-bit)	PPG 0 to 3
	with Timing point capture		Yes	
	with Start delay		No	
	with Ramp		No	
CAN Interface			1ch	CAN 0 32 Message Buffers
Stepping Motor Controller (SMC)			2ch	SMC 0/1
External Interrupts (INT)			7ch	INT 0 to 4/6/7
Non-Maskable Interrupt (NMI)			1ch	
Sound Generator (SG)			1ch	SG 0
LCD Controller			4COM × 24SEG	COM 0 to 3 SEG 3 to 6/8 to 11/ 19 to 21/23/30/36 to 39/42/45 to 47/54 to 56
Real Time Clock (RTC)			1ch	
I/O Ports			48 (Dual clock mode) 50 (Single clock mode)	
Clock Calibration Unit (CAL)			1ch	
Clock Output Function			2ch	
Low Voltage Detection Function			Yes	Low voltage detection function can be disabled by software
Hardware Watchdog Timer			Yes	
On-chip RC-oscillator			Yes	
On-chip Debugger			Yes	

Note:

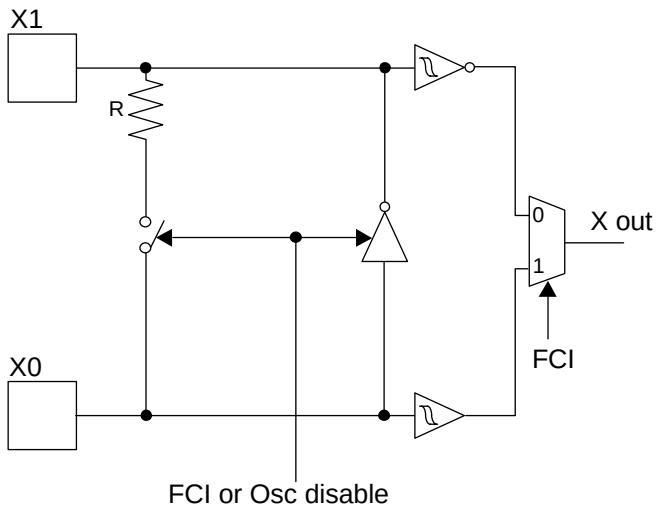
All signals of the peripheral function in each product cannot be allocated by limiting the pins of package.

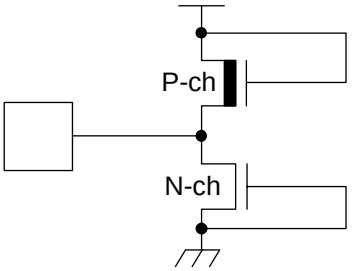
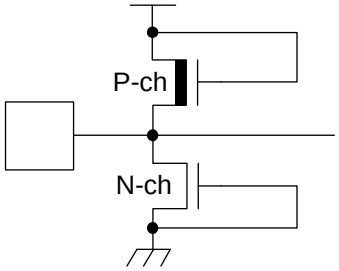
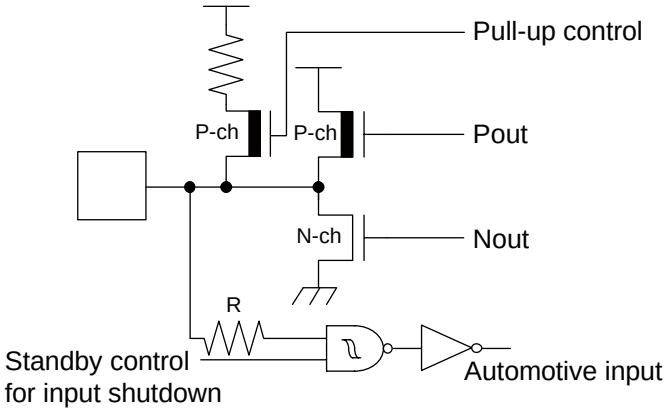
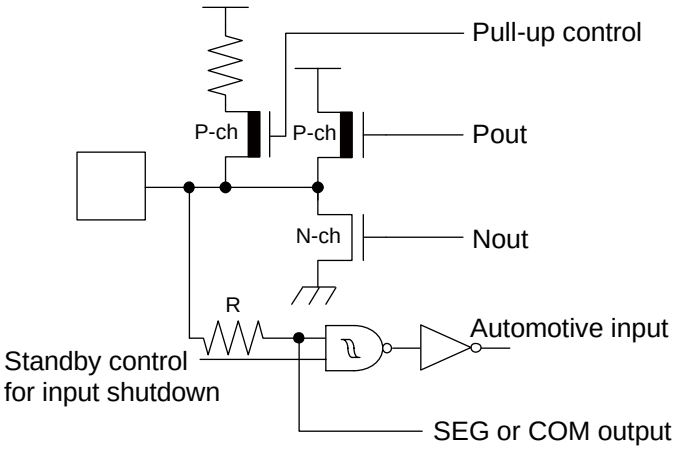
It is necessary to use the port relocate function of the general I/O port according to your function use.

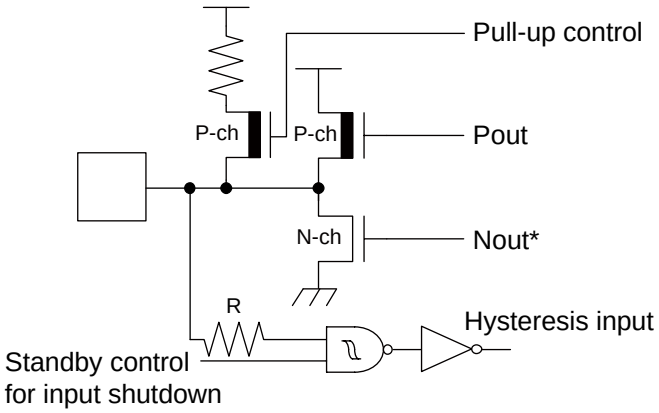
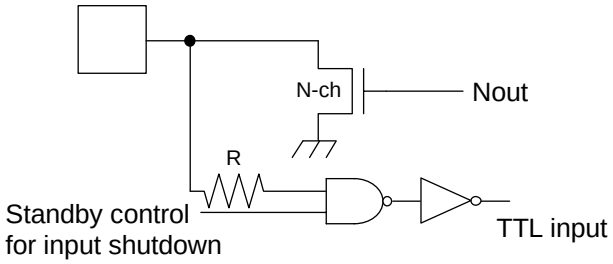
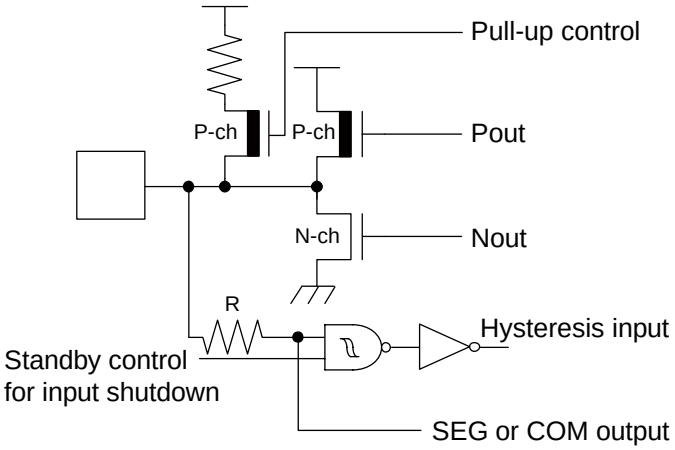
Pin no.	I/O circuit type*	Pin name
33	N	P04_5 / SCL0
34	O	DEBUG I/F
35	H	P17_0
36	C	MD
37	A	X0
38	A	X1
39	Supply	Vss
40	B	P04_0 / X0A
41	B	P04_1 / X1A
42	C	RSTX
43	J	P11_7 / SEG3 / IN0_R
44	J	P11_0 / COM0
45	J	P11_1 / COM1 / PPG0_R
46	J	P11_2 / COM2 / PPG1_R
47	J	P11_3 / COM3 / PPG2_R
48	J	P12_0 / SEG4 / IN1_R
49	J	P12_1 / SEG5 / TIN1_R / PPG0_B
50	J	P12_2 / SEG6 / TOT1_R / PPG1_B
51	J	P12_4 / SEG8
52	J	P12_5 / SEG9 / TIN2_R / PPG2_B
53	J	P12_6 / SEG10 / TOT2_R / PPG3_B
54	J	P12_7 / SEG11 / INT1_R
55	J	P01_1 / SEG21 / CKOT1
56	J	P01_3 / SEG23
57	L	P03_0 / SEG36 / V0
58	L	P03_1 / SEG37 / V1
59	L	P03_2 / SEG38 / V2
60	L	P03_3 / SEG39 / V3
61	M	P03_4 / RX0 / INT4
62	H	P03_5 / TX0
63	H	P03_6 / INT0 / NMI
64	Supply	Vcc

*: See “I/O CIRCUIT TYPE” for details on the I/O circuit types.

6. I/O Circuit Type

Type	Circuit	Remarks
A		High-speed oscillation circuit: • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Feedback resistor = approx. 1.0MΩ • The amplitude: 1.8V±0.15V to operate by the internal supply voltage

Type	Circuit	Remarks
F		Power supply input protection circuit
G		• A/D converter ref+ (AVRH) power supply input pin with protection circuit • Without protection circuit against V_{CC} for pins AVRH
H		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • Automotive input with input shutdown function • Programmable pull-up resistor
J		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • Automotive input with input shutdown function • Programmable pull-up resistor • SEG or COM output

Type	Circuit	Remarks
N		• CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor *: N-channel transistor has slew rate control according to I^2C spec, irrespective of usage.
O		• Open-drain I/O • Output 25mA, Vcc = 2.7V • TTL input
P		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • CMOS hysteresis inputs with input shutdown function • Programmable pull-up resistor • SEG or COM output

13. Handling Devices

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Notes on PLL clock mode operation
- Power supply pins (Vcc/Vss)
- Crystal oscillator and ceramic resonator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on Power-on
- Stabilization of power supply voltage
- SMC power supply pins
- Serial communication
- Mode Pin (MD)

13.1 Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between Vcc pins and Vss pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

13.2 Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register

PIER = 0).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent

damage of the device. To prevent latch-up, they must therefore be pulled up or pulled down through resistors which should be more than 2kΩ.

Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with

either input disabled or external pull-up/pull-down resistor as described above.

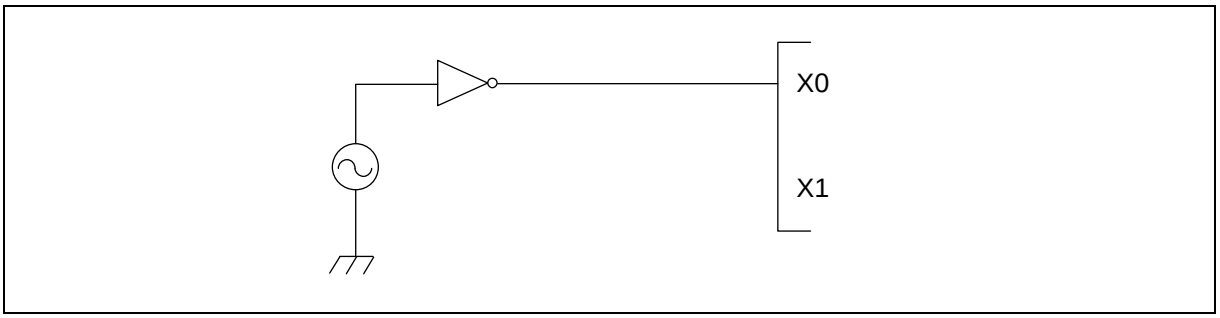
13.3 External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration.

See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

13.3.1 Single phase external clock for Main oscillator

When using a single phase external clock for the Main oscillator, X0 pin must be driven and X1 pin left open.
And supply 1.8V power to the external clock.



13.3.2 Single phase external clock for Sub oscillator

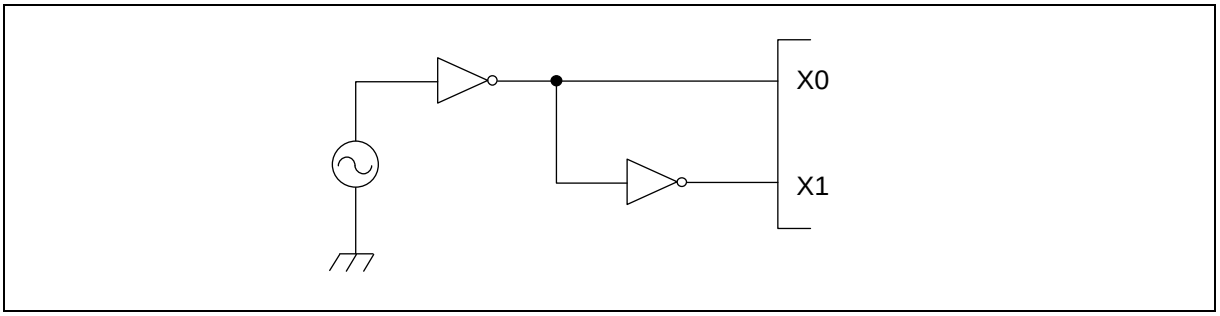
When using a single phase external clock for the Sub oscillator, “External clock mode” must be selected and

X0A/P04_0 pin must be driven. X1A/P04_1 pin can be configured as GPIO.

13.3.3 Opposite phase external clock

When using an opposite phase external clock, X1 (X1A) pins must be supplied with a clock signal which has

the opposite phase to the X0 (X0A) pins. Supply level on X0 and X1 pins must be 1.8V.



13.4 Notes on PLL clock mode operation

If the microcontroller is operated with PLL clock mode and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

13.5 Power supply pins (Vcc/Vss)

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

Vcc and Vss pins must be connected to the device from the power supply with lowest possible impedance.

The smoothing capacitor at Vcc pin must use the one of a capacity value that is larger than Cs.

Besides this, as a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1μF between Vcc and Vss pins as close as possible to Vcc and Vss pins.

14.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}, DV_{CC}	2.7	-	5.5	V	
		2.0	-	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor at C pin	C_S	0.5	1.0 to 3.9	4.7	µF	1.0µF (Allowance within ± 50%) 3.9µF (Allowance within ± 20%) Please use the ceramic capacitor or the capacitor of the frequency response of this level. The smoothing capacitor at V_{CC} must use the one of a capacity value that is larger than C_S.

WARNING

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

14.3 DC Characteristics

14.3.1 Current Rating

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Run modes[*1]	I_{CCPLL}	Vcc	PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32MHz Flash 0 wait	-	25	-	mA	T_A = +25°C
			(CLKRC and CLKSC stopped)	-	-	34	mA	T_A = +105°C
	I_{CCMAIN}		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz Flash 0 wait	-	3.5	-	mA	T_A = +25°C
			(CLKPLL, CLKSC and CLKRC stopped)	-	-	7.5	mA	T_A = +105°C
	I_{CCRCH}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz Flash 0 wait	-	1.7	-	mA	T_A = +25°C
			(CLKMC, CLKPLL and CLKSC stopped)	-	-	5.5	mA	T_A = +105°C
	I_{CCRCL}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz Flash 0 wait	-	0.15	-	mA	T_A = +25°C
			(CLKMC, CLKPLL and CLKSC stopped)	-	-	3.2	mA	T_A = +105°C
	I_{CCSUB}		Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz Flash 0 wait	-	0.1	-	mA	T_A = +25°C
			(CLKMC, CLKPLL and CLKRC stopped)	-	-	3	mA	T_A = +105°C

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH4}	4mA type	$4.5V \le (D)V_{CC} \le 5.5V$ $I_{OH} = -4mA$	$(D)V_{CC}$ - 0.5	-	$(D)V_{CC}$	V	
			$2.7V \le (D)V_{CC} < 4.5V$ $I_{OH} = -1.5mA$					
	V_{OH30}	High Drive type*	$4.5V \le DV_{CC} \le 5.5V$ $I_{OH} = -52mA$	DV_{CC} - 0.5	-	DV_{CC}	V	$T_A = -40°C$
			$2.7V \le DV_{CC} < 4.5V$ $I_{OH} = -18mA$					
			$4.5V \le DV_{CC} \le 5.5V$ $I_{OH} = -39mA$					$T_A = +25°C$
			$2.7V \le DV_{CC} < 4.5V$ $I_{OH} = -16mA$					
			$4.5V \le DV_{CC} \le 5.5V$ $I_{OH} = -32mA$					$T_A = +85°C$
			$2.7V \le DV_{CC} < 4.5V$ $I_{OH} = -14.5mA$					
			$4.5V \le DV_{CC} \le 5.5V$ $I_{OH} = -30mA$					$T_A = +105°C$
			$2.7V \le DV_{CC} < 4.5V$ $I_{OH} = -14mA$					
	V_{OH3}	3mA type	$4.5V \le V_{CC} \le 5.5V$ $I_{OH} = -3mA$	V_{CC} - 0.5	-	V_{CC}	V	
			$2.7V \le V_{CC} < 4.5V$ $I_{OH} = -1.5mA$					
"L" level output voltage	V_{OL4}	4mA type	$4.5V \le (D)V_{CC} \le 5.5V$ $I_{OL} = +4mA$	-	-	0.4	V	
			$2.7V \le (D)V_{CC} < 4.5V$ $I_{OL} = +1.7mA$					
	V_{OL30}	High Drive type*	$4.5V \le DV_{CC} \le 5.5V$ $I_{OL} = +52mA$	-	-	0.5	V	$T_A = -40°C$
			$2.7V \le DV_{CC} < 4.5V$ $I_{OL} = +22mA$					
			$4.5V \le DV_{CC} \le 5.5V$ $I_{OL} = +39mA$					$T_A = +25°C$
			$2.7V \le DV_{CC} < 4.5V$ $I_{OL} = +18mA$					
			$4.5V \le DV_{CC} \le 5.5V$ $I_{OL} = +32mA$					$T_A = +85°C$
			$2.7V \le DV_{CC} < 4.5V$ $I_{OL} = +14mA$					
			$4.5V \le DV_{CC} \le 5.5V$ $I_{OL} = +30mA$					$T_A = +105°C$
			$2.7V \le DV_{CC} < 4.5V$ $I_{OL} = +13.5mA$					
	V_{OL3}	3mA type	$2.7V \le V_{CC} < 5.5V$ $I_{OL} = +3mA$	-	-	0.4	V	
	V_{OLD}	DEBUG I/F	$V_{CC} = 2.7V$ $I_{OL} = +25mA$	0	-	0.25	V	

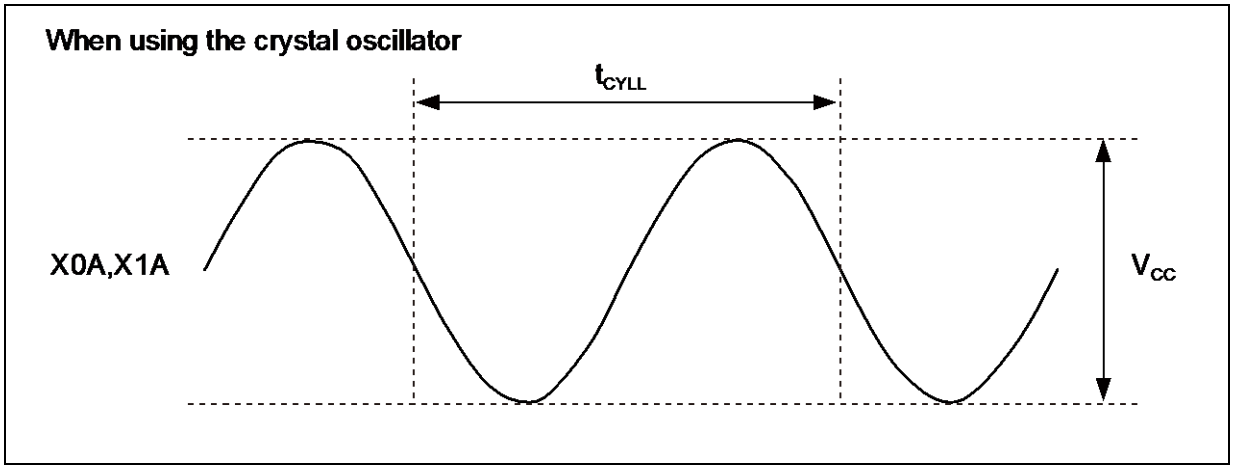
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{IL}	Pnn_m	$V_{SS} < V_I < V_{CC}$ $AV_{SS} < V_I <$ AV_{CC}, AVRH	- 1	-	+ 1	µA	Single port pin except high current output I/O for SMC
		P08_m	$DV_{SS} < V_I < DV_{CC}$ $AV_{SS} < V_I <$ AV_{CC}, AVRH	- 3	-	+ 3	µA	
Total LCD leak current	$\Sigma\|I_{ILCD}\|$	All SEG/ COM pin	V_{CC} = 5.0V	-	0.5	10	µA	Maximum leakage current of all LCD pins
Internal LCD divide resistance	R_{LCD}	Between V3 and V2, V2 and V1, V1 and V0	V_{CC} = 5.0V	6.25	12.5	25	kΩ	
Pull-up resistance value	R_{PU}	Pnn_m	V_{CC} = 5.0V ±10%	25	50	100	kΩ	
Pull-down resistance value	R_{DOWN}	P08_m	V_{CC} = 5.0V ±10%	25	50	100	kΩ	
Input capacitance	C_{IN}	Other than C, Vcc, Vss, DVcc DVss, AVcc, AVss, AVRH, P08_m	-	-	5	15	pF	
		P08_m	-	-	15	30	pF	

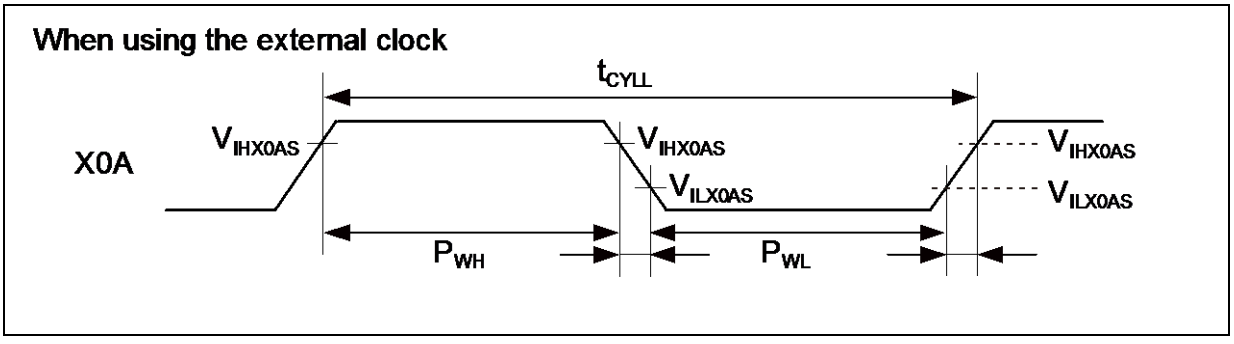
*: In the case of driving stepping motor directly or high current outputs, set "1" to the bit in the Port High Drive Register (PHDRnn:HDx="1").

14.4.2 Sub Clock Input Characteristics

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When using an oscillation circuit
			-	-	-	100	kHz	When using an opposite phase external clock
		X0A	-	-	-	50	kHz	When using a single phase external clock
Input clock cycle	t_{CYLL}	-	-	10	-	-	µs	
Input clock pulse width	-	-	P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	30	-	70	%	





14.4.8 USART Timing

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C, C_L=50pF)

Parameter	Symbol	Pin name	Conditions	4.5V ≤ V_{CC} < 5.5V		2.7V ≤ V_{CC} < 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock mode	$4t_{CLKP1}$	-	$4t_{CLKP1}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn, SOTn		- 20	+ 20	- 30	+ 30	ns
SOT → SCK ↑ delay time	t_{OVSHI}	SCKn, SOTn		$N \times t_{CLKP1}$ – 20*	-	$N \times t_{CLKP1}$ – 30*	-	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKn, SINn		t_{CLKP1} + 45	-	t_{CLKP1} + 55	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKn, SINn		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKn	External shift clock mode	t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn, SOTn		-	$2t_{CLKP1}$ + 45	-	$2t_{CLKP1}$ + 55	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKn, SINn		$t_{CLKP1}/2$ + 10	-	$t_{CLKP1}/2$ + 10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKn, SINn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK fall time	t_F	SCKn		-	20	-	20	ns
SCK rise time	t_R	SCKn		-	20	-	20	ns

Notes:

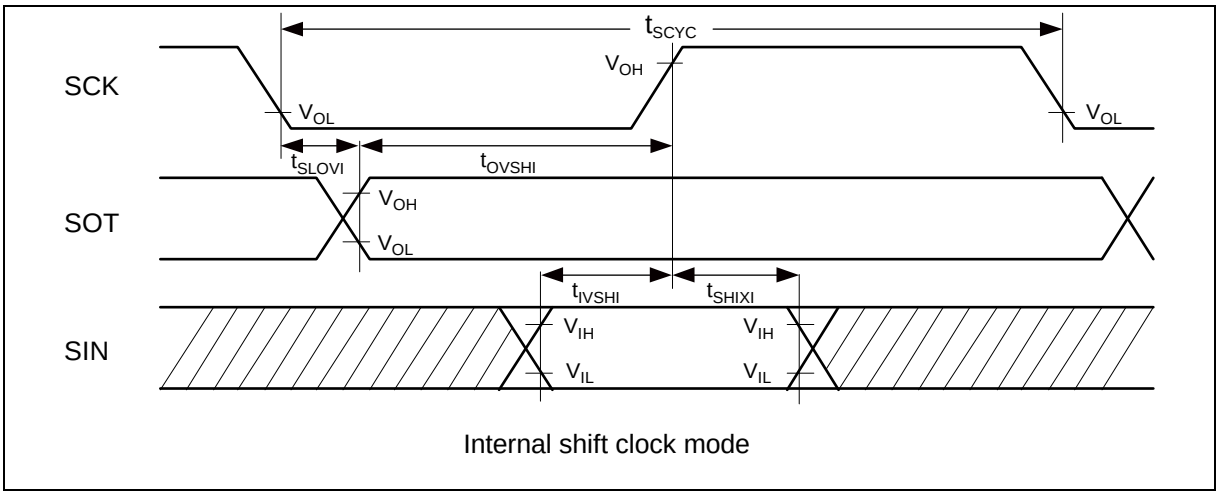
- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB96600 series HARDWARE MANUAL”.
- t_{CLKP1} indicates the peripheral clock 1 (CLKP1), Unit: ns
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKn and SOTn_R is not guaranteed.

*: Parameter N depends on t_{SCYC} and can be calculated as follows:

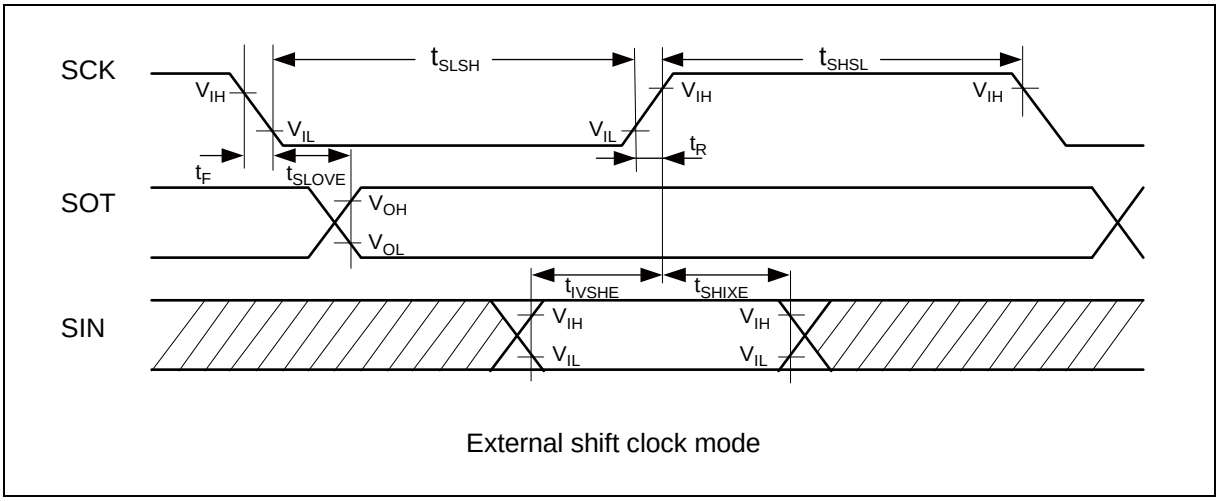
- If $t_{SCYC} = 2 \times k \times t_{CLKP1}$, then N = k, where k is an integer > 2
- If $t_{SCYC} = (2 \times k + 1) \times t_{CLKP1}$, then N = k + 1, where k is an integer > 1

Examples:

t_{SCYC}	N
$4 \times t_{CLKP1}$	2
$5 \times t_{CLKP1}$, $6 \times t_{CLKP1}$	3
$7 \times t_{CLKP1}$, $8 \times t_{CLKP1}$	4
…	…



Internal shift clock mode



External shift clock mode

14.7 Low Voltage Detection Function Characteristics

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Detected voltage[*1]	V_{DL0}	CILCR:LVL = 0000_B	2.70	2.90	3.10	V
	V_{DL1}	CILCR:LVL = 0001_B	2.79	3.00	3.21	V
	V_{DL2}	CILCR:LVL = 0010_B	2.98	3.20	3.42	V
	V_{DL3}	CILCR:LVL = 0011_B	3.26	3.50	3.74	V
	V_{DL4}	CILCR:LVL = 0100_B	3.45	3.70	3.95	V
	V_{DL5}	CILCR:LVL = 0111_B	3.73	4.00	4.27	V
	V_{DL6}	CILCR:LVL = 1001_B	3.91	4.20	4.49	V
Power supply voltage change rate[*2]	dV/dt	-	- 0.004	-	+ 0.004	V/µs
Hysteresis width	V_{HYS}	CILCR:LVHYS=0	-	-	50	mV
		CILCR:LVHYS=1	80	100	120	mV
Stabilization time	$T_{LVDSTAB}$	-	-	-	75	µs
Detection delay time	t_d	-	-	-	30	µs

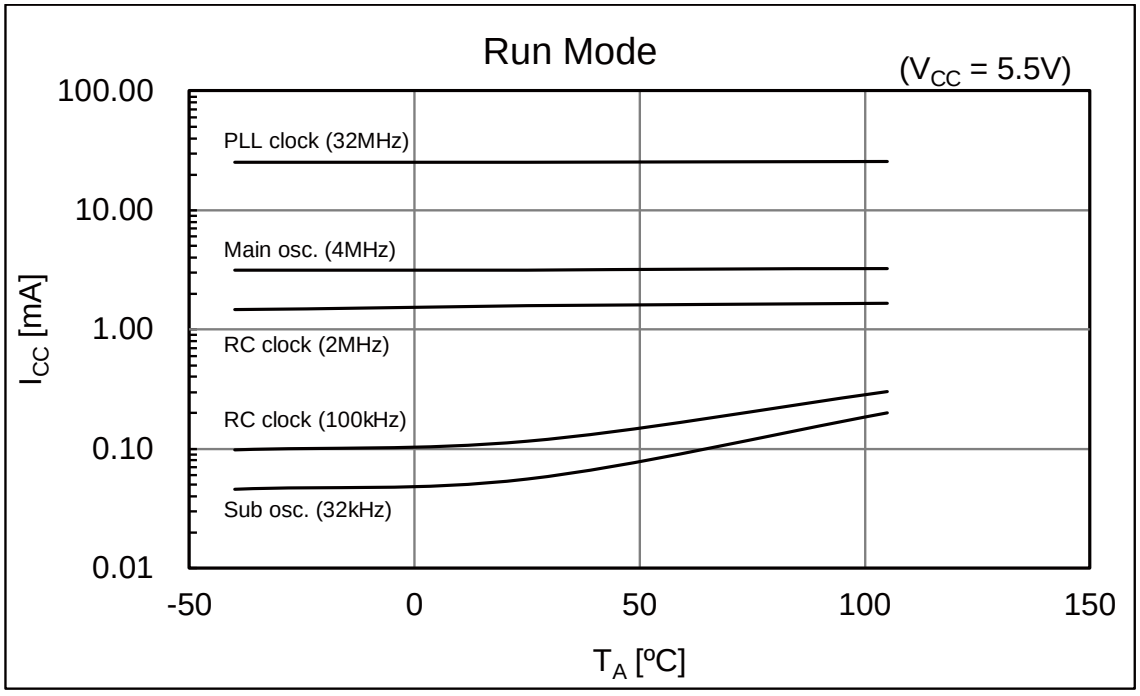
[*1]: If the power supply voltage fluctuates within the time less than the detection delay time (t_d), there is a possibility that the low voltage detection will occur or stop after the power supply voltage passes the detection range.

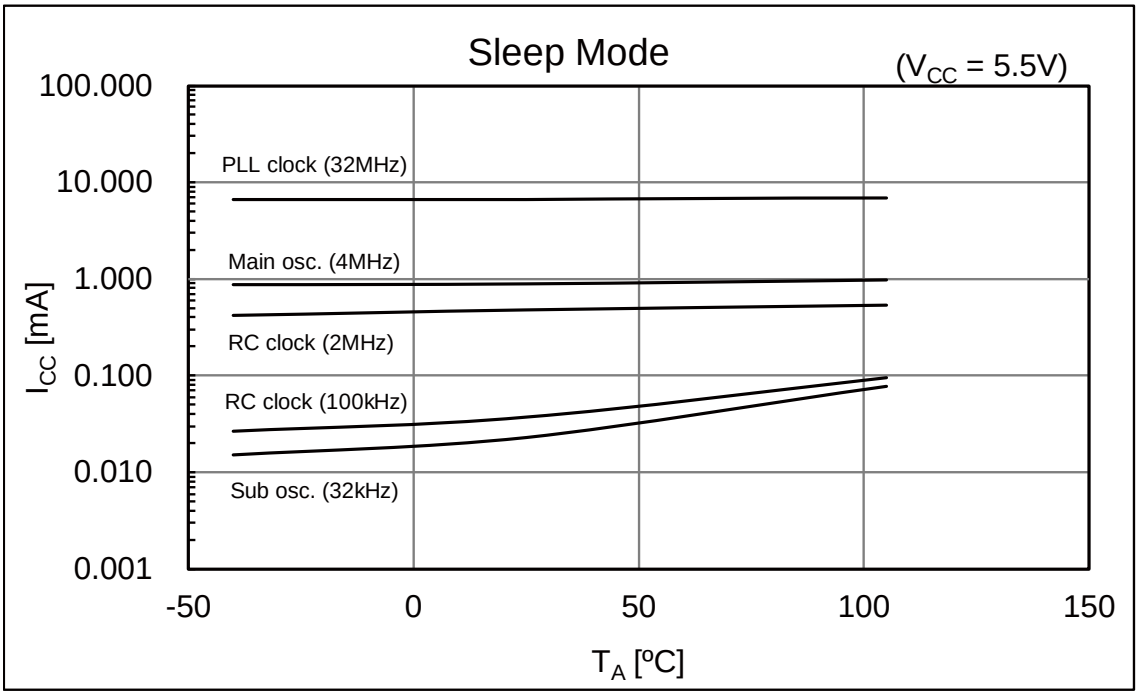
[*2]: In order to perform the low voltage detection at the detection voltage (V_{DLX}), be sure to suppress fluctuation of the power supply voltage within the limits of the change ration of power supply voltage.

15. Example Characteristics

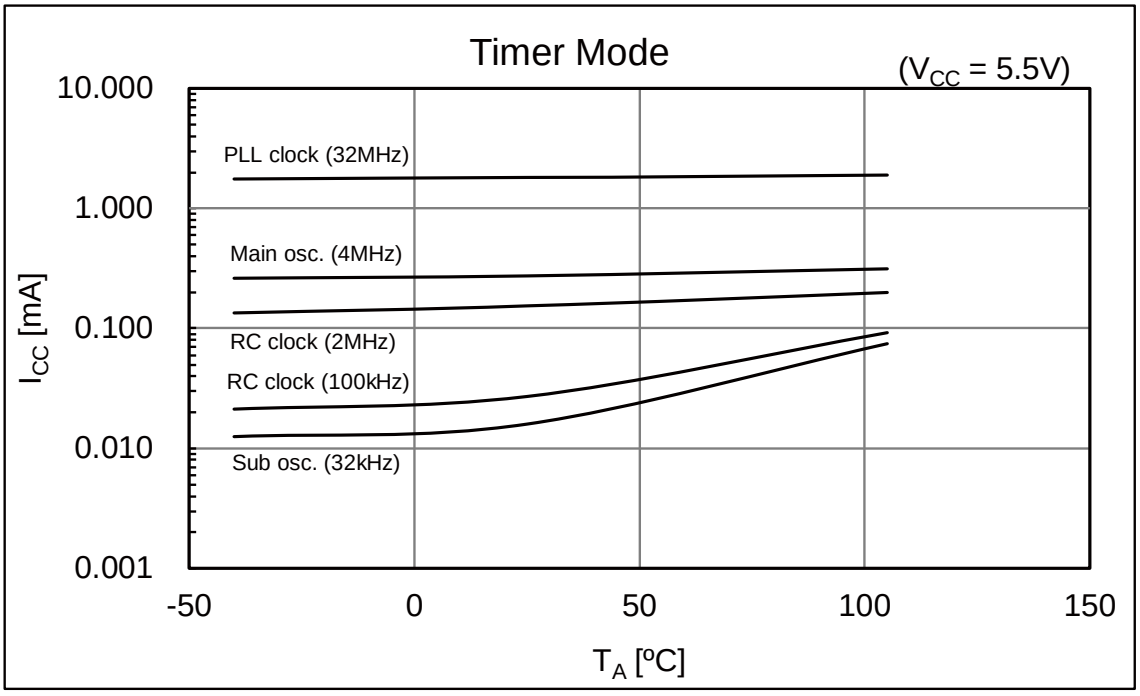
This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

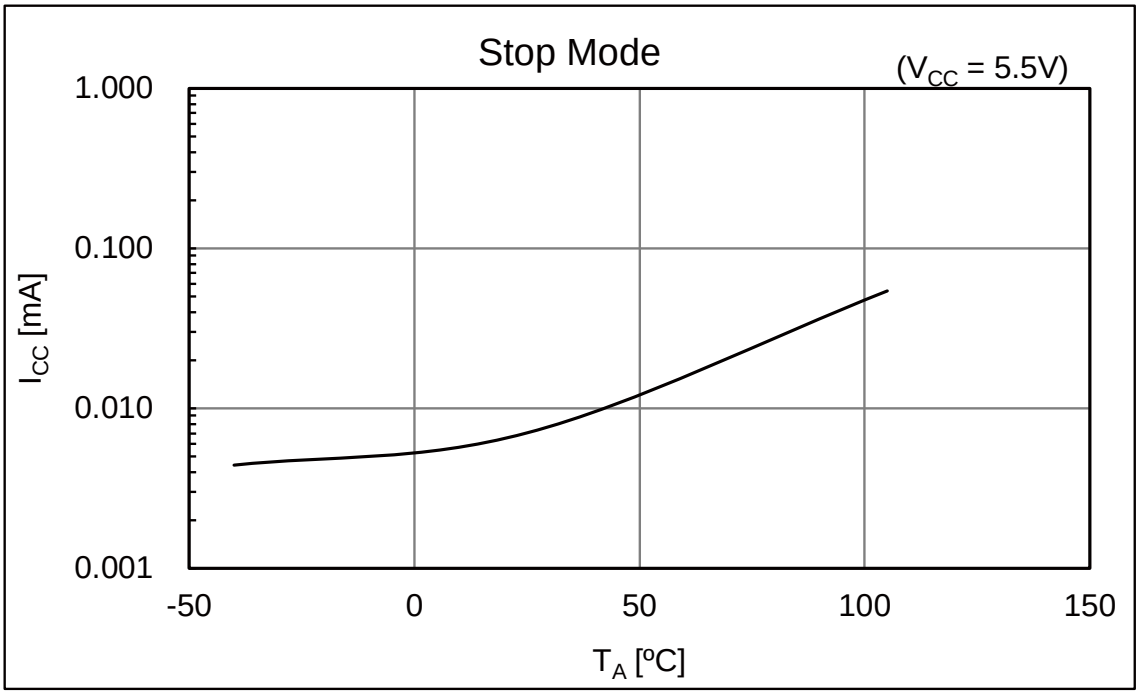
■MB96F675





■MB96F675


Timer Mode
(V_{CC} = 5.5V)
10.000
1.000
0.100
0.010
0.001
I_{CC} [mA]
PLL clock (32MHz)
Main osc. (4MHz)
RC clock (2MHz)
RC clock (100kHz)
Sub osc. (32kHz)
-50
0
50
100
150
T_A [ºC]


Stop Mode
(V_{CC} = 5.5V)
1.000
0.100
0.010
0.001
I_{CC} [mA]
-50
0
50
100
150
T_A [ºC]

■Used setting

Mode	Selected Source Clock	Clock/Regulator and FLASH Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32MHz
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4MHz
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2MHz
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100kHz
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32kHz
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
Timer mode	PLL	CLKMC = 4MHz, CLKPLL = 32MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	Main osc.	CLKMC = 4MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock fast	CLKMC = 2MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock slow	CLKMC = 100kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
	Sub osc.	CLKMC = 32 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode

18. Major Changes

Spansion Publication Number: MB96670_DS704-00001

Page	Section	Change Results
Revision 2.0		
4	FEATURES	Changed the description of “LCD Controller” On-chip drivers for internal divider resistors or external divider resistors → Internal divider resistors or external divider resistors
		Changed the description of “External Interrupts” Interrupt mask and pending bit per channel → Interrupt mask bit per channel
9	PIN DESCRIPTION	Deleted Pin name WOT
27 to 30	HANDLING PRECAUTIONS	Added a section
33	HANDLING DEVICES	Changed the description in “11. SMC power supply pins” To avoid this, VCC must always be powered on before DVCC. → To avoid this, VCC must always be powered on before DVCC. DVcc/DVss must be applied when using SMC I/O pin as GPIO.
35	ELECTRICAL CHARACTERISTICS 1. Absolute Maximum Ratings	Changed the annotation *2 It is required that AVCC does not exceed VCC and that the voltage at the analog inputs does not exceed AVCC when the power is switched on. → It is required that AVCC does not exceed VCC, DVCC and that the voltage at the analog inputs does not exceed AVCC when the power is switched on.
39	3. DC Characteristics (1) Current Rating	Changed the Conditions for ICCSRCH CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz, → CLKS1/2 = CLKP1/2 = CLKRC = 2MHz,
		Changed the Conditions for ICCSRCL CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz → CLKS1/2 = CLKP1/2 = CLKRC = 100kHz
		Changed the Conditions for ICCTPLL PLL Timer mode with CLKP1 = 32MHz → PLL Timer mode with CLKPLL = 32MHz
		Changed the Value of “Power supply current in Timer modes” ICCTPLL Typ: 2480µA → 1800µA (TA = +25°C) Max: 2710µA → 2245µA (TA = +25°C) Max: 3955µA → 3140µA (TA = +105°C)
		Changed the Conditions for ICCTRCL RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKPLL, CLKMC and CLKSC stopped) → RC Timer mode with CLKRC = 100kHz (CLKPLL, CLKMC and CLKSC stopped)