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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	F ² MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I ² C, LINbus, SCI, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f673rbpmc-gse2

■ Built-in On Chip Debugger (OCD)

- One-wire debug tool interface
- Break function:
 - Hardware break: 6 points (shared with code event)
 - Software break: 4096 points
- Event function
 - Code event: 6 points (shared with hardware break)
 - Data event: 6 points
 - Event sequencer: 2 levels + reset
- Execution time measurement function
- Trace function: 42 branches
- Security function

■ Flash Memory

- Dual operation flash allowing reading of one Flash bank while programming or erasing the other bank
- Command sequencer for automatic execution of programming algorithm and for supporting DMA for programming of the Flash Memory
- Supports automatic programming, Embedded Algorithm
- Write/Erase/Erase-Suspend/Resume commands
- A flag indicating completion of the automatic algorithm
- Erase can be performed on each sector individually
- Sector protection
- Flash Security feature to protect the content of the Flash
- Low voltage detection during Flash erase or write

Contents

1. Product Lineup	6
2. Block Diagram	7
3. Pin Assignment	8
4. Pin Description	9
5. Pin Circuit Type	11
6. I/O Circuit Type	13
7. Memory Map	19
8. RAMSTART Addresses	20
9. User ROM Memory Map For Flash Devices	21
10. Serial Programming Communication Interface	22
11. Interrupt Vector Table	23
12. Handling Precautions	27
12.1 Precautions for Product Design	27
12.2 Precautions for Package Mounting	28
12.3 Precautions for Use Environment	29
13. Handling Devices	30
13.1 Latch-up prevention	30
13.2 Unused pins handling	30
13.3 External clock usage	31
13.3.1 Single phase external clock for Main oscillator	31
13.3.2 Single phase external clock for Sub oscillator	31
13.3.3 Opposite phase external clock	31
13.4 Notes on PLL clock mode operation	31
13.5 Power supply pins (Vcc/Vss)	31
13.6 Crystal oscillator and ceramic resonator circuit	32
13.7 Turn on sequence of power supply to A/D converter and analog inputs	32
13.8 Pin handling when not using the A/D converter	32
13.9 Notes on Power-on	32
13.10 Stabilization of power supply voltage	32
13.11 SMC power supply pins	32
13.12 Serial communication	32
13.13 Mode Pin (MD)	32
14. Electrical Characteristics	33
14.1 Absolute Maximum Ratings	33
14.2 Recommended Operating Conditions	35
14.3 DC Characteristics	36
14.3.1 Current Rating	36
14.3.2 Pin Characteristics	39
14.4 AC Characteristics	42
14.4.1 Main Clock Input Characteristics	42
14.4.2 Sub Clock Input Characteristics	43
14.4.3 Built-in RC Oscillation Characteristics	44
14.4.4 Internal Clock Timing	44
14.4.5 Operating Conditions of PLL	45
14.4.6 Reset Input	45
14.4.7 Power-on Reset Timing	46

14.4.8 USART Timing	47
14.4.9 External Input Timing	49
14.4.10 I ² C Timing.....	50
14.5 A/D Converter.....	51
14.5.1 Electrical Characteristics for the A/D Converter	51
14.5.2 Accuracy and Setting of the A/D Converter Sampling Time	52
14.5.3 Definition of A/D Converter Terms	53
14.6 High Current Output Slew Rate	55
14.7 Low Voltage Detection Function Characteristics	56
14.8 Flash Memory Write/Erase Characteristics	58
15. Example Characteristics	59
16. Ordering Information	62
17. Package Dimension	63
18. Major Changes	65
Document History.....	67

1. Product Lineup

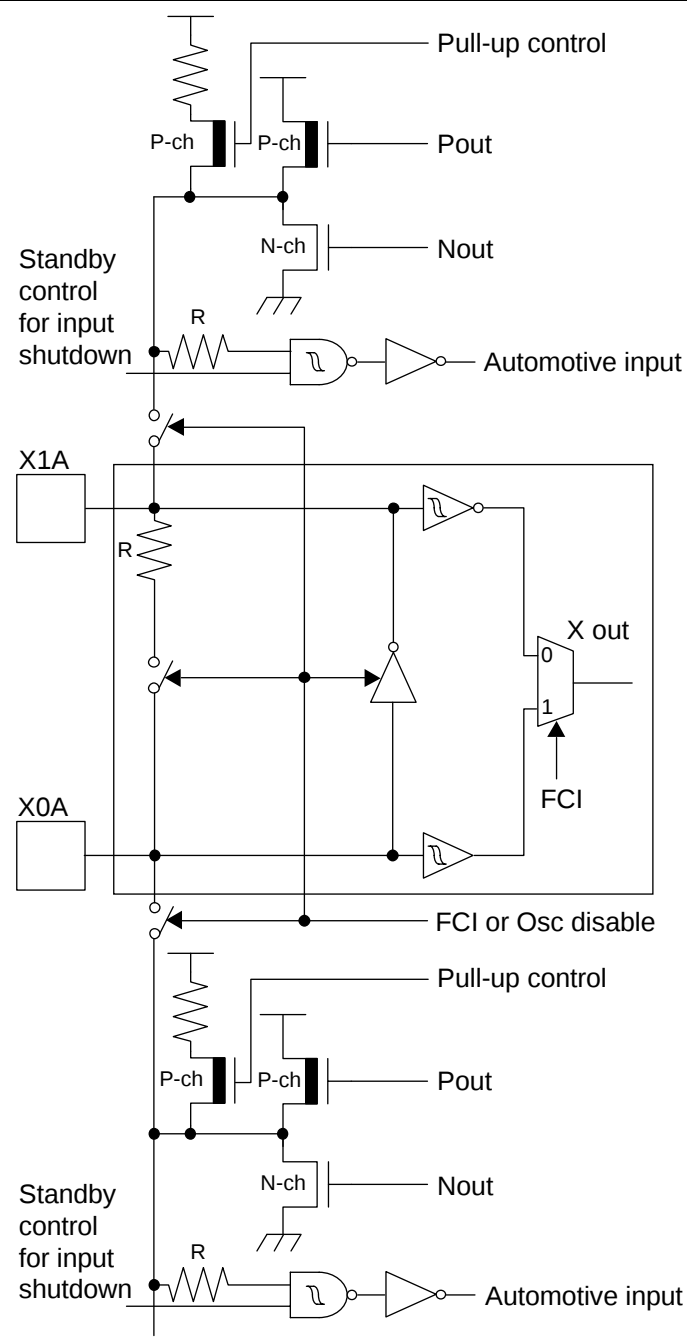
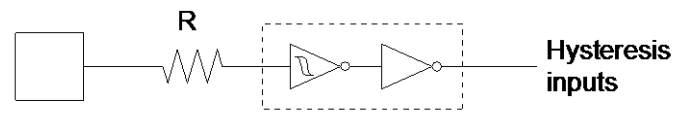
Features		MB96670	Remark
Product Type		Flash Memory Product	
Subclock		Subclock can be set by software	
Dual Operation Flash Memory	RAM	-	
64.5KB + 32KB	4KB	MB96F673R, MB96F673A	Product Options R: MCU with CAN A: MCU without CAN
128.5KB + 32KB	4KB	MB96F675R, MB96F675A	
Package		LQFP-64 FPT-64P-M23/M24	
DMA		2ch	
USART		2ch	LIN-USART 0/1
	with automatic LIN-Header transmission/reception	Yes (only 1ch)	LIN-USART 0
	with 16 byte RX- and TX-FIFO	No	
I ² C		1ch	I ² C 0
8/10-bit A/D Converter		12ch	AN 8/9/12/13/16 to 23
	with Data Buffer	No	
	with Range Comparator	Yes	
	with Scan Disable	Yes	
	with ADC Pulse Detection	Yes	
16-bit Reload Timer (RLT)		3ch	RLT 1/2/6
16-bit Free-Running Timer (FRT)		2ch	FRT 0/1
16-bit Input Capture Unit (ICU)		4ch (2 channels for LIN-USART)	ICU 0/1/4/5 ICU 0/1 for LIN-USART
8/16-bit Programmable Pulse Generator (PPG)		4ch (16-bit) / 8ch (8-bit)	PPG 0 to 3
	with Timing point capture	Yes	
	with Start delay	No	
	with Ramp	No	
CAN Interface		1ch	CAN 0 32 Message Buffers
Stepping Motor Controller (SMC)		2ch	SMC 0/1
External Interrupts (INT)		7ch	INT 0 to 4/6/7
Non-Maskable Interrupt (NMI)		1ch	
Sound Generator (SG)		1ch	SG 0
LCD Controller		4COM × 24SEG	COM 0 to 3 SEG 3 to 6/8 to 11/ 19 to 21/23/30/36 to 39/42/45 to 47/54 to 56
Real Time Clock (RTC)		1ch	
I/O Ports		48 (Dual clock mode) 50 (Single clock mode)	
Clock Calibration Unit (CAL)		1ch	
Clock Output Function		2ch	
Low Voltage Detection Function		Yes	Low voltage detection function can be disabled by software
Hardware Watchdog Timer		Yes	
On-chip RC-oscillator		Yes	
On-chip Debugger		Yes	

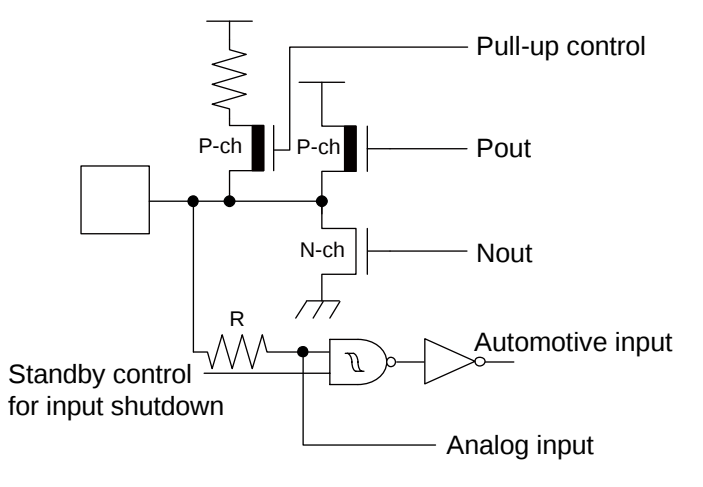
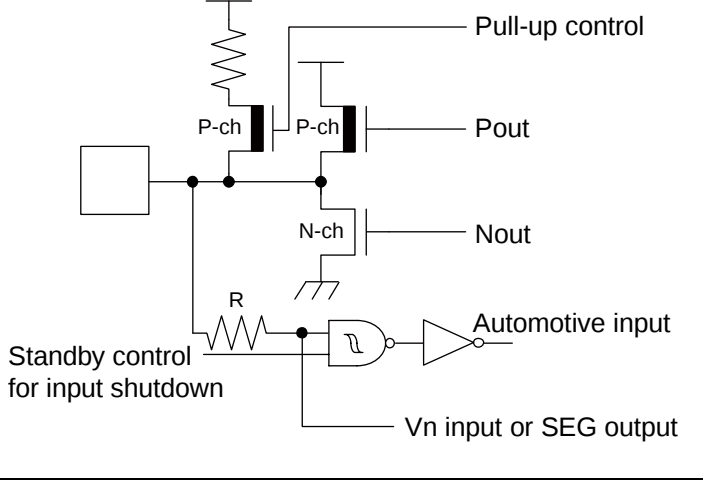
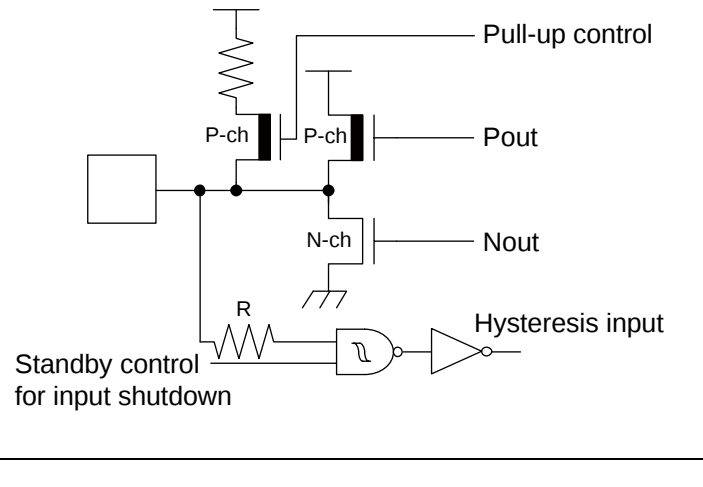
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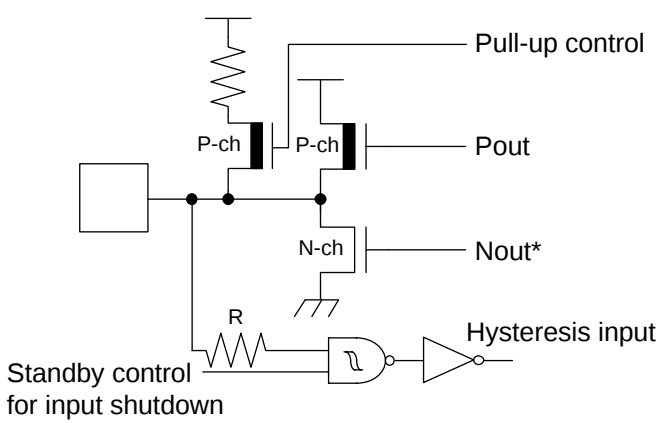
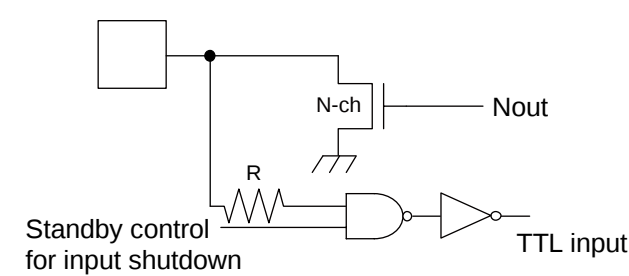
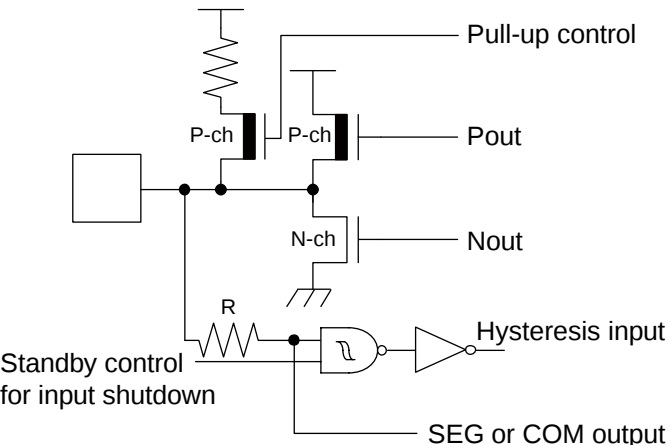
All signals of the peripheral function in each product cannot be allocated by limiting the pins of package.
It is necessary to use the port relocate function of the general I/O port according to your function use.

Pin no.	I/O circuit type*	Pin name
33	N	P04_5 / SCL0
34	O	DEBUG I/F
35	H	P17_0
36	C	MD
37	A	X0
38	A	X1
39	Supply	Vss
40	B	P04_0 / X0A
41	B	P04_1 / X1A
42	C	RSTX
43	J	P11_7 / SEG3 / IN0_R
44	J	P11_0 / COM0
45	J	P11_1 / COM1 / PPG0_R
46	J	P11_2 / COM2 / PPG1_R
47	J	P11_3 / COM3 / PPG2_R
48	J	P12_0 / SEG4 / IN1_R
49	J	P12_1 / SEG5 / TIN1_R / PPG0_B
50	J	P12_2 / SEG6 / TOT1_R / PPG1_B
51	J	P12_4 / SEG8
52	J	P12_5 / SEG9 / TIN2_R / PPG2_B
53	J	P12_6 / SEG10 / TOT2_R / PPG3_B
54	J	P12_7 / SEG11 / INT1_R
55	J	P01_1 / SEG21 / CKOT1
56	J	P01_3 / SEG23
57	L	P03_0 / SEG36 / V0
58	L	P03_1 / SEG37 / V1
59	L	P03_2 / SEG38 / V2
60	L	P03_3 / SEG39 / V3
61	M	P03_4 / RX0 / INT4
62	H	P03_5 / TX0
63	H	P03_6 / INT0 / NMI
64	Supply	Vcc

*: See "I/O CIRCUIT TYPE" for details on the I/O circuit types.

Type	Circuit	Remarks
B	 The diagram illustrates a low-speed oscillation circuit shared with GPIO functionality. It features a pull-up control, Pout, Nout, and automotive input. A feedback resistor R is connected to the input. The circuit is controlled by standby control for input shutdown and FCI or Osc disable signals. The output is labeled X out, and the feedback is labeled FCI.	Low-speed oscillation circuit shared with GPIO functionality: • Feedback resistor = approx. 5.0MΩ • GPIO functionality selectable (CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$), Automotive input with input shutdown function and programmable pull-up resistor)
C	 The diagram shows a CMOS hysteresis input pin. It includes a pull-up resistor R and a hysteresis input.	CMOS hysteresis input pin

Type	Circuit	Remarks
K	 Pull-up control P-ch Pout N-ch Nout R Standby control for input shutdown Automotive input Analog input	• CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$) • Automotive input with input shutdown function • Programmable pull-up resistor • Analog input
L	 Pull-up control P-ch Pout N-ch Nout R Standby control for input shutdown Automotive input Vn input or SEG output	• CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$) • Automotive input with input shutdown function • Programmable pull-up resistor • Vn input or SEG output
M	 Pull-up control P-ch Pout N-ch Nout R Standby control for input shutdown Hysteresis input	• CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor

Type	Circuit	Remarks
N	 The diagram shows a CMOS output stage. A pull-up resistor is connected to Vcc and the output node. A P-channel MOSFET (P-ch) is connected between the output node and Vcc, controlled by a 'Pull-up control' signal. An N-channel MOSFET (N-ch) is connected between the output node and ground, controlled by 'Pout'. The output is labeled 'Pout'. A second N-channel MOSFET (N-ch) is connected between the output node and ground, controlled by 'Nout*'. A 'Standby control for input shutdown' signal is connected to the input of a NAND gate through a resistor 'R'. The other input of the NAND gate is connected to the output node. The output of the NAND gate is connected to an inverter, which provides the 'Hysteresis input'.	• CMOS level output ($I_{OL} = 3\text{mA}$, $I_{OH} = -3\text{mA}$) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor *: N-channel transistor has slew rate control according to I²C spec, irrespective of usage.
O	 The diagram shows an open-drain output stage. An N-channel MOSFET (N-ch) is connected between the output node and ground, controlled by 'Nout'. A pull-up resistor 'R' is connected to Vcc and the output node. A 'Standby control for input shutdown' signal is connected to the input of a NAND gate through the resistor 'R'. The other input of the NAND gate is connected to the output node. The output of the NAND gate is connected to an inverter, which provides the 'TTL input'.	• Open-drain I/O • Output 25mA, $V_{CC} = 2.7\text{V}$ • TTL input
P	 The diagram shows a CMOS output stage similar to Type N. A pull-up resistor is connected to Vcc and the output node. A P-channel MOSFET (P-ch) is connected between the output node and Vcc, controlled by a 'Pull-up control' signal. An N-channel MOSFET (N-ch) is connected between the output node and ground, controlled by 'Pout'. Another N-channel MOSFET (N-ch) is connected between the output node and ground, controlled by 'Nout'. The output is labeled 'Nout'. A 'Standby control for input shutdown' signal is connected to the input of a NAND gate through a resistor 'R'. The other input of the NAND gate is connected to the output node. The output of the NAND gate is connected to an inverter, which provides the 'Hysteresis input'. The output of the inverter is also labeled 'SEG or COM output'.	• CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$) • CMOS hysteresis inputs with input shutdown function • Programmable pull-up resistor • SEG or COM output

8. RAMSTART Addresses

Devices	Bank 0 RAM size	RAMSTART0
MB96F673 MB96F675	4KB	00:7200 _H

9. User ROM Memory Map For Flash Devices

		MB96F673	MB96F675	
CPU mode address	Flash memory mode address	Flash size 64.5KB + 32KB	Flash size 128.5KB + 32KB	
FF:FFFFH FF:0000H	3F:FFFFH 3F:0000H	SA39 - 64KB	SA39 - 64KB	Bank A of Flash A
FE:FFFFH FE:0000H	3E:FFFFH 3E:0000H	Reserved	SA38 - 64KB	
FD:FFFFH			Reserved	
DF:A000H				
DF:9FFFH DF:8000H	1F:9FFFH 1F:8000H	SA4 - 8KB	SA4 - 8KB	Bank B of Flash A
DF:7FFFH DF:6000H	1F:7FFFH 1F:6000H	SA3 - 8KB	SA3 - 8KB	
DF:5FFFH DF:4000H	1F:5FFFH 1F:4000H	SA2 - 8KB	SA2 - 8KB	
DF:3FFFH DF:2000H	1F:3FFFH 1F:2000H	SA1 - 8KB	SA1 - 8KB	
DF:1FFFH DF:0000H	1F:1FFFH 1F:0000H	SAS - 512B*	SAS - 512B*	
DE:FFFFH DE:0000H		Reserved	Reserved	Bank A of Flash A

*: Physical address area of SAS-512B is from DF:0000H to DF:01FFH.

Others (from DF:0200H to DF:1FFFH) is mirror area of SAS-512B.

Sector SAS contains the ROM configuration block RCBA at CPU address DF:0000H -DF:01FFH.

SAS can not be used for E²PROM emulation.

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
81	2B8 _H	-	-	81	Reserved
82	2B4 _H	-	-	82	Reserved
83	2B0 _H	-	-	83	Reserved
84	2AC _H	-	-	84	Reserved
85	2A8 _H	-	-	85	Reserved
86	2A4 _H	-	-	86	Reserved
87	2A0 _H	-	-	87	Reserved
88	29C _H	-	-	88	Reserved
89	298 _H	FRT0	Yes	89	Free-Running Timer 0
90	294 _H	FRT1	Yes	90	Free-Running Timer 1
91	290 _H	-	-	91	Reserved
92	28C _H	-	-	92	Reserved
93	288 _H	RTC0	No	93	Real Time Clock
94	284 _H	CAL0	No	94	Clock Calibration Unit
95	280 _H	SG0	No	95	Sound Generator 0
96	27C _H	IIC0	Yes	96	I ² C interface 0
97	278 _H	-	-	97	Reserved
98	274 _H	ADC0	Yes	98	A/D Converter 0
99	270 _H	-	-	99	Reserved
100	26C _H	-	-	100	Reserved
101	268 _H	LINR0	Yes	101	LIN USART 0 RX
102	264 _H	LINT0	Yes	102	LIN USART 0 TX
103	260 _H	LINR1	Yes	103	LIN USART 1 RX
104	25C _H	LINT1	Yes	104	LIN USART 1 TX
105	258 _H	-	-	105	Reserved
106	254 _H	-	-	106	Reserved
107	250 _H	-	-	107	Reserved
108	24C _H	-	-	108	Reserved
109	248 _H	-	-	109	Reserved
110	244 _H	-	-	110	Reserved
111	240 _H	-	-	111	Reserved
112	23C _H	-	-	112	Reserved
113	238 _H	-	-	113	Reserved
114	234 _H	-	-	114	Reserved
115	230 _H	-	-	115	Reserved
116	22C _H	-	-	116	Reserved
117	228 _H	-	-	117	Reserved
118	224 _H	-	-	118	Reserved
119	220 _H	-	-	119	Reserved
120	21C _H	-	-	120	Reserved

13. Handling Devices

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator and ceramic resonator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on Power-on
- Stabilization of power supply voltage
- SMC power supply pins
- Serial communication
- Mode Pin (MD)

13.1 Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC} , AV_{RH}) exceed the digital power-supply voltage.

13.2 Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register $PIER = 0$).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. To prevent latch-up, they must therefore be pulled up or pulled down through resistors which should be more than $2k\Omega$.

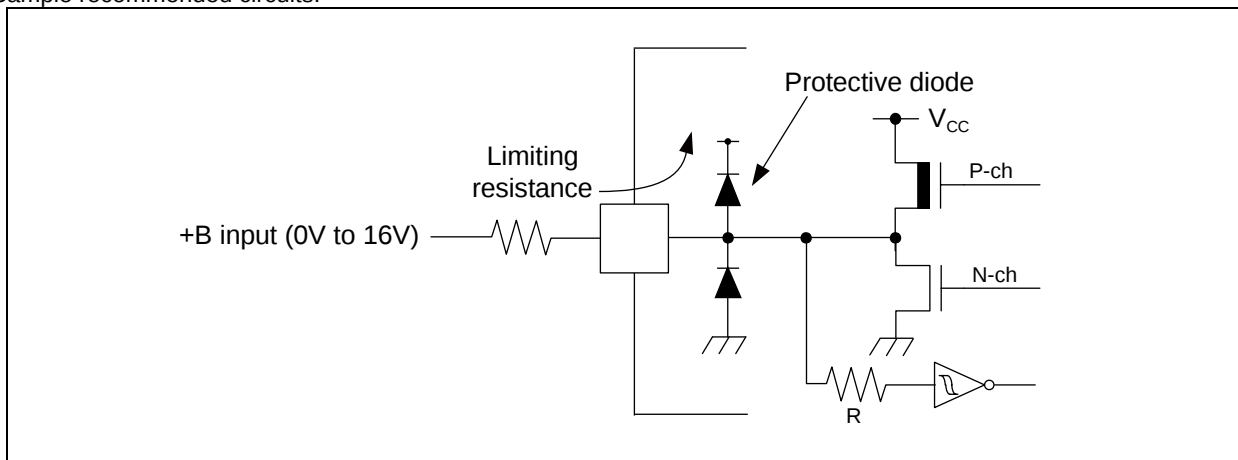
Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit	Remarks
			Min	Max		
Power supply voltage ^{*1}	V _{CC}	-	V _{SS} - 0.3	V _{SS} + 6.0	V	
Analog power supply voltage ^{*1}	AV _{CC}	-	V _{SS} - 0.3	V _{SS} + 6.0	V	V _{CC} = AV _{CC} ^{*2}
Analog reference voltage ^{*1}	AVRH	-	V _{SS} - 0.3	V _{SS} + 6.0	V	AV _{CC} ≥ AVRH, AVRH ≥ AV _{SS}
SMC Power supply ^{*1}	DV _{CC}	-	V _{SS} - 0.3	V _{SS} + 6.0	V	V _{CC} = AV _{CC} = DV _{CC} ^{*2}
LCD power supply voltage ^{*1}	V0 to V3	-	V _{SS} - 0.3	V _{SS} + 6.0	V	V0 to V3 must not exceed V _{CC}
Input voltage ^{*1}	V _I	-	V _{SS} - 0.3	V _{SS} + 6.0	V	V _I ≤ (D)V _{CC} + 0.3V ^{*3}
Output voltage ^{*1}	V _O	-	V _{SS} - 0.3	V _{SS} + 6.0	V	V _O ≤ (D)V _{CC} + 0.3V ^{*3}
Maximum Clamp Current	I _{CLAMP}	-	-4.0	+4.0	mA	Applicable to general purpose I/O pins ^{*4}
Total Maximum Clamp Current	Σ I _{CLAMP}	-	-	16	mA	Applicable to general purpose I/O pins ^{*4}
"L" level maximum output current	I _{OL}	-	-	15	mA	Normal port
	I _{OLSMC}	T _A = -40°C	-	52	mA	High current port
		T _A = +25°C	-	39	mA	
		T _A = +85°C	-	32	mA	
		T _A = +105°C	-	30	mA	
"L" level average output current	I _{OLAV}	-	-	4	mA	Normal port
	I _{OLAVSMC}	T _A = -40°C	-	40	mA	High current port
		T _A = +25°C	-	30	mA	
		T _A = +85°C	-	25	mA	
		T _A = +105°C	-	23	mA	
"L" level maximum overall output current	ΣI _{OL}	-	-	34	mA	Normal port
	ΣI _{OLSMC}	-	-	180	mA	High current port
"L" level average overall output current	ΣI _{OLAV}	-	-	17	mA	Normal port
	ΣI _{OLAVSMC}	-	-	90	mA	High current port
"H" level maximum output current	I _{OH}	-	-	-15	mA	Normal port
	I _{OHSMC}	T _A = -40°C	-	-52	mA	High current port
		T _A = +25°C	-	-39	mA	
		T _A = +85°C	-	-32	mA	
		T _A = +105°C	-	-30	mA	
"H" level average output current	I _{OHAV}	-	-	-4	mA	Normal port
	I _{OHAVSMC}	T _A = -40°C	-	-40	mA	High current port
		T _A = +25°C	-	-30	mA	
		T _A = +85°C	-	-25	mA	
		T _A = +105°C	-	-23	mA	
"H" level maximum overall output current	ΣI _{OH}	-	-	-34	mA	Normal port
	ΣI _{OHSMC}	-	-	-180	mA	High current port
"H" level average overall output current	ΣI _{OHAV}	-	-	-17	mA	Normal port
	ΣI _{OHAVSMC}	-	-	-90	mA	High current port
Power consumption ^{*5}	P _D	T _A = +105°C	-	281 ^{*6}	mW	
Operating ambient temperature	T _A	-	-40	+105	°C	
Storage temperature	T _{STG}	-	-55	+150	°C	

- ^{*1}: This parameter is based on $V_{SS} = AV_{SS} = DV_{SS} = 0V$.
- ^{*2}: AV_{CC} and V_{CC} and DV_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} , DV_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.
- ^{*3}: V_I and V_O should not exceed $V_{CC} + 0.3V$. V_I should also not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/Output voltages of high current ports depend on DV_{CC} . Input/Output voltages of standard ports depend on V_{CC} .
- ^{*4}: Applicable to all general purpose I/O pins (Pnn_m).
- Use within recommended operating conditions.
 - Use at DC voltage (current).
 - The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
 - The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
 - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
 - Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0V), the power supply is provided from the pins, so that incomplete operation may result.
 - Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset.
 - The DEBUG I/F pin has only a protective diode against V_{SS} . Hence it is only permitted to input a negative clamping current (4mA). For protection against positive input voltages, use an external clamping diode which limits the input voltage to maximum 6.0V.
 - Sample recommended circuits:



- ^{*5}: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:

$$P_D = P_{IO} + P_{INT}$$

$$P_{IO} = \sum (V_{OL} \times I_{OL} + V_{OH} \times I_{OH})$$
 (I/O load power dissipation, sum is performed on all I/O ports)

$$P_{INT} = V_{CC} \times (I_{CC} + I_A)$$
 (internal power dissipation)
 I_{CC} is the total core current consumption into V_{CC} as described in the "DC characteristics" and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming.
 I_A is the analog current consumption into AV_{CC} .
- ^{*6}: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

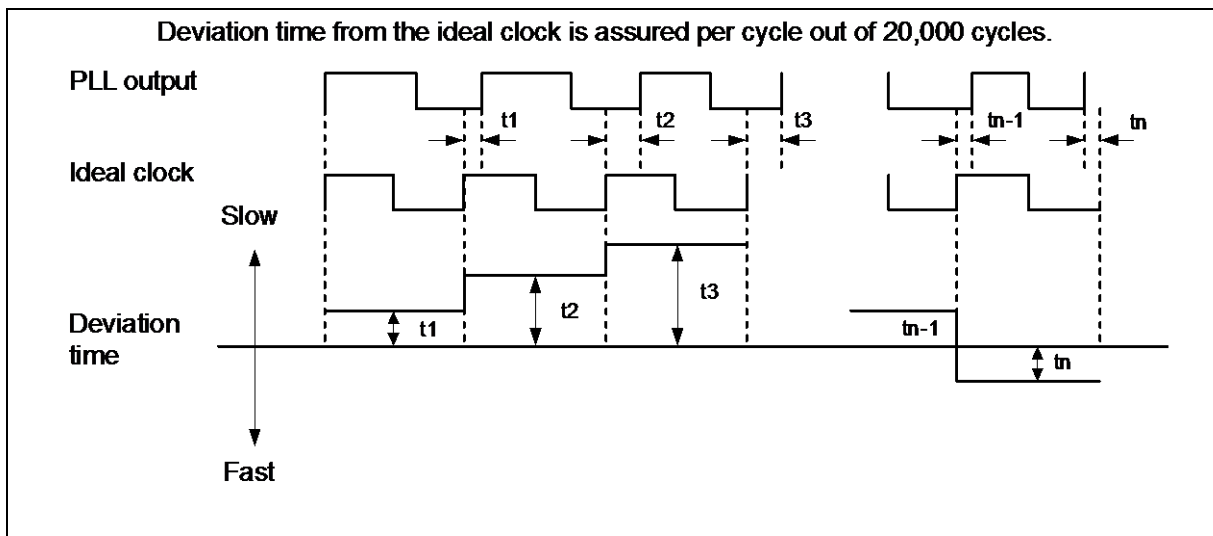
WARNING

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

14.4.5 Operating Conditions of PLL

($V_{CC} = AV_{CC} = DV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = DV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$)

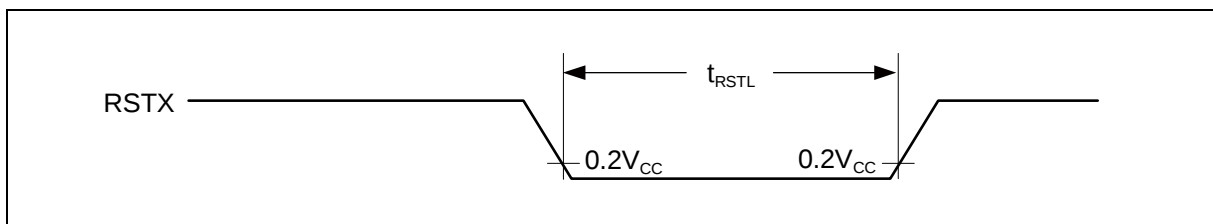
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time	t_{LOCK}	1	-	4	ms	For CLKMC = 4MHz
PLL input clock frequency	f_{PLLI}	4	-	8	MHz	
PLL oscillation clock frequency	f_{CLKVCO}	56	-	108	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL phase jitter	t_{PSKEW}	-5	-	+5	ns	For CLKMC (PLL input clock) $\geq 4MHz$



14.4.6 Reset Input

($V_{CC} = AV_{CC} = DV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = DV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Reset input time	t_{RSTL}	RSTX	10	-	μs
Rejection of reset input time			1	-	μs



14.4.8 USART Timing
 $(V_{CC} = AV_{CC} = DV_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = -40^{\circ}C \text{ to } +105^{\circ}C, C_L=50pF)$

Parameter	Symbol	Pin name	Conditions	4.5V ≤ V _{CC} < 5.5V		2.7V ≤ V _{CC} < 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t _{SCYC}	SCKn	Internal shift clock mode	4t _{CLKP1}	-	4t _{CLKP1}	-	ns
SCK ↓ → SOT delay time	t _{SLOVI}	SCKn, SOTn		- 20	+ 20	- 30	+ 30	ns
SOT → SCK ↑ delay time	t _{OVSHI}	SCKn, SOTn		N × t _{CLKP1} - 20*	-	N × t _{CLKP1} - 30*	-	ns
SIN → SCK ↑ setup time	t _{IVSHI}	SCKn, SINn		t _{CLKP1} + 45	-	t _{CLKP1} + 55	-	ns
SCK ↑ → SIN hold time	t _{SHIXI}	SCKn, SINn		0	-	0	-	ns
Serial clock "L" pulse width	t _{SLSH}	SCKn	External shift clock mode	t _{CLKP1} + 10	-	t _{CLKP1} + 10	-	ns
Serial clock "H" pulse width	t _{SHSL}	SCKn		t _{CLKP1} + 10	-	t _{CLKP1} + 10	-	ns
SCK ↓ → SOT delay time	t _{SLOVE}	SCKn, SOTn		-	2t _{CLKP1} + 45	-	2t _{CLKP1} + 55	ns
SIN → SCK ↑ setup time	t _{IVSHE}	SCKn, SINn		t _{CLKP1} /2 + 10	-	t _{CLKP1} /2 + 10	-	ns
SCK ↑ → SIN hold time	t _{SHIXE}	SCKn, SINn		t _{CLKP1} + 10	-	t _{CLKP1} + 10	-	ns
SCK fall time	t _F	SCKn		-	20	-	20	ns
SCK rise time	t _R	SCKn		-	20	-	20	ns

Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in "MB96600 series HARDWARE MANUAL".
- t_{CLKP1} indicates the peripheral clock 1 (CLKP1), Unit: ns
- These characteristics only guarantee the same relocate port number.
For example, the combination of SCKn and SOTn_R is not guaranteed.

*: Parameter N depends on t_{SCYC} and can be calculated as follows:

- If t_{SCYC} = 2 × k × t_{CLKP1}, then N = k, where k is an integer > 2
- If t_{SCYC} = (2 × k + 1) × t_{CLKP1}, then N = k + 1, where k is an integer > 1

Examples:

t _{scyc}	N
4 × t _{CLKP1}	2
5 × t _{CLKP1} , 6 × t _{CLKP1}	3
7 × t _{CLKP1} , 8 × t _{CLKP1}	4
...	...

14.8 Flash Memory Write/Erase Characteristics

($V_{CC} = AV_{CC} = DV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = DV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$)

Parameter		Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Sector erase time	Large Sector	-	-	1.6	7.5	s	Includes write time prior to internal erase.
	Small Sector	-	-	0.4	2.1	s	
	Security Sector	-	-	0.31	1.65	s	
Word (16-bit) write time		-	-	25	400	μs	Not including system-level overhead time.
Chip erase time		-	-	5.11	25.05	s	Includes write time prior to internal erase.

Note:

While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.

To put it concrete, change the external power in the range of change ration of power supply voltage ($-0.004V/\mu s$ to $+0.004V/\mu s$) after the external power falls below the detection voltage (V_{DLX})^{*1}.

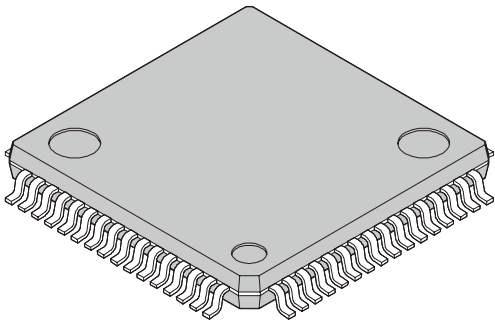
Write/Erase cycles and data hold time

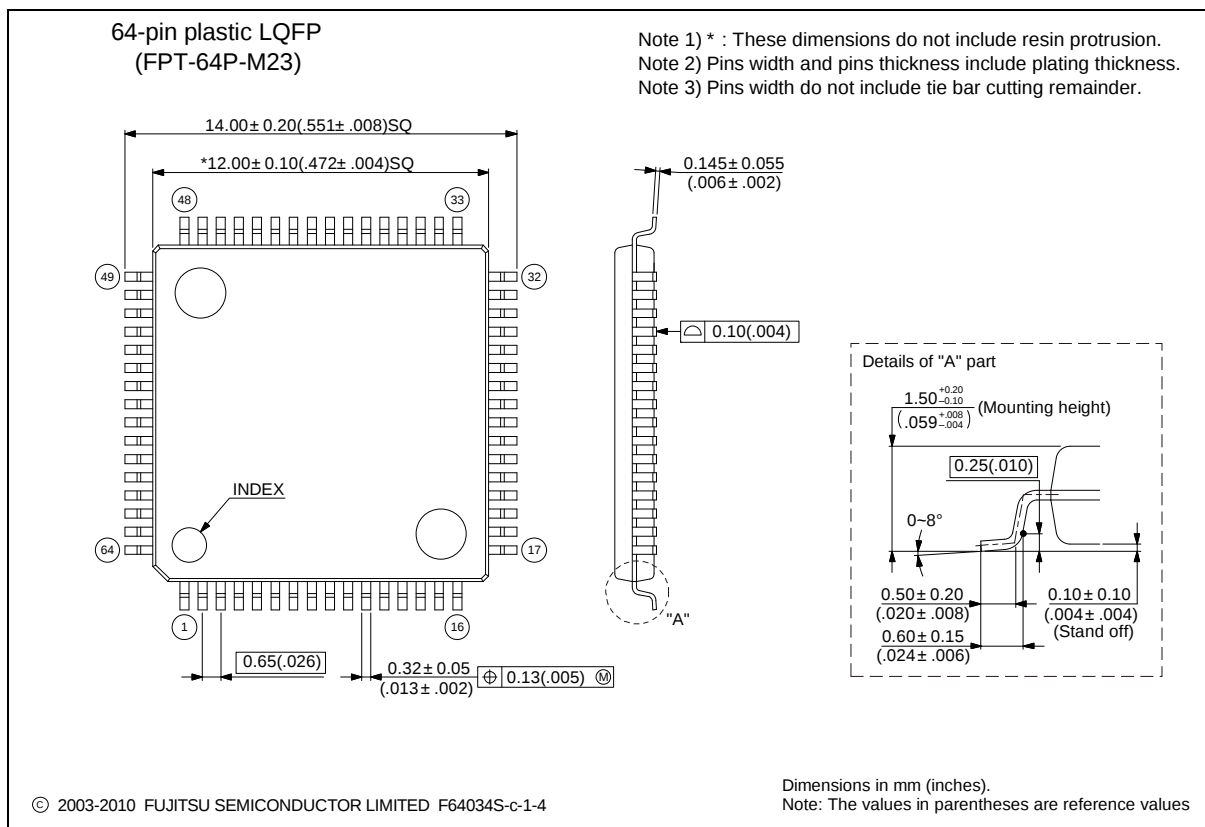
Write/Erase cycles (cycle)	Data hold time (year)
1,000	20^{*2}
10,000	10^{*2}
100,000	5^{*2}

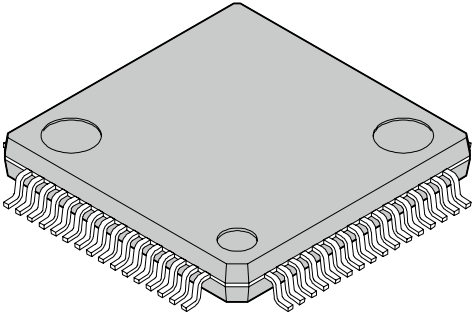
^{*1}: See "Low Voltage Detection Function Characteristics".

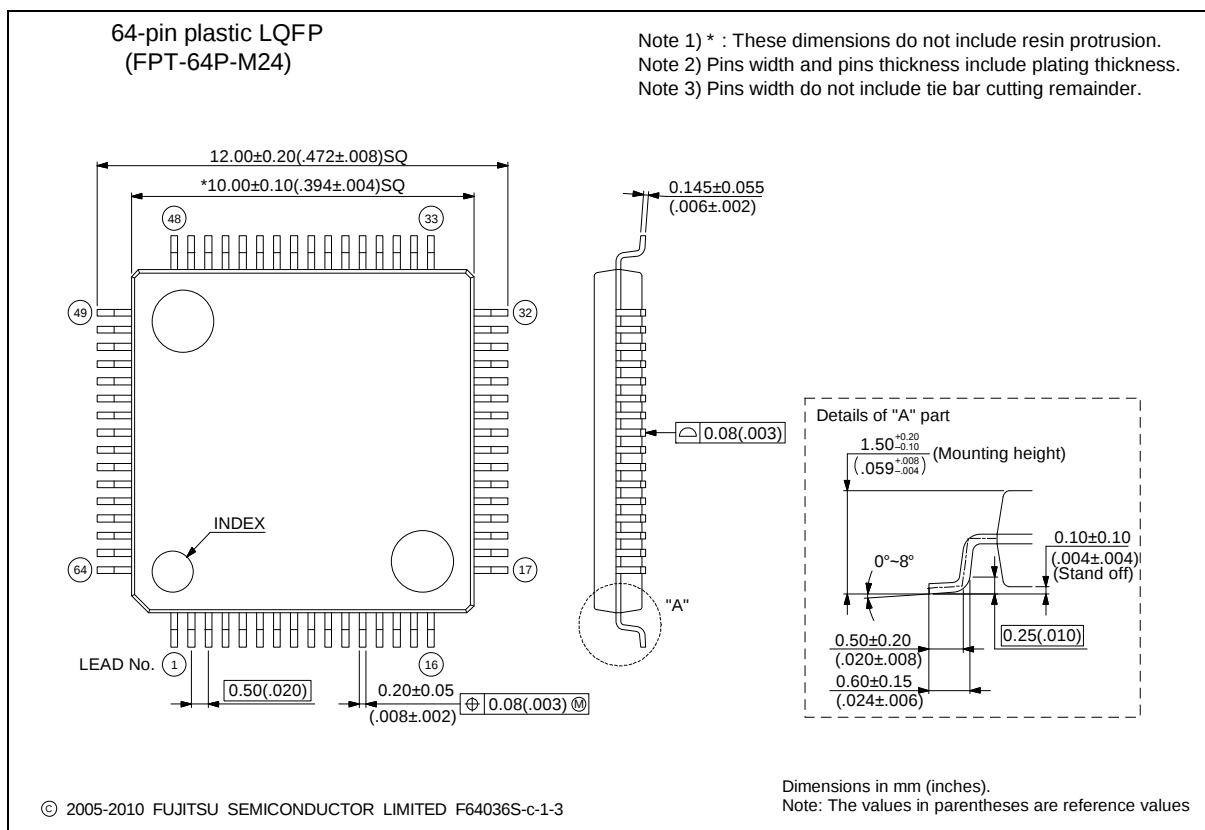
^{*2}: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at $+85^{\circ}C$).

17. Package Dimension

 64-pin plastic LQFP (FPT-64P-M23)	Lead pitch	0.65 mm
	Package width × package length	12.0 × 12.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.47 g
	Code (Reference)	P-LQFP64-12 × 12-0.65



64-pin plastic LQFP  (FPT-64P-M24)	Lead pitch	0.50 mm
	Package width × package length	10.0 × 10.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32 g
	Code (Reference)	P-LFQFP64-10×10-0.50



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