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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	F ² MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SCI, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f675abpmc-gse2

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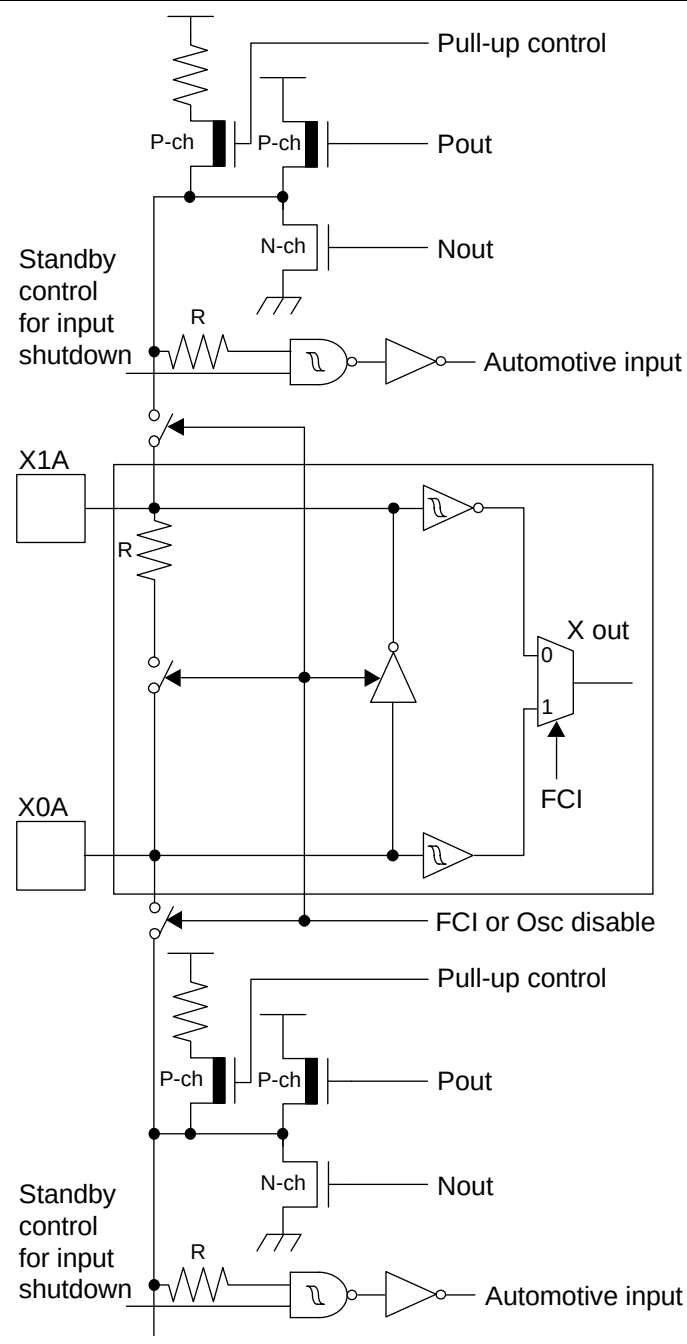
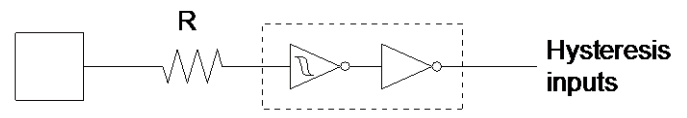
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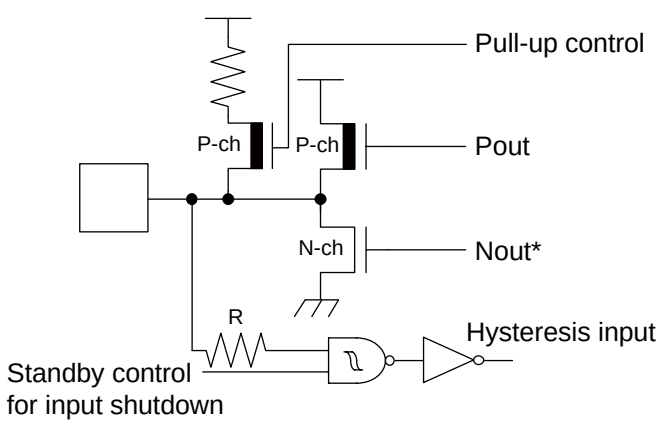
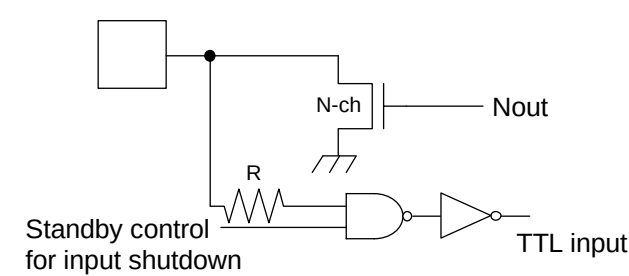
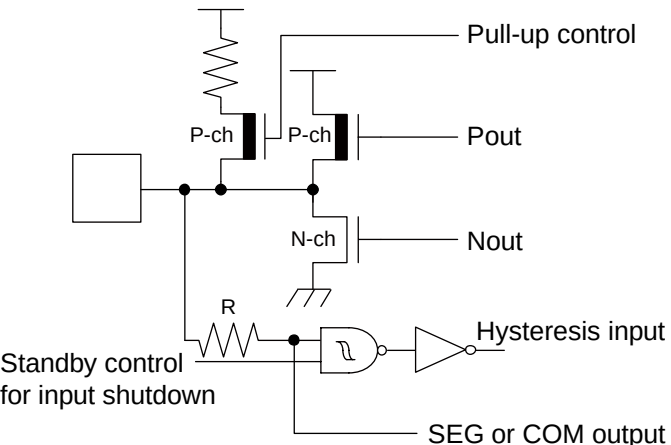
5. Pin Circuit Type

Pin no.	I/O circuit type*	Pin name
1	Supply	Vss
2	F	C
3	M	P03_7 / INT1 / SIN1
4	H	P13_0 / INT2 / SOT1
5	P	P13_1 / INT3 / SCK1 / SEG42
6	J	P00_7 / SEG19 / SGO0
7	J	P01_0 / SEG20 / SGA0
8	J	P02_2 / SEG30 / CKOT0_R
9	J	P06_5 / IN1 / SEG54 / TTG1
10	J	P06_6 / TIN1 / SEG55 / IN4_R
11	J	P06_7 / TOT1 / SEG56 / IN5_R
12	K	P05_0 / AN8
13	K	P05_1 / AN9
14	Supply	AVcc
15	G	AVRH
16	Supply	AVss
17	K	P05_4 / AN12 / INT2_R / WOT_R
18	K	P05_5 / AN13
19	R	P08_0 / PWM1P0 / AN16
20	R	P08_1 / PWM1M0 / AN17
21	R	P08_2 / PWM2P0 / AN18
22	R	P08_3 / PWM2M0 / AN19
23	Supply	DVcc
24	Supply	DVss
25	R	P08_4 / PWM1P1 / AN20
26	R	P08_5 / PWM1M1 / AN21
27	R	P08_6 / PWM2P1 / AN22
28	R	P08_7 / PWM2M1 / AN23
29	P	P13_4 / SIN0 / INT6 / SEG45
30	J	P13_5 / SOT0 / ADTG / INT7 / SEG46
31	P	P13_6 / SCK0 / CKOTX0 / SEG47
32	N	P04_4 / PPG3 / SDA0

Pin no.	I/O circuit type*	Pin name
33	N	P04_5 / SCL0
34	O	DEBUG I/F
35	H	P17_0
36	C	MD
37	A	X0
38	A	X1
39	Supply	Vss
40	B	P04_0 / X0A
41	B	P04_1 / X1A
42	C	RSTX
43	J	P11_7 / SEG3 / IN0_R
44	J	P11_0 / COM0
45	J	P11_1 / COM1 / PPG0_R
46	J	P11_2 / COM2 / PPG1_R
47	J	P11_3 / COM3 / PPG2_R
48	J	P12_0 / SEG4 / IN1_R
49	J	P12_1 / SEG5 / TIN1_R / PPG0_B
50	J	P12_2 / SEG6 / TOT1_R / PPG1_B
51	J	P12_4 / SEG8
52	J	P12_5 / SEG9 / TIN2_R / PPG2_B
53	J	P12_6 / SEG10 / TOT2_R / PPG3_B
54	J	P12_7 / SEG11 / INT1_R
55	J	P01_1 / SEG21 / CKOT1
56	J	P01_3 / SEG23
57	L	P03_0 / SEG36 / V0
58	L	P03_1 / SEG37 / V1
59	L	P03_2 / SEG38 / V2
60	L	P03_3 / SEG39 / V3
61	M	P03_4 / RX0 / INT4
62	H	P03_5 / TX0
63	H	P03_6 / INT0 / NMI
64	Supply	Vcc

*: See "I/O CIRCUIT TYPE" for details on the I/O circuit types.

Type	Circuit	Remarks
B	 Low-speed oscillation circuit shared with GPIO functionality: - Feedback resistor = approx. 5.0MΩ - GPIO functionality selectable (CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$), Automotive input with input shutdown function and programmable pull-up resistor)	Low-speed oscillation circuit shared with GPIO functionality: - Feedback resistor = approx. 5.0MΩ - GPIO functionality selectable (CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$), Automotive input with input shutdown function and programmable pull-up resistor)
C	 CMOS hysteresis input pin	CMOS hysteresis input pin

Type	Circuit	Remarks
N	 The diagram shows a CMOS output stage. A pull-up resistor is connected to the output node. A P-channel MOSFET (P-ch) is connected to the output node and its gate is controlled by a 'Pull-up control' signal. An N-channel MOSFET (N-ch) is connected to the output node and its gate is controlled by a 'Standby control for input shutdown' signal. The output node is also connected to a resistor 'R' which is connected to a 'Hysteresis input' through an inverter. The output of the N-ch MOSFET is labeled 'Nout*'. The output of the P-ch MOSFET is labeled 'Pout'.	• CMOS level output ($I_{OL} = 3\text{mA}$, $I_{OH} = -3\text{mA}$) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor *: N-channel transistor has slew rate control according to I²C spec, irrespective of usage.
O	 The diagram shows an open-drain output stage. An N-channel MOSFET (N-ch) is connected to the output node and its gate is controlled by a 'Standby control for input shutdown' signal. The output node is also connected to a resistor 'R' which is connected to a 'TTL input' through an inverter. The output of the N-ch MOSFET is labeled 'Nout'.	• Open-drain I/O • Output 25mA, $V_{CC} = 2.7\text{V}$ • TTL input
P	 The diagram shows a CMOS output stage similar to Type N. A pull-up resistor is connected to the output node. A P-channel MOSFET (P-ch) is connected to the output node and its gate is controlled by a 'Pull-up control' signal. An N-channel MOSFET (N-ch) is connected to the output node and its gate is controlled by a 'Standby control for input shutdown' signal. The output node is also connected to a resistor 'R' which is connected to a 'Hysteresis input' through an inverter. The output of the N-ch MOSFET is labeled 'Nout'. The output of the P-ch MOSFET is labeled 'Pout'. The output of the inverter is labeled 'SEG or COM output'.	• CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$) • CMOS hysteresis inputs with input shutdown function • Programmable pull-up resistor • SEG or COM output

7. Memory Map

FF:FFFF _H	USER ROM*1
DE:0000 _H	Reserved
DD:FFFF _H	
10:0000 _H	Boot-ROM
0F:C000 _H	
0E:9000 _H	Peripheral
	Reserved
01:0000 _H	
00:8000 _H	ROM/RAM MIRROR
RAMSTART0*2	Internal RAM bank0
	Reserved
00:0C00 _H	
00:0380 _H	Peripheral
00:0180 _H	GPR*3
00:0100 _H	DMA
00:00F0 _H	Reserved
00:0000 _H	Peripheral

*1: For details about USER ROM area, see “User ROM Memory Map For Flash Devices” on the following pages.

*2: For RAMSTART addresses, see the table on the next page.

*3: Unused GPR banks can be used as RAM area.

GPR: General-Purpose Register

The DMA area is only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

11. Interrupt Vector Table

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	3FC _H	CALLV0	No	-	CALLV instruction
1	3F8 _H	CALLV1	No	-	CALLV instruction
2	3F4 _H	CALLV2	No	-	CALLV instruction
3	3F0 _H	CALLV3	No	-	CALLV instruction
4	3EC _H	CALLV4	No	-	CALLV instruction
5	3E8 _H	CALLV5	No	-	CALLV instruction
6	3E4 _H	CALLV6	No	-	CALLV instruction
7	3E0 _H	CALLV7	No	-	CALLV instruction
8	3DC _H	RESET	No	-	Reset vector
9	3D8 _H	INT9	No	-	INT9 instruction
10	3D4 _H	EXCEPTION	No	-	Undefined instruction execution
11	3D0 _H	NMI	No	-	Non-Maskable Interrupt
12	3CC _H	DLY	No	12	Delayed Interrupt
13	3C8 _H	RC_TIMER	No	13	RC Clock Timer
14	3C4 _H	MC_TIMER	No	14	Main Clock Timer
15	3C0 _H	SC_TIMER	No	15	Sub Clock Timer
16	3BC _H	LVDI	No	16	Low Voltage Detector
17	3B8 _H	EXTINT0	Yes	17	External Interrupt 0
18	3B4 _H	EXTINT1	Yes	18	External Interrupt 1
19	3B0 _H	EXTINT2	Yes	19	External Interrupt 2
20	3AC _H	EXTINT3	Yes	20	External Interrupt 3
21	3A8 _H	EXTINT4	Yes	21	External Interrupt 4
22	3A4 _H	-	-	22	Reserved
23	3A0 _H	EXTINT6	Yes	23	External Interrupt 6
24	39C _H	EXTINT7	Yes	24	External Interrupt 7
25	398 _H	-	-	25	Reserved
26	394 _H	-	-	26	Reserved
27	390 _H	-	-	27	Reserved
28	38C _H	-	-	28	Reserved
29	388 _H	-	-	29	Reserved
30	384 _H	-	-	30	Reserved
31	380 _H	-	-	31	Reserved
32	37C _H	-	-	32	Reserved
33	378 _H	CAN0	No	33	CAN Controller 0
34	374 _H	-	-	34	Reserved
35	370 _H	-	-	35	Reserved
36	36C _H	-	-	36	Reserved
37	368 _H	-	-	37	Reserved
38	364 _H	PPG0	Yes	38	Programmable Pulse Generator 0
39	360 _H	PPG1	Yes	39	Programmable Pulse Generator 1

13. Handling Devices

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator and ceramic resonator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on Power-on
- Stabilization of power supply voltage
- SMC power supply pins
- Serial communication
- Mode Pin (MD)

13.1 Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC} , AV_{RH}) exceed the digital power-supply voltage.

13.2 Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register $PIER = 0$).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. To prevent latch-up, they must therefore be pulled up or pulled down through resistors which should be more than $2k\Omega$.

Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

14.3 DC Characteristics

14.3.1 Current Rating

($V_{CC} = AV_{CC} = DV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = DV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Run modes ^{*1}	I _{CCPLL}	V _{CC}	PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32MHz	-	25	-	mA	T _A = +25°C
			Flash 0 wait (CLKRC and CLKSC stopped)	-	-	34	mA	T _A = +105°C
	I _{CCMAIN}		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz	-	3.5	-	mA	T _A = +25°C
			Flash 0 wait (CLKPLL, CLKSC and CLKRC stopped)	-	-	7.5	mA	T _A = +105°C
	I _{CCRCH}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz	-	1.7	-	mA	T _A = +25°C
			Flash 0 wait (CLKMC, CLKPLL and CLKSC stopped)	-	-	5.5	mA	T _A = +105°C
	I _{CCRCL}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz	-	0.15	-	mA	T _A = +25°C
			Flash 0 wait (CLKMC, CLKPLL and CLKSC stopped)	-	-	3.2	mA	T _A = +105°C
	I _{CCSUB}		Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz	-	0.1	-	mA	T _A = +25°C
			Flash 0 wait (CLKMC, CLKPLL and CLKRC stopped)	-	-	3	mA	T _A = +105°C

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks		
				Min	Typ	Max				
Power supply current in Sleep modes ^{*1}	I _{CCSPLL}	V _{CC}	PLL Sleep mode with CLK _{S1/2} = CLK _{P1/2} = 32MHz (CLK _R C and CLK _S C stopped)	-	6.5	-	mA	T _A = +25°C		
				-	-	13	mA	T _A = +105°C		
	I _{CCSMAIN}		Main Sleep mode with CLK _{S1/2} = CLK _{P1/2} = 4MHz, SMCR:LPMSS = 0 (CLK _P LL, CLK _R C and CLK _S C stopped)	-	0.9	-	mA	T _A = +25°C		
				-	-	4	mA	T _A = +105°C		
	I _{CCSRCH}		RC Sleep mode with CLK _{S1/2} = CLK _{P1/2} = CLK _R C = 2MHz, SMCR:LPMSS = 0 (CLK _M C, CLK _P LL and CLK _S C stopped)	-	0.5	-	mA	T _A = +25°C		
				-	-	3.5	mA	T _A = +105°C		
	I _{CCSRCL}		RC Sleep mode with CLK _{S1/2} = CLK _{P1/2} = CLK _R C = 100kHz (CLK _M C, CLK _P LL and CLK _S C stopped)	-	0.06	-	mA	T _A = +25°C		
				-	-	2.7	mA	T _A = +105°C		
	I _{CCSSUB}		Sub Sleep mode with CLK _{S1/2} = CLK _{P1/2} = 32kHz, (CLK _M C, CLK _P LL and CLK _R C stopped)	-	0.04	-	mA	T _A = +25°C		
				-	-	2.5	mA	T _A = +105°C		
	Power supply current in Timer modes ^{*2}		I _{CCTPLL}	V _{CC}	PLL Timer mode with CLK _P LL = 32MHz (CLK _R C and CLK _S C stopped)	-	1800	2245	μA	T _A = +25°C
						-	-	3140	μA	T _A = +105°C
I _{CCTMAIN}		Main Timer mode with CLK _M C = 4MHz, SMCR:LPMSS = 0 (CLK _P LL, CLK _R C and CLK _S C stopped)	-		285	325	μA	T _A = +25°C		
			-		-	1055	μA	T _A = +105°C		
I _{CCTRCH}		RC Timer mode with CLK _R C = 2MHz, SMCR:LPMSS = 0 (CLK _P LL, CLK _M C and CLK _S C stopped)	-		160	210	μA	T _A = +25°C		
			-		-	970	μA	T _A = +105°C		
I _{CCTRCL}		RC Timer mode with CLK _R C = 100kHz (CLK _P LL, CLK _M C and CLK _S C stopped)	-		30	70	μA	T _A = +25°C		
			-		-	820	μA	T _A = +105°C		
I _{CCTSUB}		Sub Timer mode with CLK _S C = 32kHz (CLK _M C, CLK _P LL and CLK _R C stopped)	-		25	55	μA	T _A = +25°C		
			-		-	800	μA	T _A = +105°C		

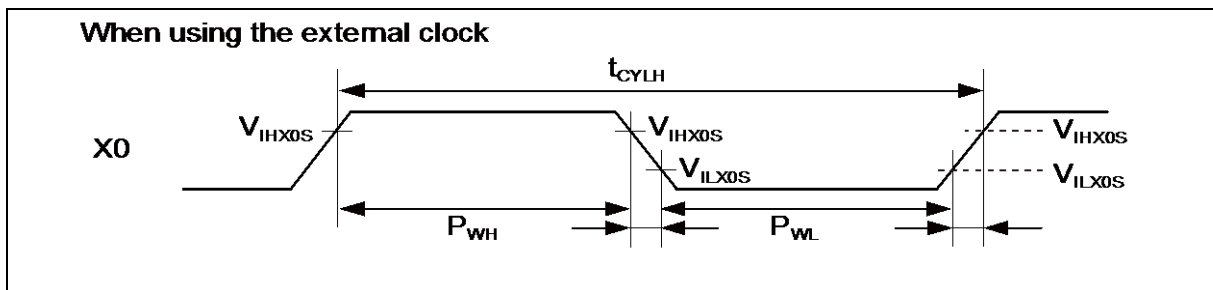
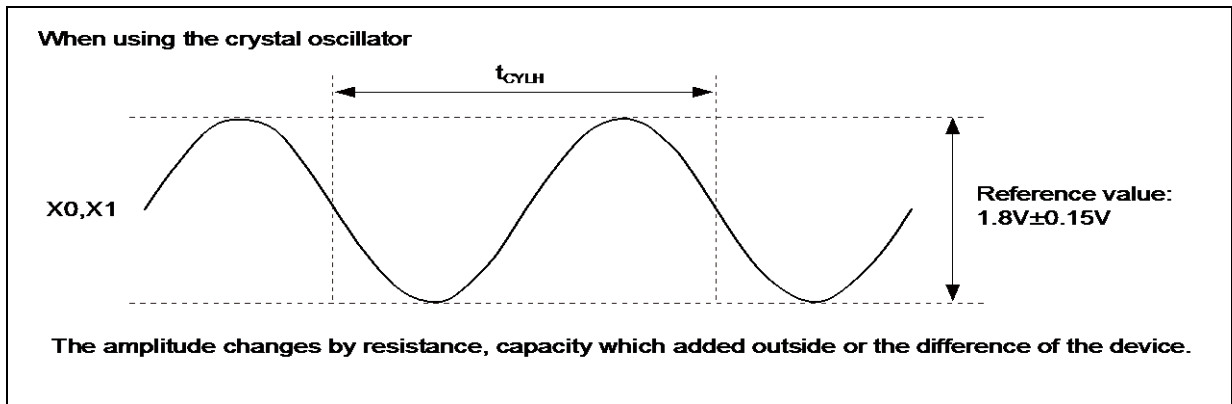
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V _{OH4}	4mA type	4.5V ≤ (D)V _{CC} ≤ 5.5V I _{OH} = -4mA	(D)V _{CC} - 0.5	-	(D)V _{CC}	V	
			2.7V ≤ (D)V _{CC} < 4.5V I _{OH} = -1.5mA					
	V _{OH30}	High Drive type*	4.5V ≤ DV _{CC} ≤ 5.5V I _{OH} = -52mA	DV _{CC} - 0.5	-	DV _{CC}	V	T _A = -40°C
			2.7V ≤ DV _{CC} < 4.5V I _{OH} = -18mA					T _A = +25°C
			4.5V ≤ DV _{CC} ≤ 5.5V I _{OH} = -39mA					T _A = +85°C
			2.7V ≤ DV _{CC} < 4.5V I _{OH} = -16mA					T _A = +105°C
			4.5V ≤ DV _{CC} ≤ 5.5V I _{OH} = -32mA					
			2.7V ≤ DV _{CC} < 4.5V I _{OH} = -14.5mA					
			4.5V ≤ DV _{CC} ≤ 5.5V I _{OH} = -30mA					
			2.7V ≤ DV _{CC} < 4.5V I _{OH} = -14mA					
	V _{OH3}	3mA type	4.5V ≤ V _{CC} ≤ 5.5V I _{OH} = -3mA	V _{CC} - 0.5	-	V _{CC}	V	
			2.7V ≤ V _{CC} < 4.5V I _{OH} = -1.5mA					
"L" level output voltage	V _{OL4}	4mA type	4.5V ≤ (D)V _{CC} ≤ 5.5V I _{OL} = +4mA	-	-	0.4	V	
			2.7V ≤ (D)V _{CC} < 4.5V I _{OL} = +1.7mA					
	V _{OL30}	High Drive type*	4.5V ≤ DV _{CC} ≤ 5.5V I _{OL} = +52mA	-	-	0.5	V	T _A = -40°C
			2.7V ≤ DV _{CC} < 4.5V I _{OL} = +22mA					T _A = +25°C
			4.5V ≤ DV _{CC} ≤ 5.5V I _{OL} = +39mA					T _A = +85°C
			2.7V ≤ DV _{CC} < 4.5V I _{OL} = +18mA					T _A = +105°C
			4.5V ≤ DV _{CC} ≤ 5.5V I _{OL} = +32mA					
			2.7V ≤ DV _{CC} < 4.5V I _{OL} = +14mA					
			4.5V ≤ DV _{CC} ≤ 5.5V I _{OL} = +30mA					
			2.7V ≤ DV _{CC} < 4.5V I _{OL} = +13.5mA					
	V _{OL3}	3mA type	2.7V ≤ V _{CC} < 5.5V I _{OL} = +3mA	-	-	0.4	V	
	V _{OLD}	DEBUG I/F	V _{CC} = 2.7V I _{OL} = +25mA	0	-	0.25	V	

14.4 AC Characteristics

14.4.1 Main Clock Input Characteristics

($V_{CC} = AV_{CC} = DV_{CC} = 2.7V$ to $5.5V$, $V_D = 1.8V \pm 0.15V$, $V_{SS} = AV_{SS} = DV_{SS} = 0V$, $T_A = -40^\circ C$ to $+105^\circ C$)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Input frequency	f_c	X0, X1	4	-	8	MHz	When using a crystal oscillator, PLL off
			-	-	8	MHz	When using an opposite phase external clock, PLL off
			4	-	8	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Input frequency	f_{FCI}	X0	-	-	8	MHz	When using a single phase external clock in "Fast Clock Input mode", PLL off
			4	-	8	MHz	When using a single phase external clock in "Fast Clock Input mode", PLL on
Input clock cycle	t_{CYLH}	-	125	-	-	ns	
Input clock pulse width	P_{WH}, P_{WL}	-	55	-	-	ns	



14.4.3 Built-in RC Oscillation Characteristics
 $(V_{CC} = AV_{CC} = DV_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = -40^{\circ}C \text{ to } +105^{\circ}C)$

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Clock frequency	f_{RC}	50	100	200	kHz	When using slow frequency of RC oscillator
		1	2	4	MHz	When using fast frequency of RC oscillator
RC clock stabilization time	t_{RCSTAB}	80	160	320	μs	When using slow frequency of RC oscillator (16 RC clock cycles)
		64	128	256	μs	When using fast frequency of RC oscillator (256 RC clock cycles)

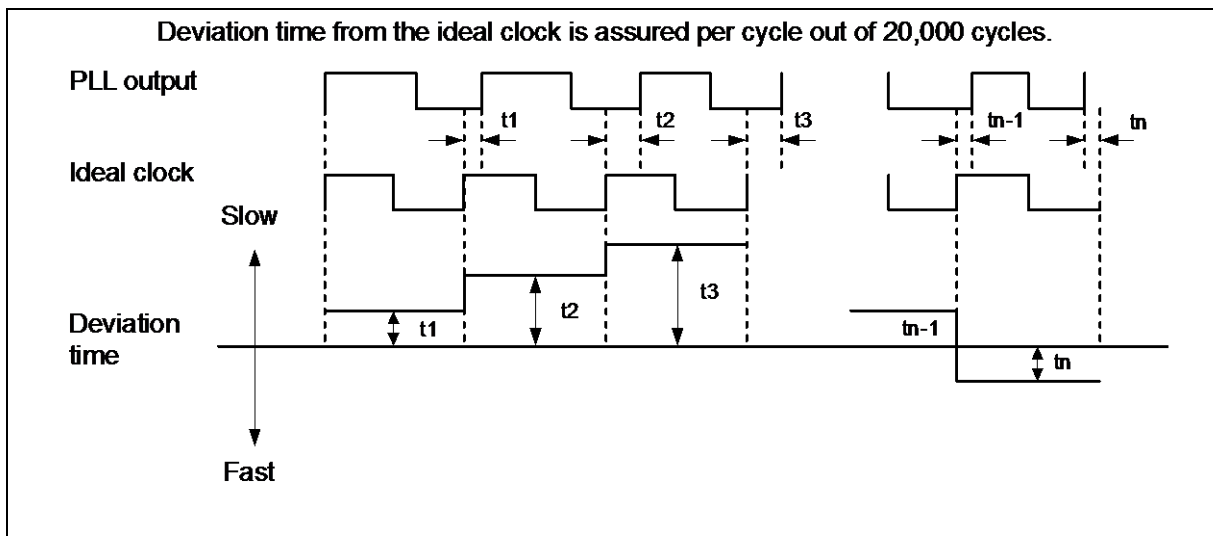
14.4.4 Internal Clock Timing
 $(V_{CC} = AV_{CC} = DV_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = -40^{\circ}C \text{ to } +105^{\circ}C)$

Parameter	Symbol	Value		Unit
		Min	Max	
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	-	54	MHz
Internal CPU clock frequency (CLKB), Internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	-	32	MHz
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	-	32	MHz

14.4.5 Operating Conditions of PLL

($V_{CC} = AV_{CC} = DV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = DV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$)

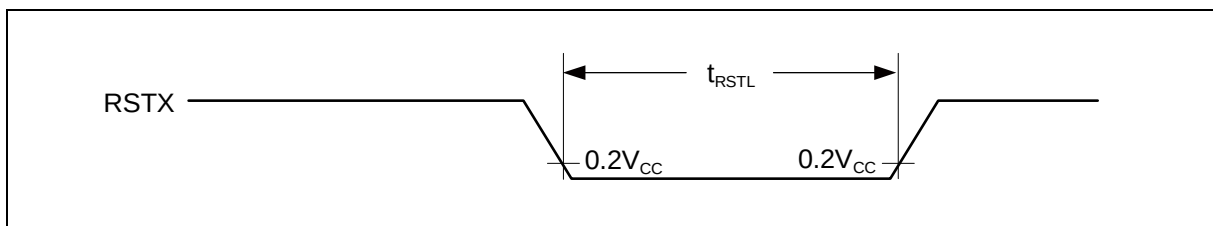
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time	t_{LOCK}	1	-	4	ms	For CLKMC = 4MHz
PLL input clock frequency	f_{PLLI}	4	-	8	MHz	
PLL oscillation clock frequency	f_{CLKVCO}	56	-	108	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL phase jitter	t_{PSKEW}	-5	-	+5	ns	For CLKMC (PLL input clock) $\geq 4MHz$

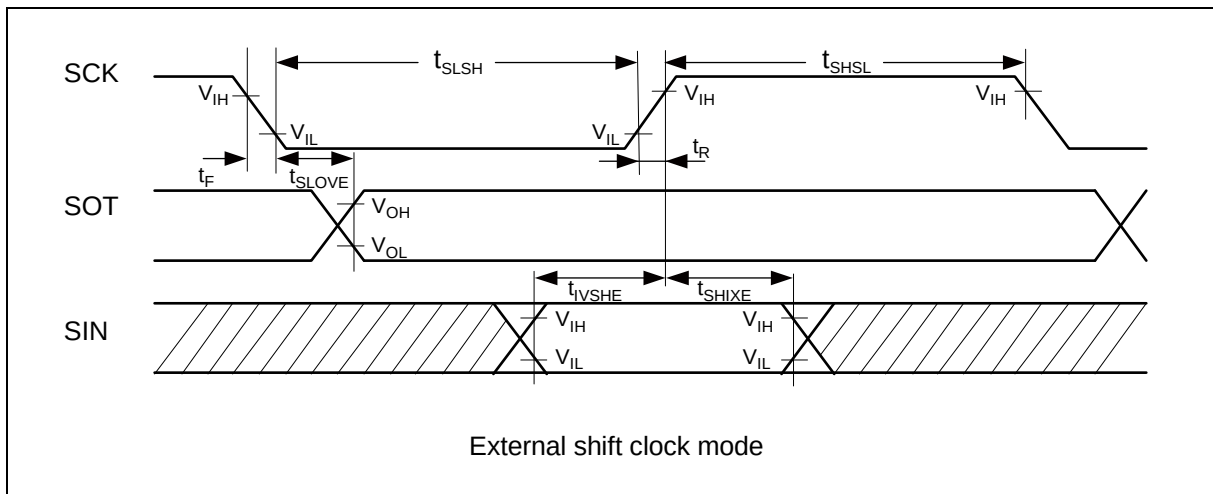
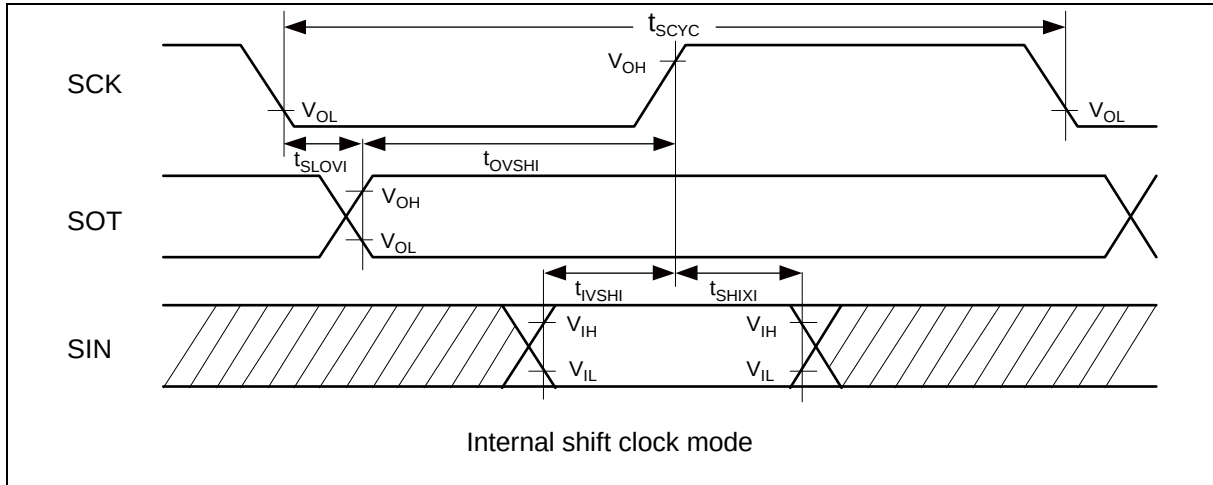


14.4.6 Reset Input

($V_{CC} = AV_{CC} = DV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = DV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Reset input time	t_{RSTL}	RSTX	10	-	μs
Rejection of reset input time			1	-	μs





14.4.10 I²C Timing

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Typical mode		High-speed mode ^{*4}		Unit
			Min	Max	Min	Max	
SCL clock frequency	f _{SCL}		0	100	0	400	kHz
(Repeated) START condition hold time SDA ↓ → SCL ↓	t _{HDSTA}	C _L = 50pF, R = (V _p /I _{OL}) ^{*1}	4.0	-	0.6	-	μs
SCL clock "L" width	t _{LOW}		4.7	-	1.3	-	μs
SCL clock "H" width	t _{HIGH}		4.0	-	0.6	-	μs
(Repeated) START condition setup time SCL ↑ → SDA ↓	t _{SUSTA}		4.7	-	0.6	-	μs
Data hold time SCL ↓ → SDA ↓ ↑	t _{HDDAT}		0	3.45 ^{*2}	0	0.9 ^{*3}	μs
Data setup time SDA ↓ ↑ → SCL ↑	t _{SUDAT}		250	-	100	-	ns
STOP condition setup time SCL ↑ → SDA ↑	t _{SUSTO}		4.0	-	0.6	-	μs
Bus free time between "STOP condition" and "START condition"	t _{BUS}		4.7	-	1.3	-	μs
Pulse width of spikes which will be suppressed by input noise filter	t _{SP}	-	0	(1-1.5) × t _{CLKP1} ^{*5}	0	(1-1.5) × t _{CLKP1} ^{*5}	ns

^{*1}: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively.

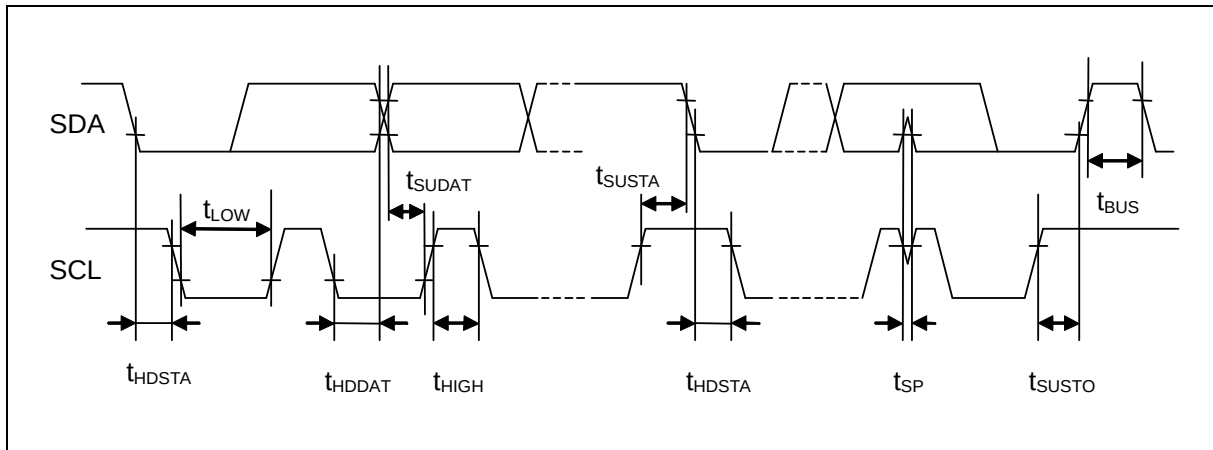
V_p indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

^{*2}: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

^{*3}: A high-speed mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250ns".

^{*4}: For use at over 100kHz, set the peripheral clock1 (CLKP1) to at least 6MHz.

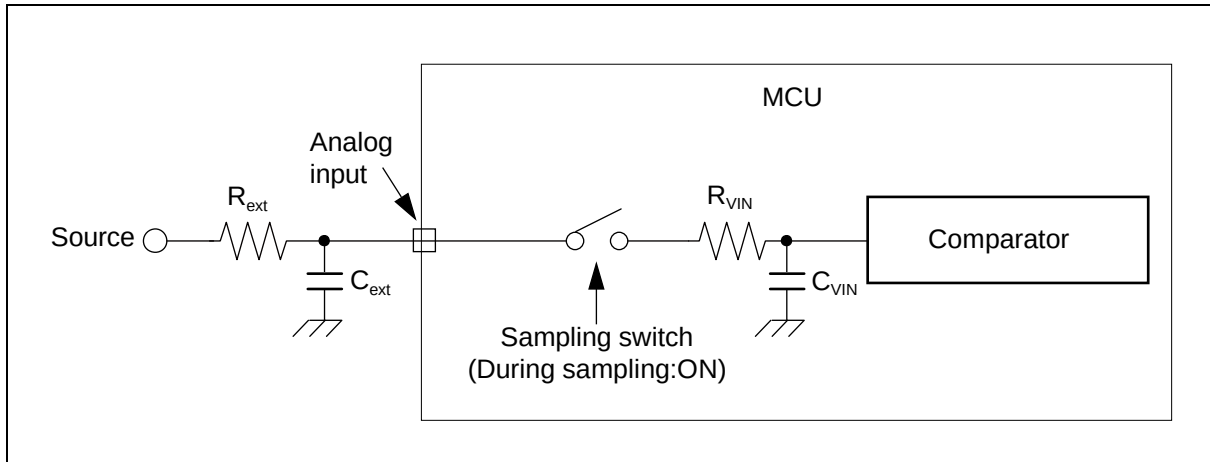
^{*5}: t_{CLKP1} indicates the peripheral clock1 (CLKP1) cycle time.



14.5.2 Accuracy and Setting of the A/D Converter Sampling Time

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.

To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time (T_{samp}) depends on the external driving impedance R_{ext} , the board capacitance of the A/D converter input pin C_{ext} and the AV_{CC} voltage level. The following replacement model can be used for the calculation:



R_{ext} : External driving impedance

C_{ext} : Capacitance of PCB at A/D converter input

C_{VIN} : Analog input capacity (I/O, analog switch and ADC are contained)

R_{VIN} : Analog input impedance (I/O, analog switch and ADC are contained)

The following approximation formula for the replacement model above can be used:

$$T_{\text{samp}} = 7.62 \times (R_{\text{ext}} \times C_{\text{ext}} + (R_{\text{ext}} + R_{\text{VIN}}) \times C_{\text{VIN}})$$

- Do not select a sampling time below the absolute minimum permitted value.
($0.5\mu\text{s}$ for $4.5\text{V} \leq AV_{\text{CC}} \leq 5.5\text{V}$, $1.2\mu\text{s}$ for $2.7\text{V} \leq AV_{\text{CC}} < 4.5\text{V}$)
- If the sampling time cannot be sufficient, connect a capacitor of about $0.1\mu\text{F}$ to the analog input pin.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current I_{IL} (static current before the sampling switch) or the analog input leakage current I_{AIN} (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current I_{IL} cannot be compensated by an external capacitor.
- The accuracy gets worse as $|AV_{\text{RH}} - AV_{\text{SS}}|$ becomes smaller.

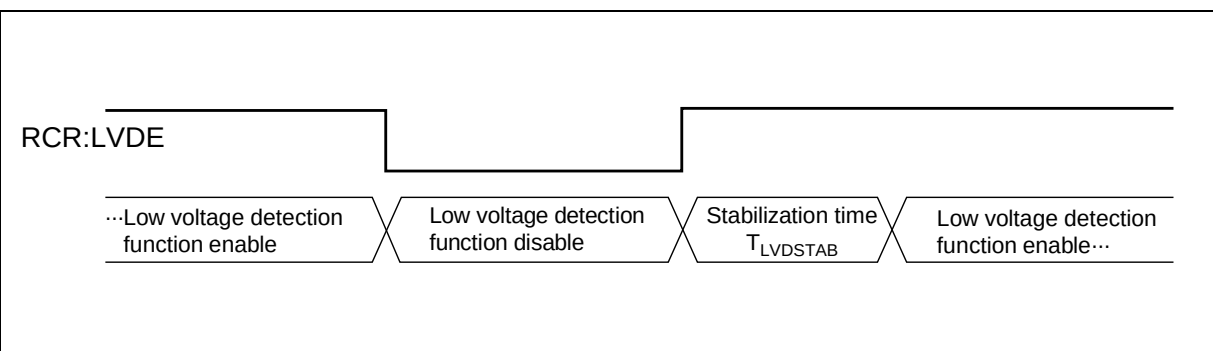
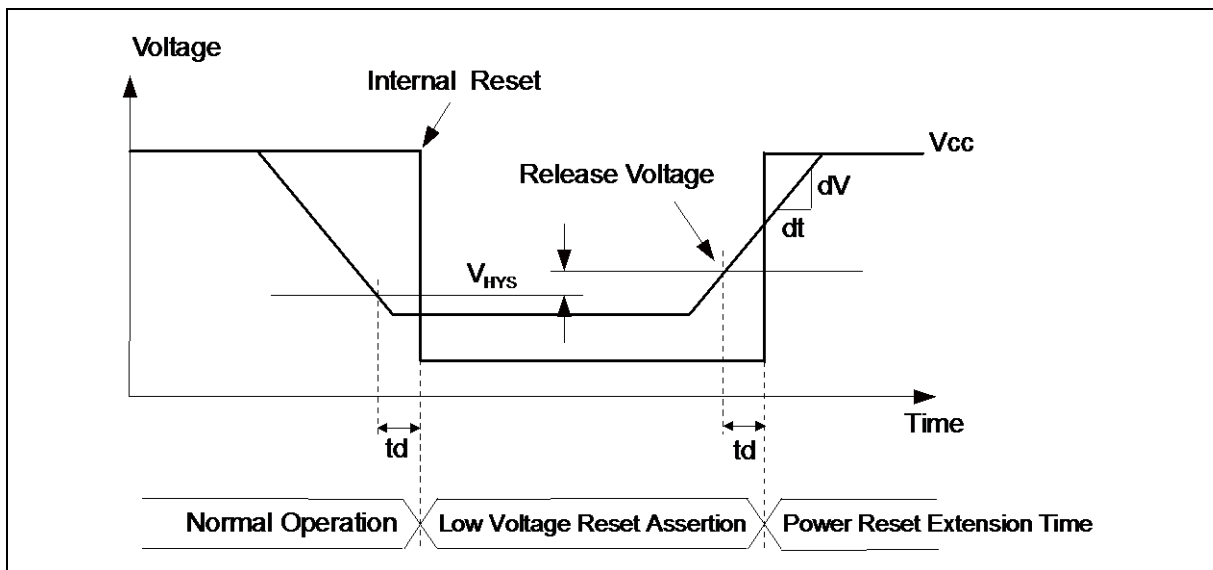
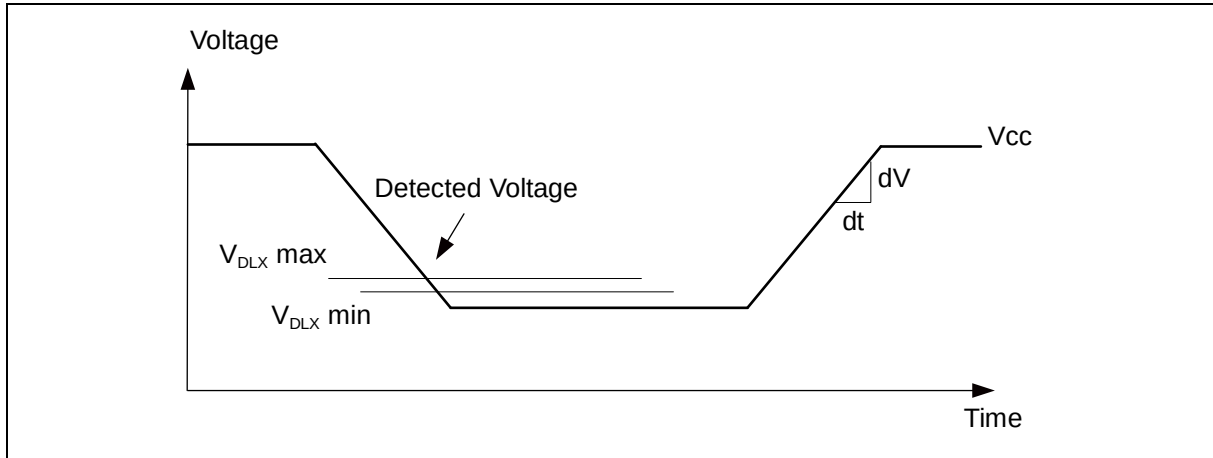
14.7 Low Voltage Detection Function Characteristics

($V_{CC} = AV_{CC} = DV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = DV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Detected voltage ^{*1}	V_{DL0}	CILCR:LVL = 0000 _B	2.70	2.90	3.10	V
	V_{DL1}	CILCR:LVL = 0001 _B	2.79	3.00	3.21	V
	V_{DL2}	CILCR:LVL = 0010 _B	2.98	3.20	3.42	V
	V_{DL3}	CILCR:LVL = 0011 _B	3.26	3.50	3.74	V
	V_{DL4}	CILCR:LVL = 0100 _B	3.45	3.70	3.95	V
	V_{DL5}	CILCR:LVL = 0111 _B	3.73	4.00	4.27	V
	V_{DL6}	CILCR:LVL = 1001 _B	3.91	4.20	4.49	V
Power supply voltage change rate ^{*2}	dV/dt	-	- 0.004	-	+ 0.004	V/ μ s
Hysteresis width	V_{HYS}	CILCR:LVHYS=0	-	-	50	mV
		CILCR:LVHYS=1	80	100	120	mV
Stabilization time	$T_{LVDSTAB}$	-	-	-	75	μ s
Detection delay time	t_d	-	-	-	30	μ s

^{*1}: If the power supply voltage fluctuates within the time less than the detection delay time (t_d), there is a possibility that the low voltage detection will occur or stop after the power supply voltage passes the detection range.

^{*2}: In order to perform the low voltage detection at the detection voltage (V_{DLX}), be sure to suppress fluctuation of the power supply voltage within the limits of the change ration of power supply voltage.



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