**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | F²MC-16FX |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CANbus, I²C, LINbus, SCI, UART/USART |
| Peripherals | DMA, LCD, LVD, POR, PWM, WDT |
| Number of I/O | 50 |
| Program Memory Size | 160KB (160K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 12x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb96f675rbpmc-gse2 |

- Built-in On Chip Debugger (OCD)
  - One-wire debug tool interface
  - Break function:
    - Hardware break: 6 points (shared with code event)
    - Software break: 4096 points
  - Event function
    - Code event: 6 points (shared with hardware break)
    - Data event: 6 points
    - Event sequencer: 2 levels + reset
  - Execution time measurement function
  - Trace function: 42 branches
  - Security function

- Flash Memory
  - Dual operation flash allowing reading of one Flash bank while programming or erasing the other bank
  - Command sequencer for automatic execution of programming algorithm and for supporting DMA for programming of the Flash Memory
  - Supports automatic programming, Embedded Algorithm
  - Write/Erase/Erase-Suspend/Resume commands
  - A flag indicating completion of the automatic algorithm
  - Erase can be performed on each sector individually
  - Sector protection
  - Flash Security feature to protect the content of the Flash
  - Low voltage detection during Flash erase or write

## Contents

## 1. Product Lineup

| Features | | | MB96670 | Remark |
|---|---|---|---|---|
| Product Type | | | Flash Memory Product | |
| Subclock | | | Subclock can be set by software | |
| Dual Operation Flash Memory | | RAM | - | |
| 64.5KB + 32KB | | 4KB | MB96F673R, MB96F673A | Product Options<br>R: MCU with CAN<br>A: MCU without CAN |
| 128.5KB + 32KB | | 4KB | MB96F675R, MB96F675A | |
| Package | | | LQFP-64<br>FPT-64P-M23/M24 | |
| DMA | | | 2ch | |
| USART | | | 2ch | LIN-USART 0/1 |
| | with automatic LIN-Header transmission/reception | | Yes (only 1ch) | LIN-USART 0 |
| | with 16 byte RX- and TX-FIFO | | No | |
| $I^2C$ | | | 1ch | $I^2C$ 0 |
| 8/10-bit A/D Converter | | | 12ch | AN 8/9/12/13/16 to 23 |
| | with Data Buffer | | No | |
| | with Range Comparator | | Yes | |
| | with Scan Disable | | Yes | |
| | with ADC Pulse Detection | | Yes | |
| 16-bit Reload Timer (RLT) | | | 3ch | RLT 1/2/6 |
| 16-bit Free-Running Timer (FRT) | | | 2ch | FRT 0/1 |
| 16-bit Input Capture Unit (ICU) | | | 4ch<br>(2 channels for LIN-USART) | ICU 0/1/4/5<br>ICU 0/1 for LIN-USART |
| 8/16-bit Programmable Pulse Generator (PPG) | | | 4ch (16-bit) / 8ch (8-bit) | PPG 0 to 3 |
| | with Timing point capture | | Yes | |
| | with Start delay | | No | |
| | with Ramp | | No | |
| CAN Interface | | | 1ch | CAN 0<br>32 Message Buffers |
| Stepping Motor Controller (SMC) | | | 2ch | SMC 0/1 |
| External Interrupts (INT) | | | 7ch | INT 0 to 4/6/7 |
| Non-Maskable Interrupt (NMI) | | | 1ch | |
| Sound Generator (SG) | | | 1ch | SG 0 |
| LCD Controller | | | 4COM × 24SEG | COM 0 to 3<br>SEG 3 to 6/8 to 11/<br>19 to 21/23/30/36 to 39/42/45 to 47/54 to 56 |
| Real Time Clock (RTC) | | | 1ch | |
| I/O Ports | | | 48 (Dual clock mode)<br>50 (Single clock mode) | |
| Clock Calibration Unit (CAL) | | | 1ch | |
| Clock Output Function | | | 2ch | |
| Low Voltage Detection Function | | | Yes | Low voltage detection function can be<br>disabled by software |
| Hardware Watchdog Timer | | | Yes | |
| On-chip RC-oscillator | | | Yes | |
| On-chip Debugger | | | Yes | |

**Note:**

All signals of the peripheral function in each product cannot be allocated by limiting the pins of package.

It is necessary to use the port relocate function of the general I/O port according to your function use.

## 4. Pin Description

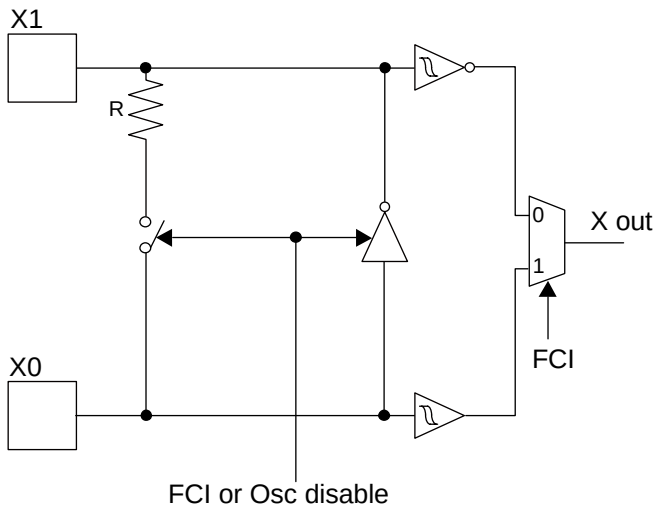
| Pin name | Feature | Description |
|---|---|---|
| ADTG | ADC | A/D converter trigger input pin |
| ANn | ADC | A/D converter channel n input pin |
| AVcc | Supply | Analog circuits power supply pin |
| AVRH | ADC | A/D converter high reference voltage input pin |
| AVss | Supply | Analog circuits power supply pin |
| C | Voltage regulator | Internally regulated power supply stabilization capacitor pin |
| CKOTn | Clock Output function | Clock Output function n output pin |
| CKOTn_R | Clock Output function | Relocated Clock Output function n output pin |
| CKOTXn | Clock Output function | Clock Output function n inverted output pin |
| COMn | LCD | LCD Common driver pin |
| DEBUG I/F | OCD | On Chip Debugger input/output pin |
| DVcc | Supply | SMC pins power supply |
| DVss | Supply | SMC pins power supply |
| INn | ICU | Input Capture Unit n input pin |
| INn_R | ICU | Relocated Input Capture Unit n input pin |
| INTn | External Interrupt | External Interrupt n input pin |
| INTn_R | External Interrupt | Relocated External Interrupt n input pin |
| MD | Core | Input pin for specifying the operating mode |
| NMI | External Interrupt | Non-Maskable Interrupt input pin |
| Pnn_m | GPIO | General purpose I/O pin |
| PPGn | PPG | Programmable Pulse Generator n output pin (16bit/8bit) |
| PPGn_R | PPG | Relocated Programmable Pulse Generator n output pin (16bit/8bit) |
| PPGn_B | PPG | Programmable Pulse Generator n output pin (16bit/8bit) |
| PWMn | SMC | SMC PWM high current output pin |
| RSTX | Core | Reset input pin |
| RXn | CAN | CAN interface n RX input pin |
| SCKn | USART | USART n serial clock input/output pin |
| SCLn | $I^2C$ | $I^2C$ interface n clock I/O input/output pin |
| SDAn | $I^2C$ | $I^2C$ interface n serial data I/O input/output pin |
| SEGn | LCD | LCD Segment driver pin |
| SGAn | Sound Generator | Sound Generator amplitude output pin |
| SGOn | Sound Generator | Sound Generator sound/tone output pin |
| SINn | USART | USART n serial data input pin |
| SOTn | USART | USART n serial data output pin |
| TINn | Reload Timer | Reload Timer n event input pin |
| TINn_R | Reload Timer | Relocated Reload Timer n event input pin |
| TOTn | Reload Timer | Reload Timer n output pin |
| TOTn_R | Reload Timer | Relocated Reload Timer n output pin |
| TTGn | PPG | Programmable Pulse Generator n trigger input pin |
| TXn | CAN | CAN interface n TX output pin |

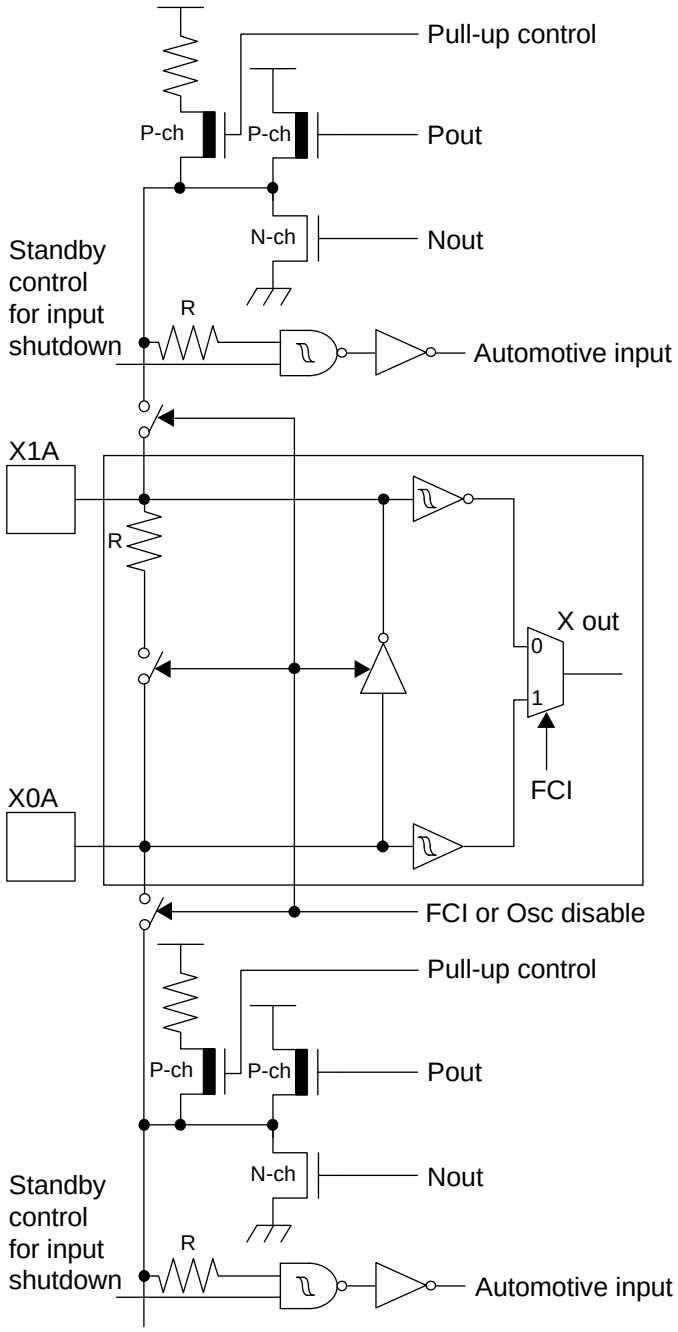
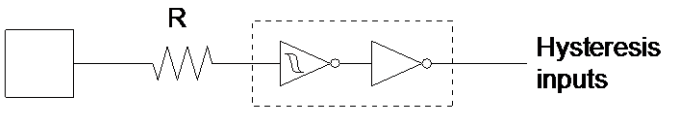
| Pin name | Feature | Description |
|---|---|---|
| Vn | LCD | LCD voltage reference pin |
| Vcc | Supply | Power supply pin |
| Vss | Supply | Power supply pin |
| WOT_R | RTC | Relocated Real Time clock output pin |
| X0 | Clock | Oscillator input pin |
| X0A | Clock | Subclock Oscillator input pin |
| X1 | Clock | Oscillator output pin |
| X1A | Clock | Subclock Oscillator output pin |

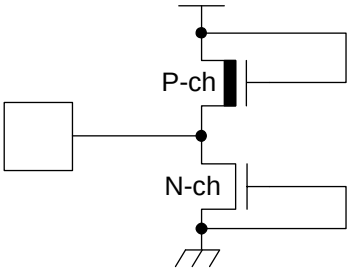
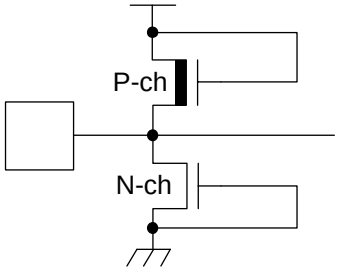
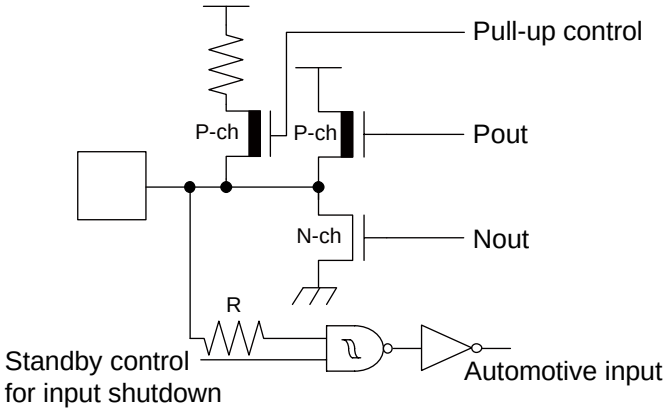
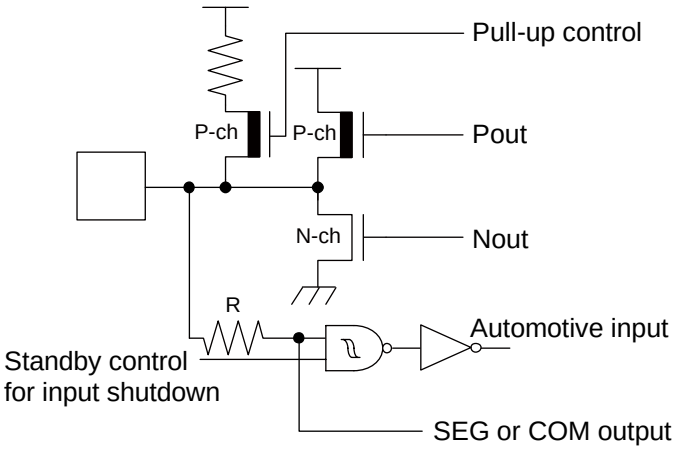
## 5. Pin Circuit Type

| Pin no. | I/O circuit type* | Pin name |
|---|---|---|
| 1 | Supply | Vss |
| 2 | F | C |
| 3 | M | P03_7 / INT1 / SIN1 |
| 4 | H | P13_0 / INT2 / SOT1 |
| 5 | P | P13_1 / INT3 / SCK1 / SEG42 |
| 6 | J | P00_7 / SEG19 / SGO0 |
| 7 | J | P01_0 / SEG20 / SGA0 |
| 8 | J | P02_2 / SEG30 / CKOT0_R |
| 9 | J | P06_5 / IN1 / SEG54 / TTG1 |
| 10 | J | P06_6 / TIN1 / SEG55 / IN4_R |
| 11 | J | P06_7 / TOT1 / SEG56 / IN5_R |
| 12 | K | P05_0 / AN8 |
| 13 | K | P05_1 / AN9 |
| 14 | Supply | AVcc |
| 15 | G | AVRH |
| 16 | Supply | AVss |
| 17 | K | P05_4 / AN12 / INT2_R / WOT_R |
| 18 | K | P05_5 / AN13 |
| 19 | R | P08_0 / PWM1P0 / AN16 |
| 20 | R | P08_1 / PWM1M0 / AN17 |
| 21 | R | P08_2 / PWM2P0 / AN18 |
| 22 | R | P08_3 / PWM2M0 / AN19 |
| 23 | Supply | DVcc |
| 24 | Supply | DVss |
| 25 | R | P08_4 / PWM1P1 / AN20 |
| 26 | R | P08_5 / PWM1M1 / AN21 |
| 27 | R | P08_6 / PWM2P1 / AN22 |
| 28 | R | P08_7 / PWM2M1 / AN23 |
| 29 | P | P13_4 / SIN0 / INT6 / SEG45 |
| 30 | J | P13_5 / SOT0 / ADTG / INT7 / SEG46 |
| 31 | P | P13_6 / SCK0 / CKOTX0 / SEG47 |
| 32 | N | P04_4 / PPG3 / SDA0 |

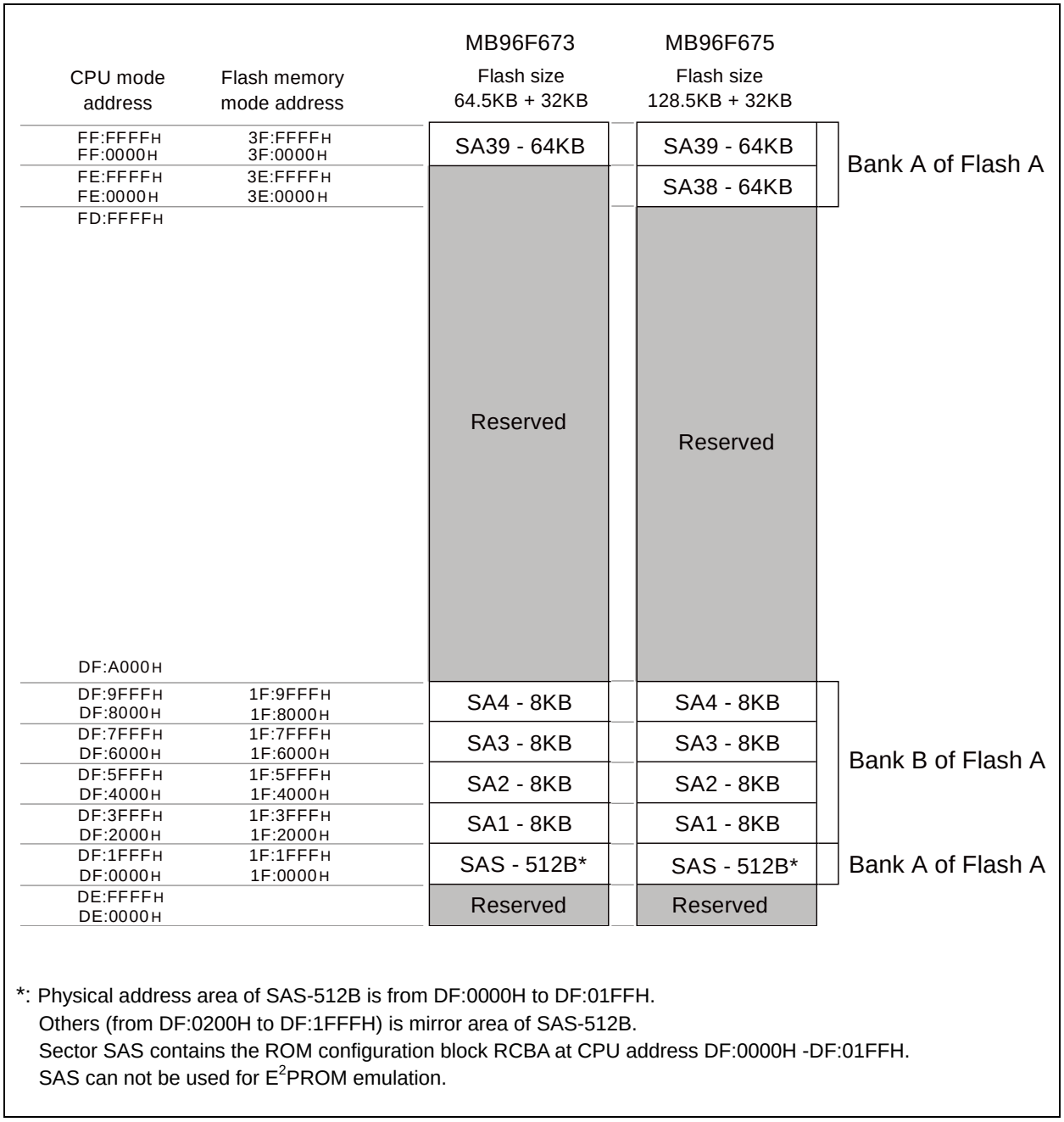
## 6. I/O Circuit Type

| Type | Circuit | Remarks |
|---|---|---|
| A |  | High-speed oscillation circuit:<br>• Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin)<br>• Feedback resistor = approx. 1.0MΩ<br>• The amplitude: 1.8V±0.15V to operate by the internal supply voltage |

| Type | Circuit | Remarks |
|---|---|---|
| B |  | Low-speed oscillation circuit shared with GPIO functionality:<br>• Feedback resistor = approx. 5.0MΩ<br>• GPIO functionality selectable (CMOS level output ($I_{OL}$ = 4mA, $I_{OH}$ = -4mA), Automotive input with input shutdown function and programmable pull-up resistor) |
| C |  | CMOS hysteresis input pin |

| Type | Circuit | Remarks |
|---|---|---|
| F |  | Power supply input protection circuit |
| G |  | • A/D converter ref+ (AVRH) power supply input pin with protection circuit<br>• Without protection circuit against $V_{CC}$ for pins AVRH |
| H |  | • CMOS level output ($I_{OL}$ = 4mA, $I_{OH}$ = -4mA)<br>• Automotive input with input shutdown function<br>• Programmable pull-up resistor |
| J |  | • CMOS level output ($I_{OL}$ = 4mA, $I_{OH}$ = -4mA)<br>• Automotive input with input shutdown function<br>• Programmable pull-up resistor<br>• SEG or COM output |

## 9. User ROM Memory Map For Flash Devices




*: Physical address area of SAS-512B is from DF:0000H to DF:01FFH.
Others (from DF:0200H to DF:1FFFH) is mirror area of SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address DF:0000H -DF:01FFH.
SAS can not be used for $E^2$PROM emulation.

| Vector number | Offset in vector table | Vector name | Cleared by DMA | Index in ICR to program | Description |
|---|---|---|---|---|---|
| 81 | $2B8_H$ | - | - | 81 | Reserved |
| 82 | $2B4_H$ | - | - | 82 | Reserved |
| 83 | $2B0_H$ | - | - | 83 | Reserved |
| 84 | $2AC_H$ | - | - | 84 | Reserved |
| 85 | $2A8_H$ | - | - | 85 | Reserved |
| 86 | $2A4_H$ | - | - | 86 | Reserved |
| 87 | $2A0_H$ | - | - | 87 | Reserved |
| 88 | $29C_H$ | - | - | 88 | Reserved |
| 89 | $298_H$ | FRT0 | Yes | 89 | Free-Running Timer 0 |
| 90 | $294_H$ | FRT1 | Yes | 90 | Free-Running Timer 1 |
| 91 | $290_H$ | - | - | 91 | Reserved |
| 92 | $28C_H$ | - | - | 92 | Reserved |
| 93 | $288_H$ | RTC0 | No | 93 | Real Time Clock |
| 94 | $284_H$ | CAL0 | No | 94 | Clock Calibration Unit |
| 95 | $280_H$ | SG0 | No | 95 | Sound Generator 0 |
| 96 | $27C_H$ | IIC0 | Yes | 96 | $I^2C$ interface 0 |
| 97 | $278_H$ | - | - | 97 | Reserved |
| 98 | $274_H$ | ADC0 | Yes | 98 | A/D Converter 0 |
| 99 | $270_H$ | - | - | 99 | Reserved |
| 100 | $26C_H$ | - | - | 100 | Reserved |
| 101 | $268_H$ | LINR0 | Yes | 101 | LIN USART 0 RX |
| 102 | $264_H$ | LINT0 | Yes | 102 | LIN USART 0 TX |
| 103 | $260_H$ | LINR1 | Yes | 103 | LIN USART 1 RX |
| 104 | $25C_H$ | LINT1 | Yes | 104 | LIN USART 1 TX |
| 105 | $258_H$ | - | - | 105 | Reserved |
| 106 | $254_H$ | - | - | 106 | Reserved |
| 107 | $250_H$ | - | - | 107 | Reserved |
| 108 | $24C_H$ | - | - | 108 | Reserved |
| 109 | $248_H$ | - | - | 109 | Reserved |
| 110 | $244_H$ | - | - | 110 | Reserved |
| 111 | $240_H$ | - | - | 111 | Reserved |
| 112 | $23C_H$ | - | - | 112 | Reserved |
| 113 | $238_H$ | - | - | 113 | Reserved |
| 114 | $234_H$ | - | - | 114 | Reserved |
| 115 | $230_H$ | - | - | 115 | Reserved |
| 116 | $22C_H$ | - | - | 116 | Reserved |
| 117 | $228_H$ | - | - | 117 | Reserved |
| 118 | $224_H$ | - | - | 118 | Reserved |
| 119 | $220_H$ | - | - | 119 | Reserved |
| 120 | $21C_H$ | - | - | 120 | Reserved |

# 13. Handling Devices

**Special care is required for the following when handling the device:**

- Latch-up prevention
- Unused pins handling
- External clock usage
- Notes on PLL clock mode operation
- Power supply pins (Vcc/Vss)
- Crystal oscillator and ceramic resonator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on Power-on
- Stabilization of power supply voltage
- SMC power supply pins
- Serial communication
- Mode Pin (MD)

## 13.1 Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than $V_{CC}$ or lower than $V_{SS}$ is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between Vcc pins and Vss pins.
- The $AV_{CC}$ power supply is applied before the $V_{CC}$ voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage ($AV_{CC}$, AVRH) exceed the digital power-supply voltage.

## 13.2 Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register

PIER = 0).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent

damage of the device. To prevent latch-up, they must therefore be pulled up or pulled down through resistors which should be more than 2kΩ.

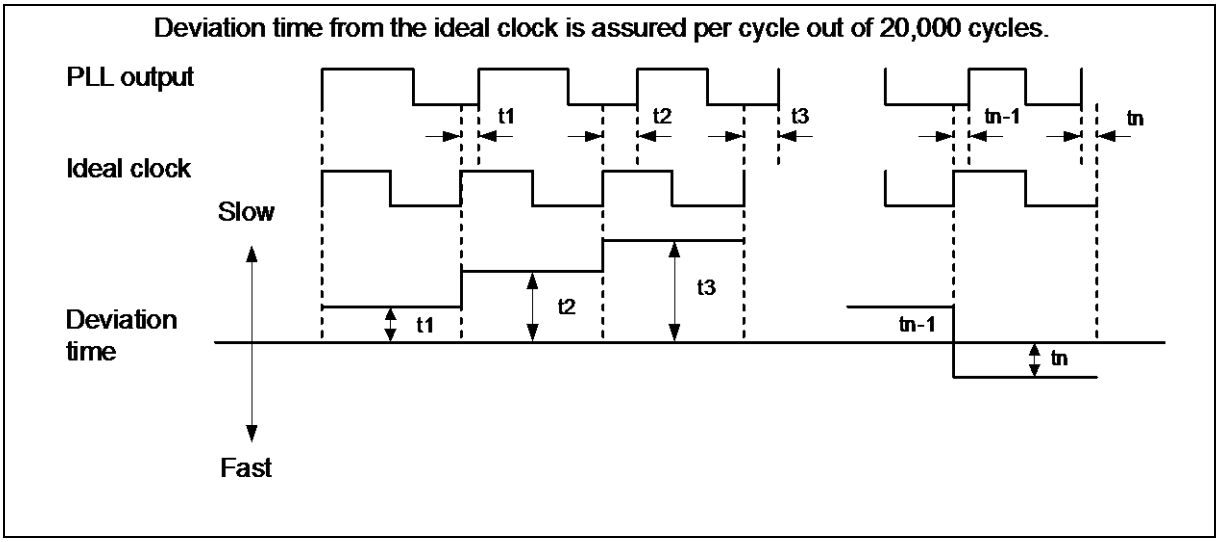
Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with

either input disabled or external pull-up/pull-down resistor as described above.

### 14.4.5 Operating Conditions of PLL

($V_{CC}$ = $AV_{CC}$ = $DV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V, $T_A$ = - 40°C to + 105°C)

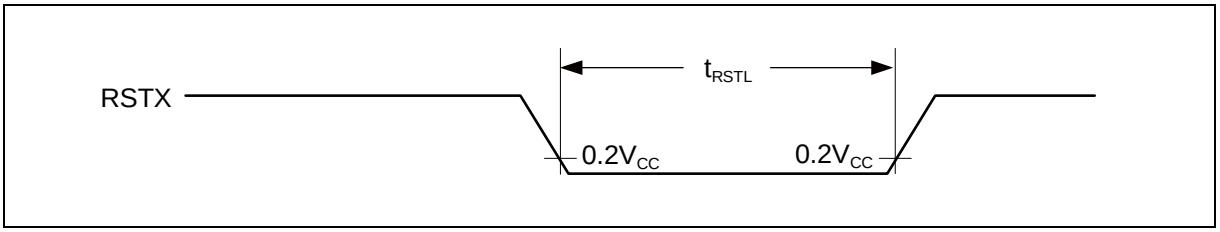
| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| PLL oscillation stabilization wait time | $t_{LOCK}$ | 1 | - | 4 | ms | For CLKMC = 4MHz |
| PLL input clock frequency | $f_{PLLI}$ | 4 | - | 8 | MHz | |
| PLL oscillation clock frequency | $f_{CLKVCO}$ | 56 | - | 108 | MHz | Permitted VCO output frequency of PLL (CLKVCO) |
| PLL phase jitter | $t_{PSKEW}$ | -5 | - | +5 | ns | For CLKMC (PLL input clock) ≥ 4MHz |




### 14.4.6 Reset Input

($V_{CC}$ = $AV_{CC}$ = $DV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V, $T_A$ = - 40°C to + 105°C)

| Parameter | Symbol | Pin name | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Reset input time | $t_{RSTL}$ | RSTX | 10 | - | µs |
| Rejection of reset input time | | | 1 | - | µs |

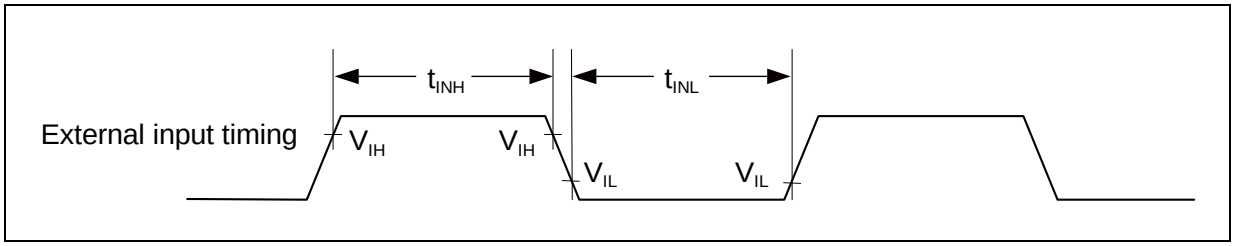


### 14.4.9 External Input Timing

($V_{CC}$ = $AV_{CC}$ = $DV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V, $T_A$ = - 40°C to + 105°C)

| Parameter | Symbol | Pin name | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Input pulse width | $t_{INH}$, $t_{INL}$ | Pnn_m | $2t_{CLKP1}$ +200 ($t_{CLKP1}$= $1/f_{CLKP1}$)* | - | ns | General Purpose I/O |
| | | ADTG | | | | A/D Converter trigger input |
| | | TINn, TINn_R | | | | Reload Timer |
| | | TTGn | | | | PPG trigger input |
| | | INn, INn_R | | | | Input Capture |
| | | INTn, INTn_R | 200 | - | ns | External Interrupt |
| | | NMI | | | | Non-Maskable Interrupt |

*: $t_{CLKP1}$ indicates the peripheral clock1 (CLKP1) cycle time except stop when in stop mode.



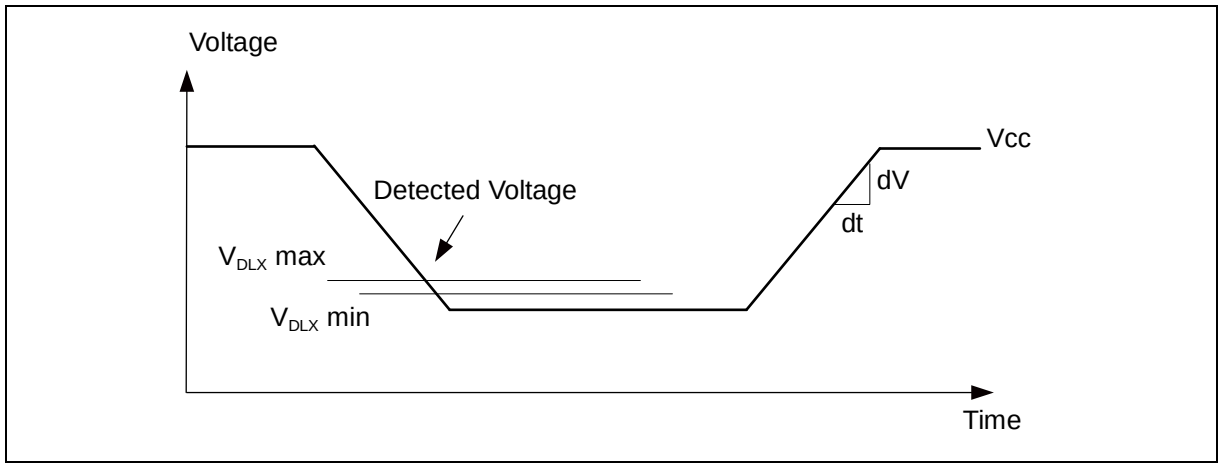
## 14.7 Low Voltage Detection Function Characteristics

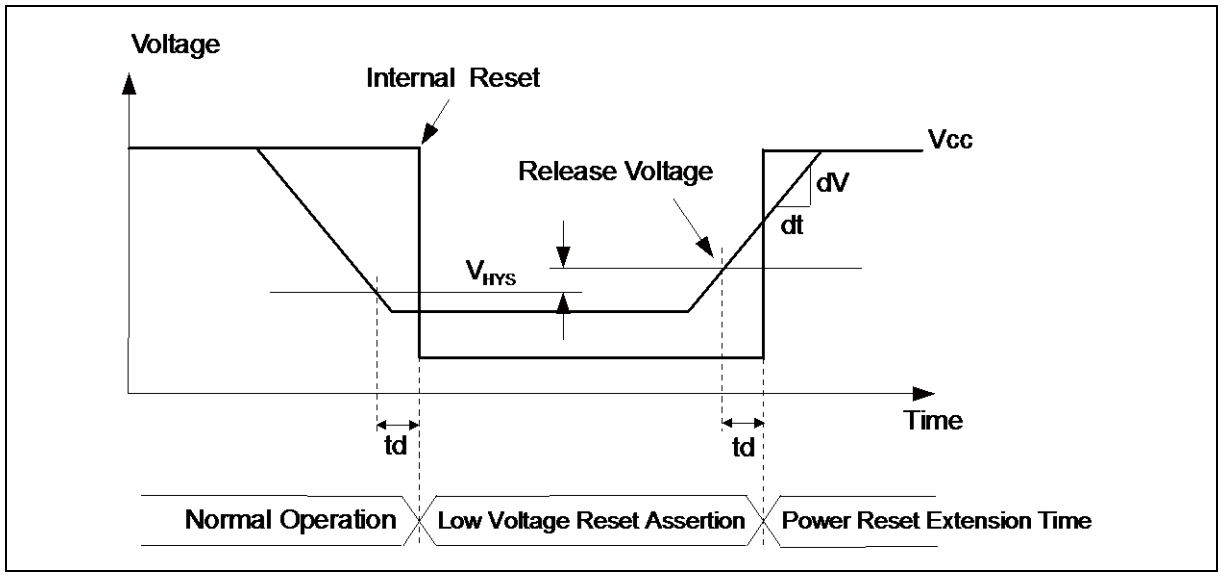
($V_{CC}$ = $AV_{CC}$ = $DV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V, $T_A$ = - 40°C to + 105°C)

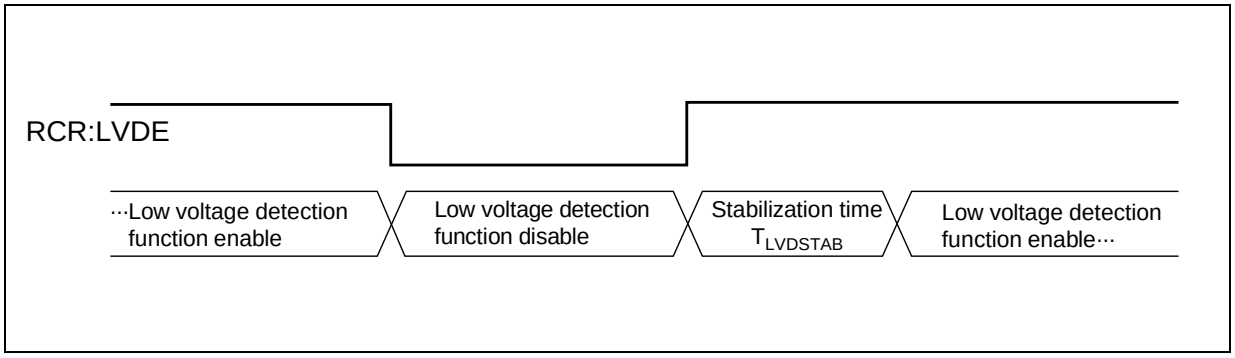
| Parameter | Symbol | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Detected voltage[*1] | $V_{DL0}$ | CILCR:LVL = $0000_B$ | 2.70 | 2.90 | 3.10 | V |
| | $V_{DL1}$ | CILCR:LVL = $0001_B$ | 2.79 | 3.00 | 3.21 | V |
| | $V_{DL2}$ | CILCR:LVL = $0010_B$ | 2.98 | 3.20 | 3.42 | V |
| | $V_{DL3}$ | CILCR:LVL = $0011_B$ | 3.26 | 3.50 | 3.74 | V |
| | $V_{DL4}$ | CILCR:LVL = $0100_B$ | 3.45 | 3.70 | 3.95 | V |
| | $V_{DL5}$ | CILCR:LVL = $0111_B$ | 3.73 | 4.00 | 4.27 | V |
| | $V_{DL6}$ | CILCR:LVL = $1001_B$ | 3.91 | 4.20 | 4.49 | V |
| Power supply voltage change rate[*2] | dV/dt | - | - 0.004 | - | + 0.004 | V/µs |
| Hysteresis width | $V_{HYS}$ | CILCR:LVHYS=0 | - | - | 50 | mV |
| | | CILCR:LVHYS=1 | 80 | 100 | 120 | mV |
| Stabilization time | $T_{LVDSTAB}$ | - | - | - | 75 | µs |
| Detection delay time | $t_d$ | - | - | - | 30 | µs |

[*1]: If the power supply voltage fluctuates within the time less than the detection delay time ($t_d$), there is a possibility that the low voltage detection will occur or stop after the power supply voltage passes the detection range.

[*2]: In order to perform the low voltage detection at the detection voltage ($V_{DLX}$), be sure to suppress fluctuation of the power supply voltage within the limits of the change ration of power supply voltage.


Voltage
Vcc
Detected Voltage
dV
dt
$V_{DLX}$ max
$V_{DLX}$ min
Time


Voltage
Internal Reset
Vcc
Release Voltage
dV
dt
$V_{HYS}$
Time
td
td
Normal Operation
Low Voltage Reset Assertion
Power Reset Extension Time


RCR:LVDE
···Low voltage detection function enable
Low voltage detection function disable
Stabilization time $T_{LVDSTAB}$
Low voltage detection function enable···

## 14.8 Flash Memory Write/Erase Characteristics

($V_{CC}$ = $AV_{CC}$ = $DV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V, $T_A$ = - 40°C to + 105°C)

| Parameter | | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Sector erase time | Large Sector | - | - | 1.6 | 7.5 | s | Includes write time prior to internal erase. |
| | Small Sector | - | - | 0.4 | 2.1 | s | |
| | Security Sector | - | - | 0.31 | 1.65 | s | |
| Word (16-bit) write time | | - | - | 25 | 400 | µs | Not including system-level overhead time. |
| Chip erase time | | - | - | 5.11 | 25.05 | s | Includes write time prior to internal erase. |

**Note:**

While the Flash memory is written or erased, shutdown of the external power ($V_{CC}$) is prohibited. In the application system where the external power ($V_{CC}$) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.

To put it concrete, change the external power in the range of change ration of power supply voltage (-0.004V/µs to +0.004V/µs) after the external power falls below the detection voltage ($V_{DLX}$)[*1].

Write/Erase cycles and data hold time

| Write/Erase cycles (cycle) | Data hold time (year) |
|---|---|
| 1,000 | 20 [*2] |
| 10,000 | 10 [*2] |
| 100,000 | 5 [*2] |

[*1]: See "Low Voltage Detection Function Characteristics".

[*2]: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

| Page | Section | Change Results |
|---|---|---|
| 40 | ELECTRICAL CHARACTERISTICS<br>3. DC Characteristics<br>(1) Current Rating | Changed the annotation *2<br>Power supply for "On Chip Debugger" part is not included.<br>Power supply current in Run mode does not include Flash Write / Erase current.<br>→<br>The current for "On Chip Debugger" part is not included. |
| | | Added the description to annotation *2, *3<br>When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current. |
| 52 | 4. AC Characteristics<br>(10) $I^2C$ timing | Added parameter, “Noise filter” and an annotation *5 for it |
| | | Added $t_{SP}$ to the figure |
| 54 | 5. A/D Converter<br>(2) Accuracy and Setting of the A/D Converter Sampling Time | Deleted the unit “[Min]” from approximation formula of Sampling time |
| 57 | 6. High Current Output Slew Rate | Changed the condition<br>($V_{CC}$ = $AV_{CC}$ = $DV_{CC}$ = 2.7V to 5.5V, VD=1.8V±0.15V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V, $T_A$ = - 40°C to + 105°C)<br>→<br>($V_{CC}$ = $AV_{CC}$ = $DV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V, $T_A$ = - 40°C to + 105°C) |
| 60 | 8. Flash Memory Write/Erase Characteristics | Changed the condition<br>($V_{CC}$ = $AV_{CC}$ = $DV_{CC}$ = 2.7V to 5.5V, VD=1.8V±0.15V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V, $T_A$ = - 40°C to + 105°C)<br>→<br>($V_{CC}$ = $AV_{CC}$ = $DV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = $DV_{SS}$ = 0V, $T_A$ = - 40°C to + 105°C) |
| | | Changed the Note<br>While the Flash memory is written, shutdown of the external power ($V_{CC}$) is prohibited. In the application system where the external power ($V_{CC}$) might be shut down while writing, be sure to turn the power off by using an external voltage detector.<br>→<br>While the Flash memory is written or erased, shutdown of the external power ($V_{CC}$) is prohibited. In the application system where the external power ($V_{CC}$) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function. |
| Revision 2.1 | | |
| - | - | Company name and layout design change |

**NOTE: Please see “Document History” about later revised information.**

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