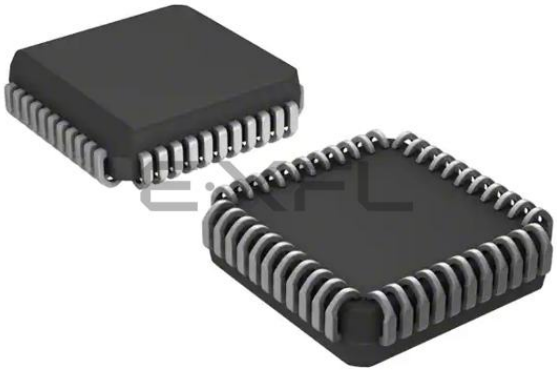

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Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc952fa-512

6. Pinning information

6.1 Pinning

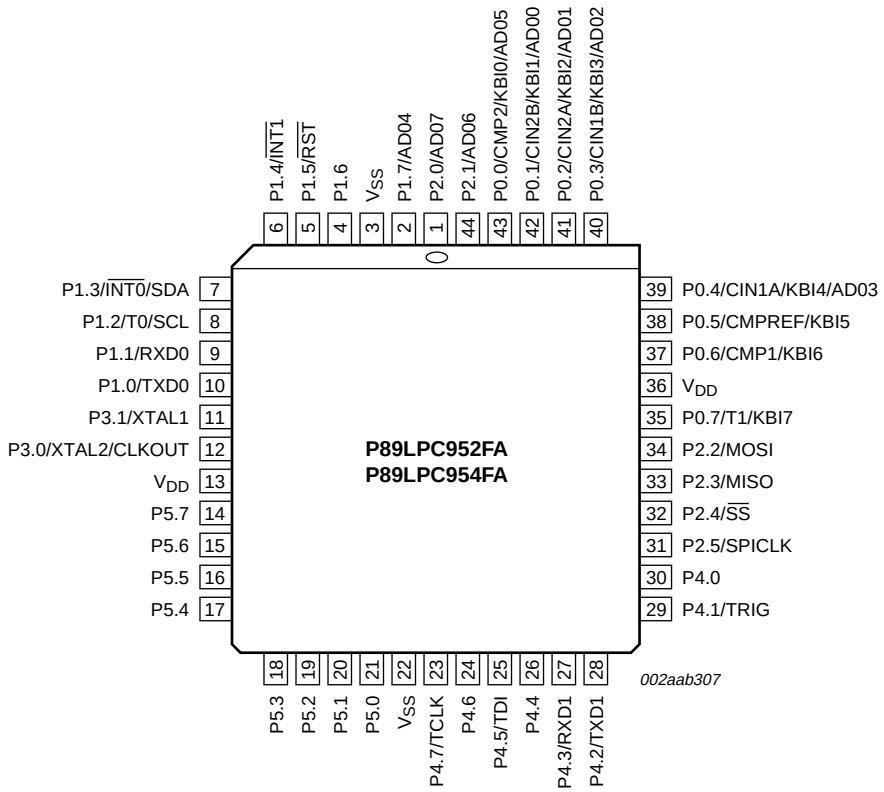


Fig 3. PLCC44 pin configuration

Table 3. Pin description *...continued*

Symbol	Pin			Type	Description
	LQFP48	PLCC44	LQFP44		
P1.5/$\overline{\text{RST}}$	47	5	43	I	**P1.5 —** Port 1 bit 5 (input only).
				I	**$\overline{\text{RST}}$ —** External Reset input during power-on or maybe a reset input/output if selected via UCFG1 and UCFG2. When functioning as a reset input or input/output, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. When functioning as a reset output or input/output an internal reset source will drive this pin LOW. Also used during a power-on sequence to force ISP mode. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**
P1.6	46	4	42	I/O	**P1.6 —** Port 1 bit 6.
P1.7/AD04	43	2	40	I/O	**P1.7 —** Port 1 bit 7.
				I	**AD04 —** ADC0 channel 4 analog input.
P2.0 to P2.5				I/O	**Port 2:** Port 2 is an 8-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 “Port configurations” and Table 11 “Static characteristics” for details. All pins have Schmitt triggered inputs. Port 2 also provides various special functions as described below:
P2.0/AD07	42	1	39	I/O	**P2.0 —** Port 2 bit 0.
				I	**AD07 —** ADC0 channel 7 analog input.
P2.1/AD06	41	44	38	I/O	**P2.1 —** Port 2 bit 1.
				I	**AD06 —** ADC0 channel 6 analog input.
P2.2/MOSI	30	34	28	I/O	**P2.2 —** Port 2 bit 2.
				I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.3/MISO	29	33	27	I/O	**P2.3 —** Port 2 bit 3.
				I/O	**MISO —** When configured as master, this pin is input, when configured as slave, this pin is output.
P2.4/$\overline{\text{SS}}$	28	32	26	I/O	**P2.4 —** Port 2 bit 4.
				I/O	**$\overline{\text{SS}}$ —** SPI Slave select.

Table 4. Special function registers *…continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**		
IEN0[1]	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	EX1	ET0	EX0	00	0000 0000
		Bit address	**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**	**E8**		
IEN1[1]	Interrupt enable 1	E8H	-	EST	-	-	ESPI	EC	EKBI	EI2C	00[2]	00x0 0000
IEN2	Interrupt enable 2	D5H	-	-	-	-	EST1	ES1/ESR1	EADC	-	00[2]	00x0 0000
		Bit address	**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**	**B8**		
IP0[1]	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	PX1	PT0	PX0	00[2]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/ PSRH	PT1H	PX1H	PT0H	PX0H	00[2]	x000 0000
		Bit address	**FF**	**FE**	**FD**	**FC**	**FB**	**FA**	**F9**	**F8**		
IP1[1]	Interrupt priority 1	F8H	-	PST	-	-	PSPI	PC	PKBI	PI2C	00[2]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	-	PSTH	-	-	PSPIH	PCH	PKBIH	PI2CH	00[2]	00x0 0000
IP2	Interrupt priority 2	D6H	-	-	-	-	PEST1	PES1/ PESR1	PADC	-	00[2]	00x0 0000
IP2H	Interrupt priority 2 high	D7H	-	-	-	-	PEST1H	PES1H/ PESR1H	PADCH	-	00[2]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN _SEL	KBIF	00[2]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H									00	0000 0000
KBPATN	Keypad pattern register	93H									FF	1111 1111
		Bit address	**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**		
P0[1]	Port 0	80H	T1/KB7	CMP1 /KB6	CMPREF /KB5	CIN1A /KB4	CIN1B /KB3	CIN2A /KB2	CIN2B /KB1	CMP2 /KB0	[2]	
		Bit address	**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P1[1]	Port 1	90H	-	-	$\overline{\text{RST}}$	$\overline{\text{INT1}}$	$\overline{\text{INT0}}$/SDA	T0/SCL	RXD0	TXD0	[2]	

Table 4. Special function registers *...continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	97	96	95	94	93	92	91	90		
P2[1]	Port 2	A0H	-	-	SPICLK	$\overline{SS}$	MISO	MOSI	-	-	[2]	
		Bit address	B7	B6	B5	B4	B3	B2	B1	B0		
P3[1]	Port 3	B0H	-	-	-	-	-	-	XTAL1	XTAL2	[2]	
P4	Port 4	B3H	-	TMS	-	-	RXD1	TXD1	TRIG	T3EX	[2]	
P5	Port 5	B4H	T3	-	-	-	-	-	-	-	[2]	
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF[2]	1111 1111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00[2]	0000 0000
P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3[2]	11x1 xx11
P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00[2]	00x0 xx00
P2M1	Port 2 output mode 1	A4H	(P2M1.7)	(P2M1.6)	(P2M1.5)	(P2M1.4)	(P2M1.3)	(P2M1.2)	(P2M1.1)	(P2M1.0)	FF[2]	1111 1111
P2M2	Port 2 output mode 2	A5H	(P2M2.7)	(P2M2.6)	(P2M2.5)	(P2M2.4)	(P2M2.3)	(P2M2.2)	(P2M2.1)	(P2M2.0)	00[2]	0000 0000
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03[2]	xxxx xx11
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00[2]	xxxx xx00
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD	-	VCPD	ADPD	I2PD	SPPD	SPD	-	00[2]	0000 0000
		Bit address	D7	D6	D5	D4	D3	D2	D1	D0		
PSW[1]	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00 000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX	[4]	

Table 4. Special function registers *...continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
RTCCON	RTC control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[2][7]	011x xx00
RTCH	RTC register high	D2H									00[7]	0000 0000
RTCL	RTC register low	D3H									00[7]	0000 0000
S0ADDR	Serial port address register	A9H									00	0000 0000
S0ADEN	Serial port address enable	B9H									00	0000 0000
S0BUF	Serial Port data buffer register	99H									xx	xxxx xxxx
	Bit address		**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**		
S0CON[1]	Serial port control	98H	SM0_0/FE_0	SM1_00	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	00	0000 0000
S0STAT	Serial port extended status register	BAH	DBMOD_0	INTLO_0	CIDIS_0	DBISEL_0	FE_0	BR_0	OE_0	STINT_0	00	0000 0000
SP	Stack pointer	81H									07	0000 0111
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04	0000 0100
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-	-	00	00xx xxxx
SPDAT	SPI data register	E3H									00	0000 0000
S1CON	Serial port 1 control	B6H	SM0_1/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	00	0000 0000
S1STAT	Serial port 1 extended status register	D4H	DBMOD_1	INTLO_1	CIDIS_1	DBISEL_1	FE_1	BR_1	OE_1	STINT_1	00	0000 0000
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0 xxx0

Table 5. Extended special function registers

Name	Description	SFR addr.	Bit functions and addresses		Reset value	
			MSB	LSB	Hex	Binary
ADC0HBND	ADC0 high_boundary register, left (MSB)	FFEFH			FF	1111 1111
ADC0LBND	ADC0 low_boundary register (MSB)	FFEEH			00	0000 0000
AD0DAT0R	ADC0 data register 0, right (LSB)	FFFEH	AD0DAT0[7:0]		00	0000 0000
AD0DAT0L	ADC0 data register 0, left (MSB)	FFFFH	AD0DAT0[9:2]		00	0000 0000
AD0DAT1R	ADC0 data register 1, right (LSB)	FFFCH	AD0DAT1[7:0]		00	0000 0000
AD0DAT1L	ADC0 data register 1, left (MSB)	FFFDH	AD0DAT1[9:2]		00	0000 0000
AD0DAT2R	ADC0 data register 2, right (LSB)	FFFAH	AD0DAT2[7:0]		00	0000 0000
AD0DAT2L	ADC0 data register 2, left (MSB)	FFFBH	AD0DAT2[9:2]		00	0000 0000
AD0DAT3R	ADC0 data register 3, right (LSB)	FFF8H	AD0DAT3[7:0]		00	0000 0000
AD0DAT3L	ADC0 data register 3, left (MSB)	FFF9H	AD0DAT3[9:2]		00	0000 0000
AD0DAT4R	ADC0 data register 4, right (LSB)	FFF6H	AD0DAT4[7:0]		00	0000 0000
AD0DAT4L	ADC0 data register 4, left (MSB)	FFF7H	AD0DAT4[9:2]		00	0000 0000
AD0DAT5R	ADC0 data register 5, right (LSB)	FFF4H	AD0DAT5[7:0]		00	0000 0000
AD0DAT5L	ADC0 data register 5, left (MSB)	FFF5H	AD0DAT5[9:2]		00	0000 0000
AD0DAT6R	ADC0 data register 6, right (LSB)	FFF2H	AD0DAT6[7:0]		00	0000 0000
AD0DAT6L	ADC0 data register 6, left (MSB)	FFF3H	AD0DAT6[9:2]		00	0000 0000
AD0DAT7R	ADC0 data register 7, right (LSB)	FFF0H	AD0DAT7[7:0]			

in reset when V_{DD} falls below the minimum specified operating voltage. These requirements for clock frequencies above 12 MHz do not apply when using the internal RC oscillator in clock doubler mode.

7.3.6 Clock output

The P89LPC952/954 supports a user-selectable clock output function on the XTAL2/CLKOUT pin when crystal oscillator is not being used. This condition occurs if another clock source has been selected (on-chip RC oscillator, watchdog oscillator, external clock input on XTAL1) and if the RTC is not using the crystal oscillator as its clock source. This allows external devices to synchronize to the P89LPC952/954. This output is enabled by the ENCLK bit in the TRIM register.

The frequency of this clock output is $\frac{1}{2}$ that of the CCLK. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power.

7.4 On-chip RC oscillator option

The P89LPC952/954 has a 6-bit TRIM register that can be used to tune the frequency of the RC oscillator. During reset, the TRIM value is initialized to a factory pre-programmed value to adjust the oscillator frequency to 7.373 MHz ± 1 % at room temperature. End-user applications can write to the TRIM register to adjust the on-chip RC oscillator to other frequencies. When the clock doubler option is enabled (UCFG1.3 = 1), the output frequency is 14.746 MHz. If CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to reduce power consumption. On reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

The requirements in Section 7.3.5 “High speed oscillator option” for configuring P1.5 as an external reset input and using an external reset circuit when the clock frequency is greater than 12 MHz do **not** apply when using the internal RC oscillator’s clock doubler option.

7.5 Watchdog oscillator option

The watchdog has a separate oscillator which has a frequency of 400 kHz. This oscillator can be used to save power when a high clock frequency is not needed.

7.6 External clock input option

In this configuration, the processor clock is derived from an external source driving the P3.1/XTAL1 pin. The rate may be from 0 Hz up to 18 MHz. The P3.0/XTAL2 pin may be used as a standard port pin or a clock output.

When using an external clock input frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an external clock input frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage. These requirements for clock frequencies above 12 MHz do not apply when using the internal RC oscillator in clock doubler mode.

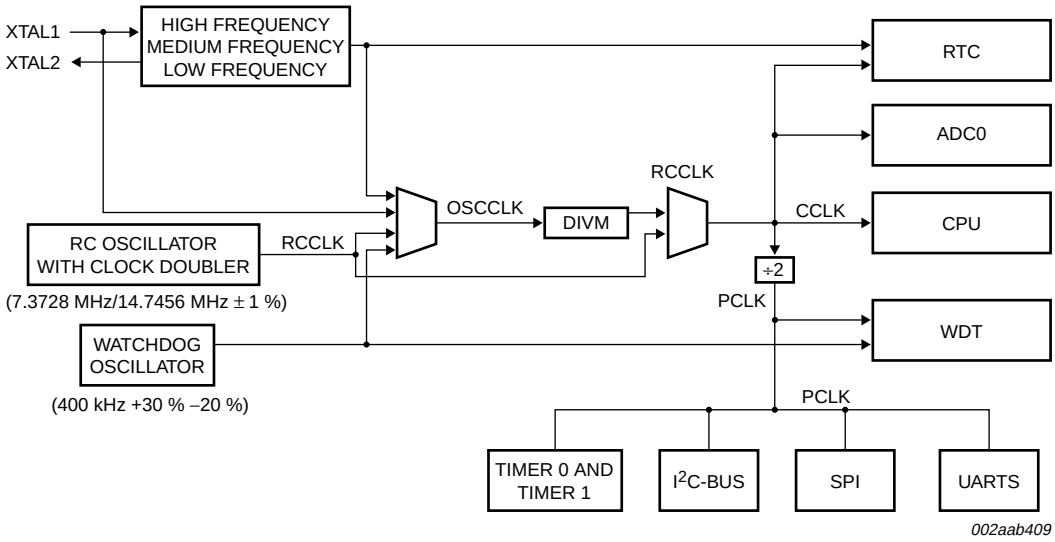


Fig 6. Block diagram of oscillator control

7.7 CCLK wake-up delay

The P89LPC952/954 has an internal wake-up timer that delays the clock until it stabilizes depending on the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 992 OSCCLK cycles plus 60 μs to 100 μs. If the clock source is either the internal RC oscillator, watchdog oscillator, or external clock, the delay is 224 OSCCLK cycles plus 60 μs to 100 μs.

7.8 CCLK modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

7.9 Low power select

The P89LPC952/954 is designed to run at 18 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to ‘1’ to lower the power consumption further. On any reset, CLKLP is ‘0’ allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

7.10 Memory organization

The various P89LPC952/954 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.

- IDATA

  Indirect Data. 256 bytes of internal data memory space (00H:FFH) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- XDATA

  'External' Data or Auxiliary RAM. Duplicates the classic 80C51 64 kB memory space addressed via the MOVX instruction using the SPTR, R0, or R1. All or part of this space could be implemented on-chip. The P89LPC952/954 has 256 bytes of on-chip XDATA memory, plus extended SFRs located in XDATA.

- CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC952/954 has 8 kB/16 kB of on-chip Code memory.

7.11 Data RAM arrangement

The 768 bytes of on-chip RAM are organized as shown in Table 6.

Table 6. On-chip data memory usages

Type	Data RAM	Size (bytes)
DATA	Memory that can be addressed directly and indirectly	128
IDATA	Memory that can be addressed indirectly	256
XDATA	Auxiliary ('External Data') on-chip memory that is accessed using the MOVX instructions	256

7.12 Interrupts

The P89LPC952/954 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources. The P89LPC952/954 supports 17 interrupt sources: external interrupts 0 and 1, timers 0 and 1, serial port 0 TX, serial port 0 RX, combined serial port 0 RX/TX, serial port 1 TX, serial port 1 RX, combined serial port 1 RX/TX, brownout detect, watchdog/RTC, I^2C-bus, keyboard, comparators 1 and 2, SPI, and ADC completion.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0, IEN1 or IEN2. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

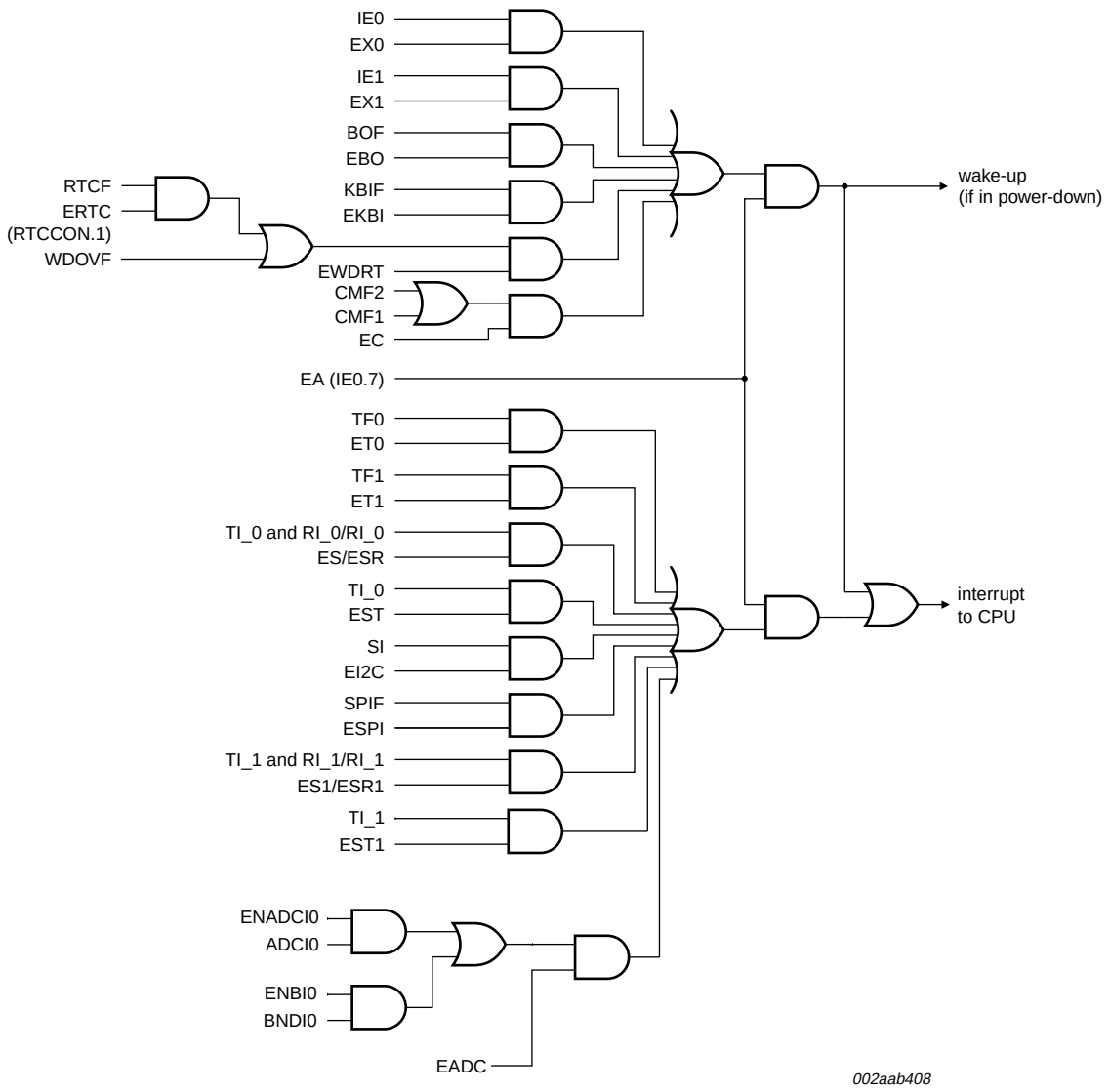


Fig 7. Interrupt sources, interrupt enables, and power-down wake-up sources

7.13 I/O ports

The P89LPC952/954 has six I/O ports: Port 0, Port 1, Port 2, Port 3, Port 4, and Port 5. Ports 0, 1, 2, 4, and 5 are 8-bit ports, and Port 3 is a 2-bit port. The exact number of I/O pins available depends upon the clock and reset options and package chosen, as shown in Table 7.

Table 7. Number of I/O pins available

Clock source	Reset option	Number of I/O pins (48-pin package)	Number of I/O pins (44-pin package)
On-chip oscillator or watchdog oscillator	No external reset (except during power-up)	42	40
	External $\overline{RST}$ pin supported	41	39
External clock input	No external reset (except during power-up)	41	39
	External $\overline{RST}$ pin supported[1]	40	38
Low/medium/high speed oscillator (external crystal or resonator)	No external reset (except during power-up)	40	38
	External $\overline{RST}$ pin supported[1]	39	37

[1] Required for operation above 12 MHz.

7.13.1 Port configurations

All but three I/O port pins on the P89LPC952/954 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

1. P1.5/$\overline{RST}$ can only be an input and cannot be configured.
2. P1.2/T0/SCL and P1.3/$\overline{INT0}$/SDA may only be configured to be either input-only or open-drain.

7.13.1.1 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC952/954 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt triggered input that also has a glitch suppression circuit.

7.13.1.2 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

Brownout detection may be enabled or disabled in software.

If brownout detection is enabled the brownout condition occurs when V_{DD} falls below the brownout trip voltage, V_{bo} (see Table 11 “Static characteristics”), and is negated when V_{DD} rises above V_{bo}. If the P89LPC952/954 device is to operate with a power supply that can be below 2.7 V, BOE should be left in the unprogrammed state so that the device can operate at 2.4 V, otherwise continuous brownout reset may prevent the device from operating.

For correct activation of brownout detect, the V_{DD} rise and fall times must be observed. Please see Table 11 “Static characteristics” for specifications.

7.14.2 Power-on detection

The Power-on detect has a function similar to the brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where brownout detect can work. The POF flag in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

7.15 Power reduction modes

The P89LPC952/954 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and total Power-down mode.

7.15.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

7.15.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC952/954 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the data retention supply voltage V_{DDR}. This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{DDR}, therefore it is highly recommended to wake-up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during power-down. These include: Brownout detect, watchdog timer, comparators (note that comparators can be powered down separately), and RTC/system timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock and the RTC is enabled.

7.15.3 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled. If the internal RC oscillator is used to clock the RTC during power-down, there will be high power consumption. Please use an external low frequency clock to achieve low power with the RTC running during power-down.

7.17.6 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

7.18 RTC/system timer

The P89LPC952/954 has a simple RTC that allows a user to continue running an accurate timer while the rest of the device is powered down. The RTC can be a wake-up or an interrupt source. The RTC is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all ‘0’s, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator, provided that the XTAL oscillator is not being used as the CPU clock. If the XTAL oscillator is used as the CPU clock, then the RTC will use CCLK as its clock source. Only power-on reset will reset the RTC and its associated SFRs to the default state.

7.19 UARTs

The P89LPC952/954 has two enhanced UARTs that are compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC952/954 does include an independent Baud Rate Generator for each UART (BRG0 for UART 0 and BRG1 for UART 1). The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator associated with the specific UART. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UARTs can be operated in 4 modes: shift register, 8-bit UART, 9-bit UART, and CPU clock/32 or CPU clock/16.

7.19.1 Mode 0

Serial data enters and exits through RXDn. TXDn outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $^{1}/_{16}$ of the CPU clock frequency.

7.19.2 Mode 1

10 bits are transmitted (through TXDn) or received (through RXDn): a start bit (logic 0), 8 data bits (LSB first), and a stop bit (logic 1). When data is received, the stop bit is stored in RB8_n in Special Function Register SnCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in Section 7.19.5 “Baud rate generator and selection”).

7.19.3 Mode 2

11 bits are transmitted (through TXDn) or received (through RXDn): start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). When data is transmitted, the 9th data bit (TB8_n in SnCON) can be assigned the value of ‘0’ or ‘1’. Or, for example, the parity bit (P, in the PSW) could be moved into TB8_n. When data is received, the 9th data bit goes into RB8_n in Special Function Register SnCON, while the

9. Limiting values

Table 10. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature		–55	+125	°C
T_{stg}	storage temperature		–65	+150	°C
$I_{OH(I/O)}$	HIGH-level output current per input/output pin		-	20	mA
$I_{OL(I/O)}$	LOW-level output current per input/output pin		-	20	mA
$I_{I/Otot(max)}$	maximum total input/output current		-	100	mA
V_n	voltage on any other pin	except V_{SS}, with respect to V_{DD}	-	3.5	V
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	1.5	W

[1] The following applies to Table 10:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over ambient temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

Table 11. Static characteristics *…continued*

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
C_{iss}	input capacitance		[6]	-	-	15	pF
I_{IL}	LOW-level input current	V_I = 0.4 V	[7]	-	-	−80	µA
I_{LI}	input leakage current	$V_I = V_{IL}$, V_{IH}, or $V_{th(HL)}$	[8]	-	-	±1	µA
I_{THL}	HIGH-LOW transition current	all ports; V_I = 1.5 V at V_{DD} = 3.6 V	[9]	−30	-	−450	µA
$R_{RST\_N(int)}$	internal pull-up resistance on pin $\overline{RST}$	pin $\overline{RST}$		10	-	30	kΩ
V_{bo}	brownout trip voltage	BOE = 1		2.4	-	2.7	V
$V_{ref(bg)}$	band gap reference voltage			1.19	1.23	1.27	V
TC_{bg}	band gap temperature coefficient			-	10	20	ppm/°C

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] The $I_{DD(oper)}$, $I_{DD(idle)}$, and $I_{DD(pd)}$ specifications are measured using an external clock with the following functions disabled: comparators, real-time clock, and watchdog timer.

[3] The $I_{DD(tpd)}$ specification is measured using an external clock with the following functions disabled: comparators, real-time clock, brownout detect, and watchdog timer.

[4] See Section 9 “Limiting values” for steady state (non-transient) limits on I_{OL} or I_{OH}. If I_{OL}/I_{OH} exceeds the test condition, V_{OL}/V_{OH} may exceed the related specification.

[5] This specification can be applied to pins which have A/D input or analog comparator input functions when the pin is not being used for those analog functions. When the pin is being used as an analog input pin, the maximum voltage on the pin must be limited to 4.0 V with respect to V_{SS}.

[6] Pin capacitance is characterized but not tested.

[7] Measured with port in quasi-bidirectional mode.

[8] Measured with port in high-impedance mode.

[9] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

11. Dynamic characteristics

Table 12. Dynamic characteristics (12 MHz)

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	nominal f = 7.3728 MHz trimmed to ± 1 % at T_{amb} = 25 °C; clock doubler option = OFF (default)	7.189	7.557	7.189	7.557	MHz
		nominal f = 14.7456 MHz; clock doubler option = ON, V_{DD} = 2.7 V to 3.6 V	14.378	15.114	14.378	15.114	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency		320	520	320	520	kHz
f_{osc}	oscillator frequency		0	12	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 19	83	-	-	-	ns
f_{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection time	P1.5/$\overline{\text{RST}}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{\text{RST}}$	-	15	-	15	ns
t_{sa}	signal acceptance time	P1.5/$\overline{\text{RST}}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{\text{RST}}$	50	-	50	-	ns
External clock							
t_{CHCX}	clock HIGH time	see Figure 19	33	$T_{cy(clk)} - t_{CLCX}$	33	-	ns
t_{CLCX}	clock LOW time	see Figure 19	33	$T_{cy(clk)} - t_{CHCX}$	33	-	ns
t_{CLCH}	clock rise time	see Figure 19	-	8	-	8	ns
t_{CHCL}	clock fall time	see Figure 19	-	8	-	8	ns
Shift register (UART mode 0)							
T_{XLXL}	serial port clock cycle time	see Figure 18	$16T_{cy(clk)}$	-	1333	-	ns
t_{QVXH}	output data set-up to clock rising edge time	see Figure 18	$13T_{cy(clk)}$	-	1083	-	ns
t_{XHQX}	output data hold after clock rising edge time	see Figure 18	-	$T_{cy(clk)}$ + 20	-	103	ns
t_{XHDX}	input data hold after clock rising edge time	see Figure 18	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge time	see Figure 18	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	slave		0	CCLK/6	0	2.0	MHz
	master		-	CCLK/4	-	3.0	MHz

11.1 Waveforms

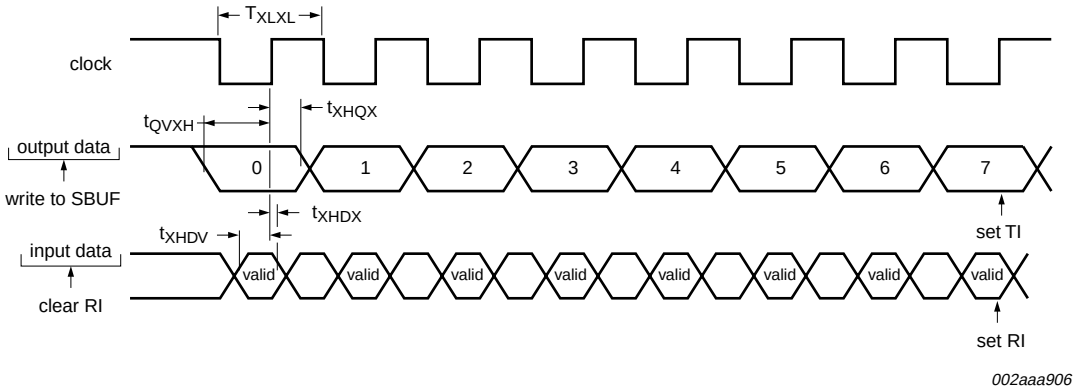


Fig 18. Shift register mode timing

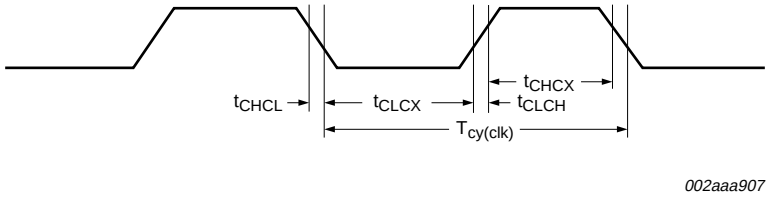


Fig 19. External clock timing

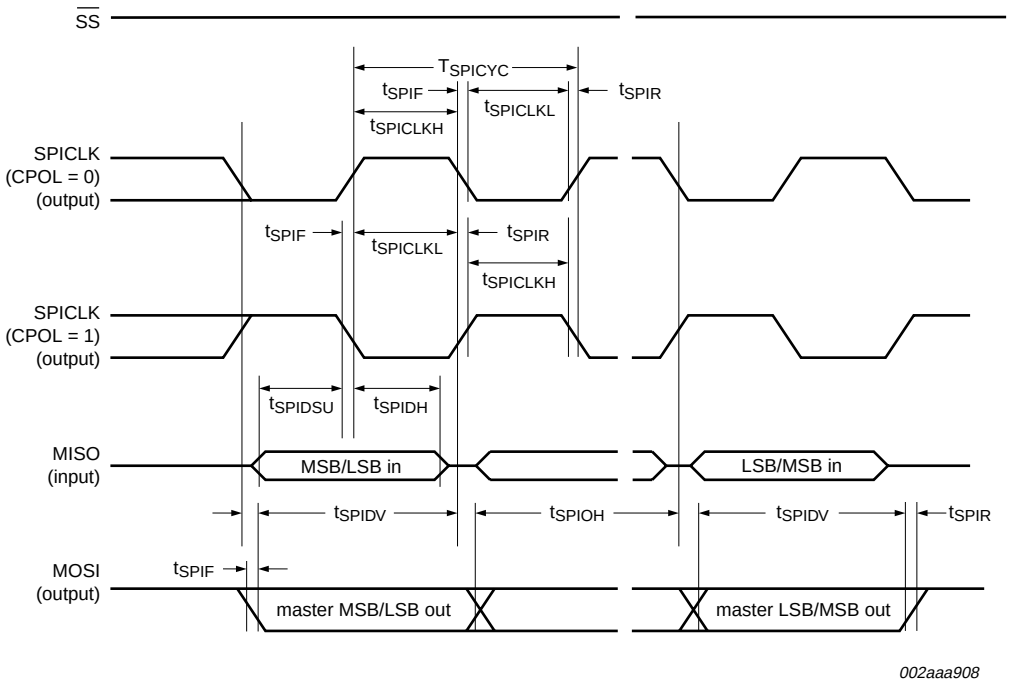
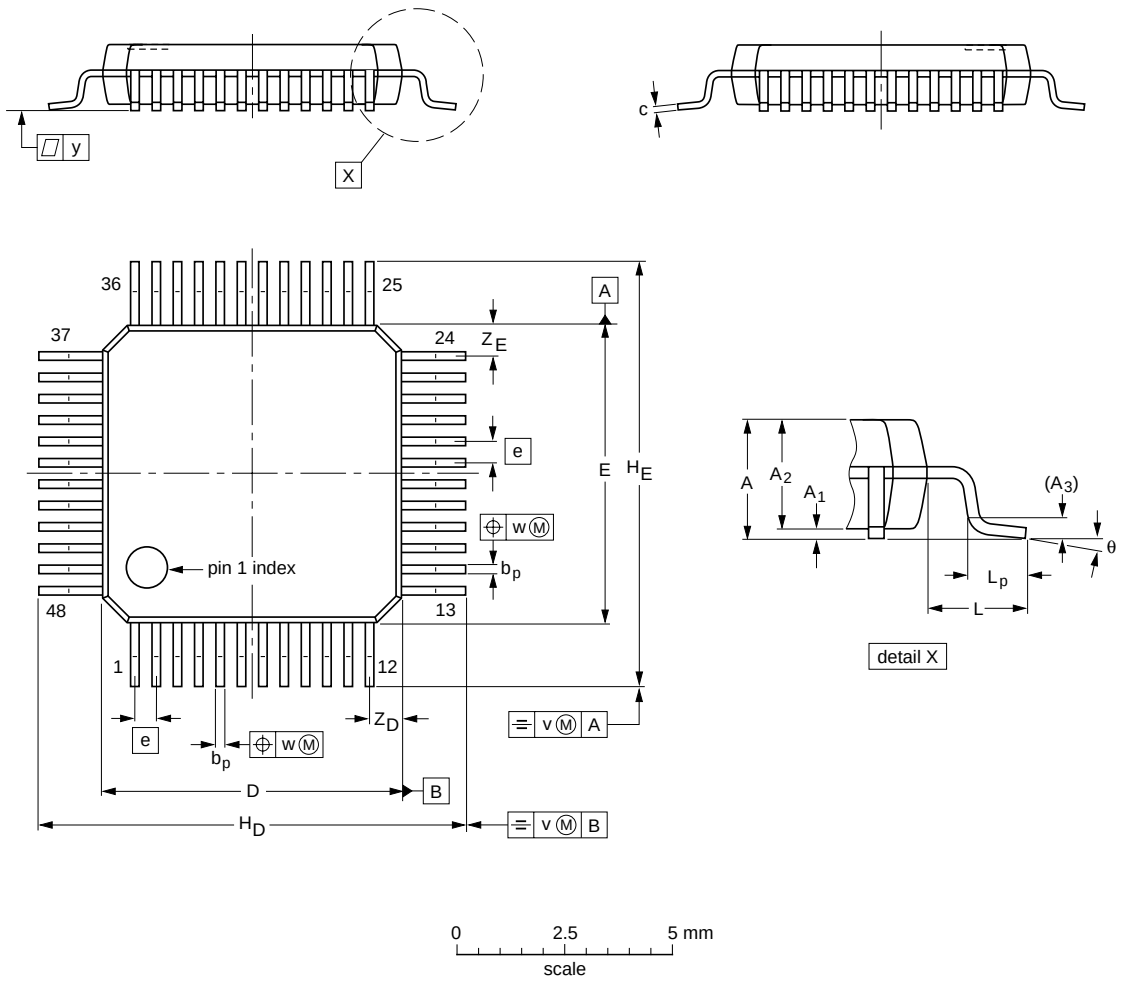


Fig 20. SPI master timing (CPHA = 0)

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 27. Package outline SOT313-2 (LQFP48)

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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