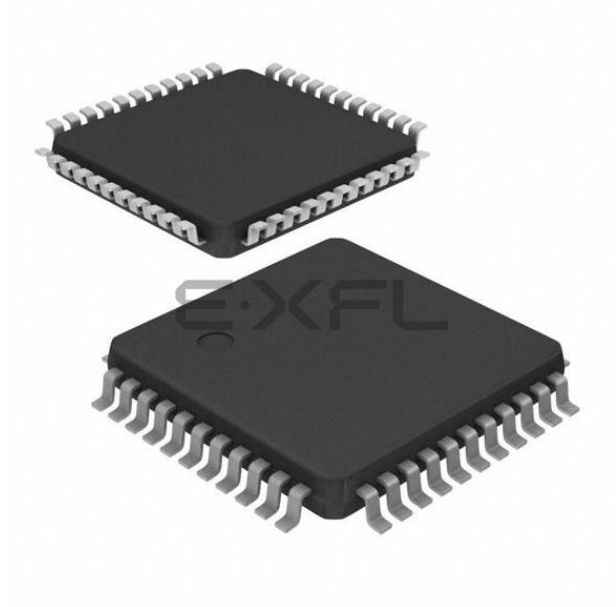

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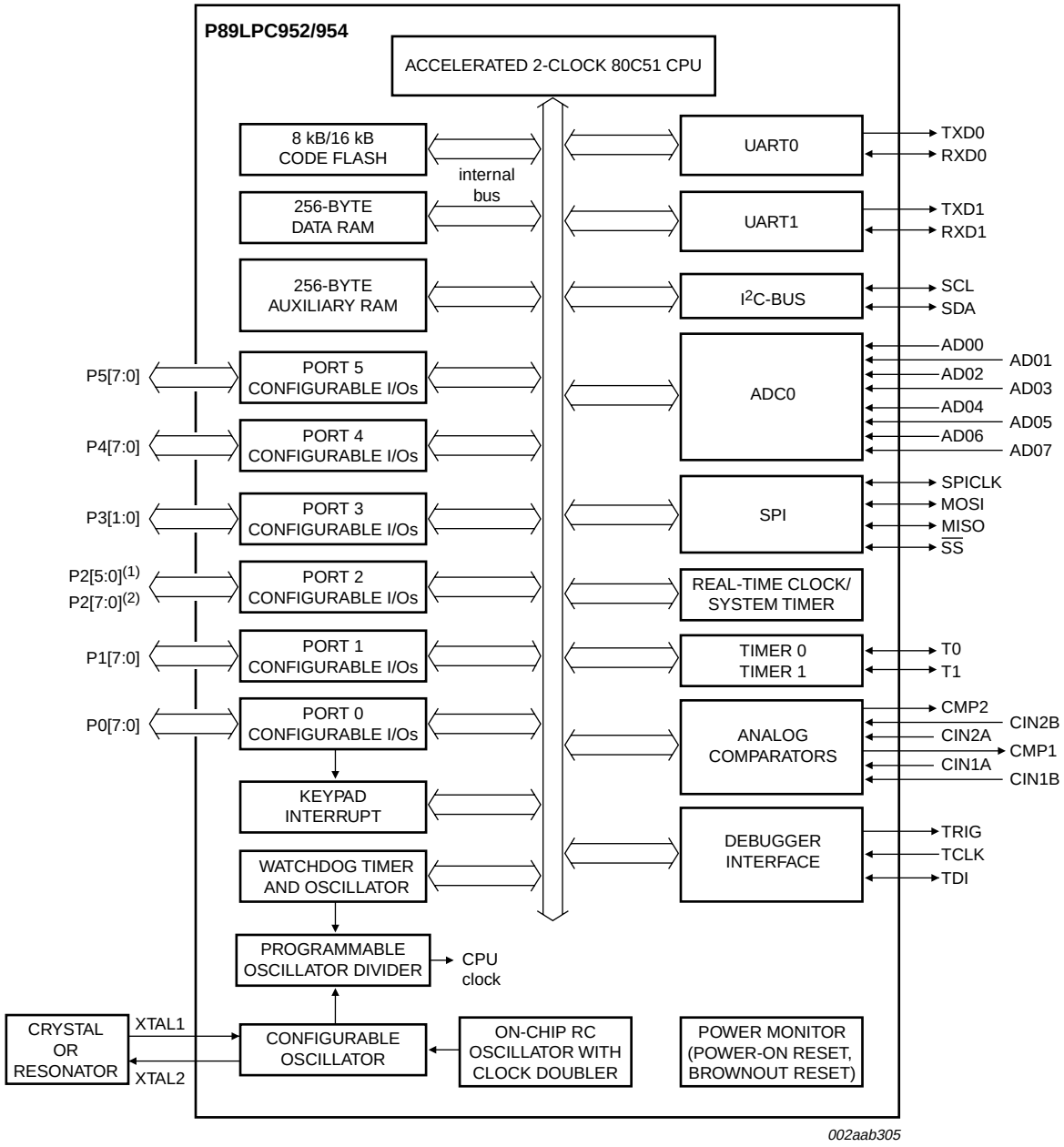
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc952fbd-157

2.2 Additional features

- A high performance 80C51 CPU provides instruction cycle times of 111 ns to 222 ns for all instructions except multiply and divide when executing at 18 MHz. This is six times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.
- Serial flash In-Circuit Programming (ICP) allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Serial flash In-System Programming (ISP) allows coding while the device is mounted in the end application.
- In-Application Programming (IAP) of the flash code memory. This allows changing the code in a running application.
- Low voltage (brownout) detect allows a graceful system shutdown when power fails. May optionally be configured as an interrupt.
- Idle and two different power-down reduced power modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical power-down current is 1 μA (total power-down with voltage comparators disabled).
- On-chip power-on reset allows operation without external reset components. A software reset function is also available.
- Programmable external reset pin (P1.5) configuration options: open drain bidirectional reset input/output, reset input with pull-up, push-pull reset output, input-only port. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets.
- Only power and ground connections are required to operate the P89LPC952/954 when internal reset option is selected.
- Configurable on-chip oscillator with frequency range options selected by user programmed flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz.
- Oscillator fail detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.
- Port ‘input pattern match’ detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Four interrupt priority levels.
- Eight keypad interrupt inputs, plus two additional external interrupt inputs.
- Schmitt trigger port inputs.
- Second data pointer.
- Extended temperature range.
- Emulation support.

4. Block diagram



(1) 44-pin package.

(2) 48-pin package.

Fig 1. Block diagram

6.2 Pin description

Table 3. Pin description

Symbol	Pin			Type	Description
	LQFP48	PLCC44	LQFP44		
P0.0 to P0.7				I/O	**Port 0:** Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 “Port configurations” and Table 11 “Static characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
P0.0/CMP2/ KBI0/AD05	40	43	37	I/O	**P0.0 —** Port 0 bit 0.
				O	**CMP2 —** Comparator 2 output.
				I	**KBI0 —** Keyboard input 0.
				I	**AD05 —** ADC0 channel 5 analog input.
P0.1/CIN2B/ KBI1/AD00	39	42	36	I/O	**P0.1 —** Port 0 bit 1.
				I	**CIN2B —** Comparator 2 positive input B.
				I	**KBI1 —** Keyboard input 1.
				I	**AD00 —** ADC0 channel 0 analog input.
P0.2/CIN2A/ KBI2/AD01	38	41	35	I/O	**P0.2 —** Port 0 bit 2.
				I	**CIN2A —** Comparator 2 positive input A.
				I	**KBI2 —** Keyboard input 2.
				I	**AD01 —** ADC0 channel 1 analog input.
P0.3/CIN1B/ KBI3/AD02	37	40	34	I/O	**P0.3 —** Port 0 bit 3.
				I	**CIN1B —** Comparator 1 positive input B.
				I	**KBI3 —** Keyboard input 3.
				I	**AD02 —** ADC0 channel 2 analog input.
P0.4/CIN1A/ KBI4/AD03	36	39	33	I/O	**P0.4 —** Port 0 bit 4.
				I	**CIN1A —** Comparator 1 positive input A.
				I	**KBI4 —** Keyboard input 4.
				I	**AD03 —** ADC0 channel 3 analog input.
P0.5/CMPREF/ KBI5	35	38	32	I/O	**P0.5 —** Port 0 bit 5.
				I	**CMPREF —** Comparator reference (negative) input.
				I	**KBI5 —** Keyboard input 5.

Table 3. Pin description *...continued*

Symbol	Pin			Type	Description
	LQFP48	PLCC44	LQFP44		
P0.6/CMP1/KBI6	34	37	31	I/O	**P0.6 —** Port 0 bit 6.
				O	**CMP1 —** Comparator 1 output.
				I	**KBI6 —** Keyboard input 6.
P0.7/T1/KBI7	31	35	29	I/O	**P0.7 —** Port 0 bit 7.
				I/O	**T1 —** Timer/counter 1 external count input or overflow output.
				I	**KBI7 —** Keyboard input 7.
P1.0 to P1.7				I/O, I [1]	**Port 1:** Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 7.13.1 "Port configurations" and Table 11 "Static characteristics" for details. P1.2 to P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.0/TXD0	4	10	4	I/O	**P1.0 —** Port 1 bit 0.
				O	**TXD0 —** Transmitter output for serial port 0.
P1.1/RXD0	3	9	3	I/O	**P1.1 —** Port 1 bit 1.
				I	**RXD0 —** Receiver input for serial port 0.
P1.2/T0/SCL	2	8	2	I/O	**P1.2 —** Port 1 bit 2 (open-drain when used as output).
				I/O	**T0 —** Timer/counter 0 external count input or overflow output (open-drain when used as output).
				I/O	**SCL —** I^2C-bus serial clock input/output.
P1.3/$\overline{INT0}$/SDA	1	7	1	I/O	**P1.3 —** Port 1 bit 3 (open-drain when used as output).
				I	**$\overline{INT0}$ —** External interrupt 0 input.
				I/O	**SDA —** I^2C-bus serial data input/output.
P1.4/$\overline{INT1}$	48	6	44	I/O	**P1.4 —** Port 1 bit 4.
				I	**$\overline{INT1}$ —** External interrupt 1 input.

Table 3. Pin description *...continued*

Symbol	Pin			Type	Description
	LQFP48	PLCC44	LQFP44		
P1.5/$\overline{\text{RST}}$	47	5	43	I	**P1.5 —** Port 1 bit 5 (input only).
				I	**$\overline{\text{RST}}$ —** External Reset input during power-on or maybe a reset input/output if selected via UCFG1 and UCFG2. When functioning as a reset input or input/output, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. When functioning as a reset output or input/output an internal reset source will drive this pin LOW. Also used during a power-on sequence to force ISP mode. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**
P1.6	46	4	42	I/O	**P1.6 —** Port 1 bit 6.
P1.7/AD04	43	2	40	I/O	**P1.7 —** Port 1 bit 7.
				I	**AD04 —** ADC0 channel 4 analog input.
P2.0 to P2.5				I/O	**Port 2:** Port 2 is an 8-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 “Port configurations” and Table 11 “Static characteristics” for details. All pins have Schmitt triggered inputs. Port 2 also provides various special functions as described below:
P2.0/AD07	42	1	39	I/O	**P2.0 —** Port 2 bit 0.
				I	**AD07 —** ADC0 channel 7 analog input.
P2.1/AD06	41	44	38	I/O	**P2.1 —** Port 2 bit 1.
				I	**AD06 —** ADC0 channel 6 analog input.
P2.2/MOSI	30	34	28	I/O	**P2.2 —** Port 2 bit 2.
				I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.3/MISO	29	33	27	I/O	**P2.3 —** Port 2 bit 3.
				I/O	**MISO —** When configured as master, this pin is input, when configured as slave, this pin is output.
P2.4/$\overline{\text{SS}}$	28	32	26	I/O	**P2.4 —** Port 2 bit 4.
				I/O	**$\overline{\text{SS}}$ —** SPI Slave select.

Table 4. Special function registers *…continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
DPH	Data pointer high	83H									00	0000 0000
DPL	Data pointer low	82H									00	0000 0000
FMADRH	Program flash address high	E7H									00	0000 0000
FMADRL	Program flash address low	E6H									00	0000 0000
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash control (Write)	E4H	FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program flash data	E5H									00	0000 0000
I2ADR	I^2C-bus slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	0000 0000
	Bit address		**DF**	**DE**	**DD**	**DC**	**DB**	**DA**	**D9**	**D8**		
I2CON[1]	I^2C-bus control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x000 00x0
I2DAT	I^2C-bus data register	DAH										
I2SCLH	Serial clock generator/SCL duty cycle register high	DDH									00	0000 0000
I2SCLL	Serial clock generator/SCL duty cycle register low	DCH									00	0000 0000
I2STAT	I^2C-bus status register	D9H	STA.4	STA.3	STA.2	STA.1	STA.0	0	0	0	F8	1111 1000

Table 4. Special function registers *...continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	97	96	95	94	93	92	91	90		
P2[1]	Port 2	A0H	-	-	SPICLK	$\overline{SS}$	MISO	MOSI	-	-	[2]	
		Bit address	B7	B6	B5	B4	B3	B2	B1	B0		
P3[1]	Port 3	B0H	-	-	-	-	-	-	XTAL1	XTAL2	[2]	
P4	Port 4	B3H	-	TMS	-	-	RXD1	TXD1	TRIG	T3EX	[2]	
P5	Port 5	B4H	T3	-	-	-	-	-	-	-	[2]	
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF[2]	1111 1111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00[2]	0000 0000
P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3[2]	11x1 xx11
P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00[2]	00x0 xx00
P2M1	Port 2 output mode 1	A4H	(P2M1.7)	(P2M1.6)	(P2M1.5)	(P2M1.4)	(P2M1.3)	(P2M1.2)	(P2M1.1)	(P2M1.0)	FF[2]	1111 1111
P2M2	Port 2 output mode 2	A5H	(P2M2.7)	(P2M2.6)	(P2M2.5)	(P2M2.4)	(P2M2.3)	(P2M2.2)	(P2M2.1)	(P2M2.0)	00[2]	0000 0000
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03[2]	xxxx xx11
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00[2]	xxxx xx00
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD	-	VCPD	ADPD	I2PD	SPPD	SPD	-	00[2]	0000 0000
		Bit address	D7	D6	D5	D4	D3	D2	D1	D0		
PSW[1]	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00 000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX	[4]	

Table 4. Special function registers *...continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
RTCCON	RTC control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[2][7]	011x xx00
RTCH	RTC register high	D2H									00[7]	0000 0000
RTCL	RTC register low	D3H									00[7]	0000 0000
S0ADDR	Serial port address register	A9H									00	0000 0000
S0ADEN	Serial port address enable	B9H									00	0000 0000
S0BUF	Serial Port data buffer register	99H									xx	xxxx xxxx
	Bit address		**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**		
S0CON[1]	Serial port control	98H	SM0_0/FE_0	SM1_00	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	00	0000 0000
S0STAT	Serial port extended status register	BAH	DBMOD_0	INTLO_0	CIDIS_0	DBISEL_0	FE_0	BR_0	OE_0	STINT_0	00	0000 0000
SP	Stack pointer	81H									07	0000 0111
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04	0000 0100
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-	-	00	00xx xxxx
SPDAT	SPI data register	E3H									00	0000 0000
S1CON	Serial port 1 control	B6H	SM0_1/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	00	0000 0000
S1STAT	Serial port 1 extended status register	D4H	DBMOD_1	INTLO_1	CIDIS_1	DBISEL_1	FE_1	BR_1	OE_1	STINT_1	00	0000 0000
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0 xxx0

Table 5. Extended special function registers *…continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
AD0DAT7L	ADC0 data register 7, left (MSB)	FFF1H	AD0DAT7[9:2]									
BNDSTA0	ADC0 boundary status register	FFEDH										
BRGCON_1	Baud rate generator 1 control	FFB3H	-	-	-	-	-	-	SBRGS_1	BRGEN_1	00[2]	xxxx xx00
BRG0_1	Baud rate generator 1 rate low	FFB4H										
BRG1_1	Baud rate generator 1 rate high	FFB5H										
FREEZE	Peripheral clock freeze	FFD0H	-	-	-	RTC_F	CCU_F	WDT_F	T1_F	T0_F	00	xxx0 0000
P4M1	Port 4 output mode 1	FFB8H	(P4M1.7)	(P4M1.6)	(P4M1.5)	(P4M1.4)	(P4M1.3)	(P4M1.2)	(P4M1.1)	(P4M1.0)	FF[1]	1111 1111
P4M2	Port 4 output mode 2	FFB9H	(P4M2.7)	(P4M2.6)	(P4M2.5)	(P4M2.4)	(P4M2.3)	(P4M2.2)	(P4M2.1)	(P4M2.0)	00[1]	0000 0000
P5M1	Port 5 output mode 1	FFBAH	(P5M1.7)	(P5M1.6)	(P5M1.5)	(P5M1.4)	(P5M1.3)	(P5M1.2)	(P5M1.1)	(P5M1.0)	FF[1]	1111 1111
P5M2	Port 5 output mode 3	FFBBH	(P5M2.7)	(P5M2.6)	(P5M2.5)	(P5M2.4)	(P5M2.3)	(P5M2.2)	(P5M2.1)	(P5M2.0)	00[1]	0000 0000
S1ADDR	Serial port 1 address register	FFB2H									00	0000 0000
S1ADEN	Serial port 1 address enable	FFB1H									00	0000 0000
S1BUF	Serial port 1 data buffer register	FFB0H									xx	xxxx xxxx

[1] Extended SFRs are physically located on-chip but logically located in external data memory address space (XDATA). The MOVX A,@DPTR and MOVX @DPTR,A instructions are used to access these extended SFRs.

[2] BRGR1_1 and BRGR0_1 must only be written if BRGEN_1 in BRGCON_1 SFR is logic 0. If any are written while BRGEN_1 = 1, the result is unpredictable.

An open-drain port pin has a Schmitt triggered input that also has a glitch suppression circuit.

7.13.1.3 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt triggered input that also has a glitch suppression circuit.

7.13.1.4 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt triggered input that also has a glitch suppression circuit.

7.13.2 Port 0 analog functions

The P89LPC952/954 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high-impedance) mode.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register, bits 1:5. On any reset, PT0AD[1:5] defaults to ‘0’s to enable digital functions.

7.13.3 Additional port features

After power-up, all pins are in Input-Only mode. **Please note that this is different from the LPC76x series of devices.**

- After power-up, all I/O pins except P1.5, may be configured by software.
- Pin P1.5 is input only. Pins P1.2 and P1.3 are configurable for either input-only or open-drain.

Every output on the P89LPC952/954 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to Table 11 for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

7.14 Power monitoring functions

The P89LPC952/954 incorporates power monitoring functions designed to prevent incorrect operation during initial power-up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-on detect and brownout detect.

7.14.1 Brownout detection

The brownout detect function determines if the power supply voltage drops below a certain level. The default operation is for a brownout detection to cause a processor reset, however it may alternatively be configured to generate an interrupt.

7.16 Reset

The P1.5/$\overline{\text{RST}}$ pin can function as either a digital input (P1.5), an active-LOW reset input with an internal pull-up, a bidirectional reset input/output (open drain output with an internal pull-up), or as push-pull reset output. These modes are selected by the RPE (Reset Pin Enable) bit in UCFG1 and the RPE1 (Reset Pin Enable 1) bit in UCFG2.

Table 8. Reset pin modes

P1.5/$\overline{\text{RST}}$ mode	RPE1 (UCFG2.0)	RPE (UCFG1.6)
General purpose input	0	0
Reset input with pull-up	0	1
Bidirectional reset input/output (open drain with pull-up)	1	0
Reset output	1	1

Remark: During a power-up sequence, the RPE and RPE1 selection is overridden and this pin always functions as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this pin will function as defined by the RPE and RPE1 bits. Only a power-up reset will temporarily override the selection defined by RPE and RPE1 bits. Other sources of reset will not override the RPE and RPE1 bits.

Remark: During a power cycle, V_{DD} must fall below V_{POR} before power is reapplied, in order to ensure a power-on reset (see Table 11 “Static characteristics” on page 51).

Remark: When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user configured via UCFG1, UCGF2);
- Power-on detect;
- Brownout detect;
- Watchdog timer;
- Software reset;
- UART break character detect reset.

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a ‘0’ to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

Double buffering can be disabled. If disabled (DBMOD_n, i.e., SnSTAT.7 = 0), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SnBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD_n = 0).

7.19.9 Transmit interrupts with double buffering enabled (Modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the TI_n interrupt is generated when the double buffer is ready to receive new data.

7.19.10 The 9th bit (bit 8) in double buffering (Modes 1, 2 and 3)

If double buffering is disabled TB8_n can be written before or after SnBUF is written, as long as TB8_n is updated some time before that bit is shifted out. TB8_n must not be changed until the bit is shifted out, as indicated by the TI_n interrupt.

If double buffering is enabled, TB8_n **must** be updated before SnBUF is written, as TB8_n will be double-buffered together with SnBUF data.

7.20 I²C-bus serial interface

I²C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bidirectional data transfer between masters and slaves
- Multi master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I²C-bus may be used for test and diagnostic purposes.

A typical I²C-bus configuration is shown in Figure 9. The P89LPC952/954 device provides a byte-oriented I²C-bus interface that supports data transfers up to 400 kHz.

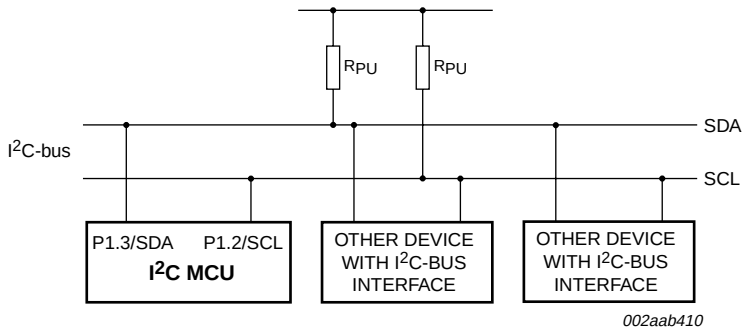


Fig 9. I²C-bus configuration

7.21 SPI

The P89LPC952/954 provides another high-speed serial communication interface — the SPI interface. SPI is a full-duplex, high-speed, synchronous communication bus with two operation modes: Master mode and Slave mode. Up to 3 Mbit/s can be supported in either Master or Slave mode. It has a Transfer Completion Flag and Write Collision Flag Protection.

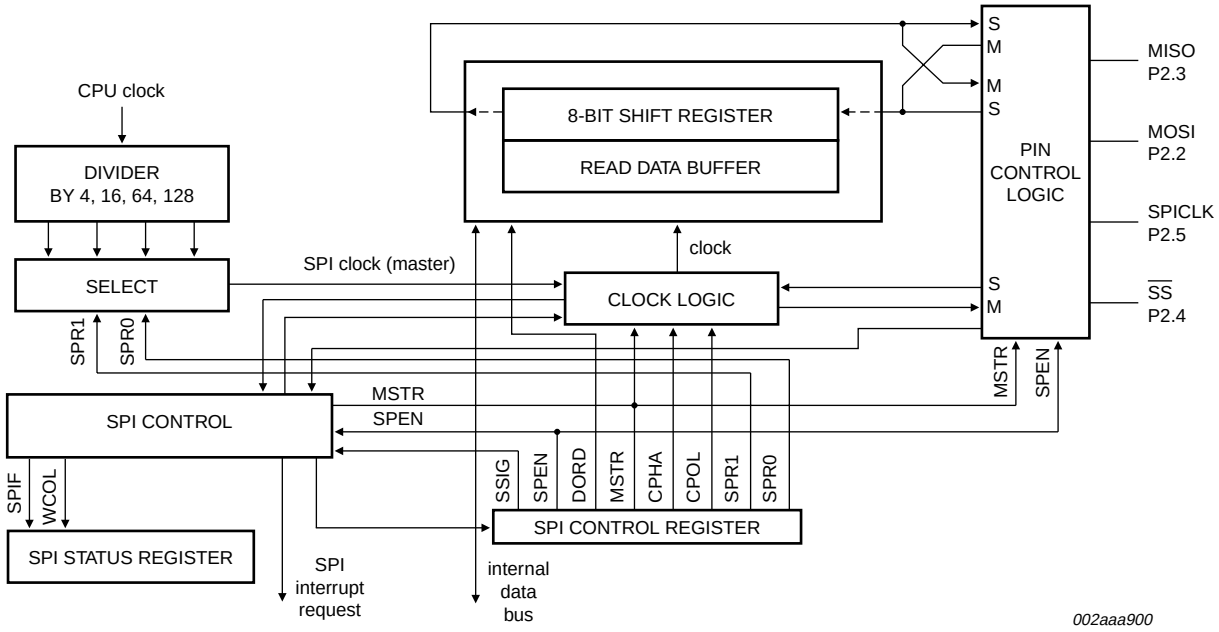


Fig 11. SPI block diagram

The SPI interface has four pins: SPICLK, MOSI, MISO and $\overline{SS}$:

- SPICLK, MOSI and MISO are typically tied together between two or more SPI devices. Data flows from master to slave on MOSI (Master Out Slave In) pin and flows from slave to master on MISO (Master In Slave Out) pin. The SPICLK signal is output in the Master mode and is input in the Slave mode. If the SPI system is disabled, i.e., SPEN (SPCTL.6) = 0 (reset value), these pins are configured for port functions.
- $\overline{SS}$ is the optional slave select pin. In a typical configuration, an SPI master asserts one of its port pins to select one SPI device as the current slave. An SPI slave device uses its $\overline{SS}$ pin to determine whether it is selected.

Typical connections are shown in Figure 12 through Figure 14.

7.26.9 Power-on reset code execution

The P89LPC952/954 contains two special flash elements: the Boot Vector and the Boot Status bit. Following reset, the P89LPC952/954 examines the contents of the Boot Status bit. If the Boot Status bit is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the Boot Status bit is set to a value other than zero, the contents of the Boot Vector are used as the high byte of the execution address and the low byte is set to 00H.

Table 9 shows the factory default Boot Vector setting for these devices. A factory-provided bootloader is pre-programmed into the address space indicated and uses the indicated bootloader entry point to perform ISP functions. This code can be erased by the user. **Users who wish to use this loader should take precautions to avoid erasing the 1 kB sector that contains this bootloader. Instead, the page erase function can be used to erase the first eight 64-byte pages located in this sector.** A custom bootloader can be written with the Boot Vector set to the custom bootloader, if desired.

Table 9. Default boot vector values and ISP entry points

Device	Default boot vector	Default bootloader entry point	Default bootloader code range	1 kB sector range
P89LPC952	1FH	1F00H	1E00H to 1FFFH	1C00H to 1FFFH
P89LPC954	3FH	3F00H	3E00H to 3FFFH	3C00H to 3FFFH

7.26.10 Hardware activation of the bootloader

The bootloader can also be executed by forcing the device into ISP mode during a power-on sequence (see the P89LPC952/954 *User's Manual* for specific information). This has the same effect as having a non-zero status byte. This allows an application to be built that will normally execute user code but can be manually forced into ISP operation. If the factory default setting for the boot vector (1FH/3FH) is changed, it will no longer point to the factory pre-programmed ISP bootloader code. After programming the flash, the status byte should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

7.27 User configuration bytes

Some user-configurable features of the P89LPC952/954 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the flash byte UCFG1. Please see the P89LPC952/954 *User's Manual* for additional details.

7.28 User sector security bytes

There are eight/sixteen User Sector Security Bytes on the P89LPC952/954. Each byte corresponds to one sector. Please see the P89LPC952/954 *User's Manual* for additional details.

10. Static characteristics

Table 11. Static characteristics

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(oper)}$	operating supply current	V_{DD} = 3.6 V; f_{osc} = 12 MHz	[2]	-	11	18	mA
		V_{DD} = 3.6 V; f_{osc} = 18 MHz	[2]	-	14	23	mA
$I_{DD(idle)}$	Idle mode supply current	V_{DD} = 3.6 V; f_{osc} = 12 MHz	[2]	-	3.25	5	mA
		V_{DD} = 3.6 V; f_{osc} = 18 MHz	[2]	-	5	7	mA
$I_{DD(pd)}$	Power-down mode supply current	V_{DD} = 3.6 V; voltage comparators powered down	[2]	-	55	80	µA
$I_{DD(tpd)}$	total Power-down mode supply current	V_{DD} = 3.6 V	[3]	-	0.5	5	µA
$(dV/dt)_r$	rise rate	of V_{DD}		-	-	2	mV/µs
$(dV/dt)_f$	fall rate	of V_{DD}		-	-	50	mV/µs
V_{POR}	power-on reset voltage			-	-	0.5	V
V_{DDR}	data retention supply voltage			1.5	-	-	V
$V_{th(HL)}$	HIGH-LOW threshold voltage	except SCL, SDA		$0.22V_{DD}$	$0.4V_{DD}$	-	V
V_{IL}	LOW-level input voltage	SCL, SDA only		−0.5	-	$0.3V_{DD}$	V
$V_{th(LH)}$	LOW-HIGH threshold voltage	except SCL, SDA		-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{IH}	HIGH-level input voltage	SCL, SDA only		$0.7V_{DD}$	-	5.5	V
V_{hys}	hysteresis voltage	port 1		-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 20 mA; V_{DD} = 2.4 V to 3.6 V all ports, all modes except high-Z	[4]	-	0.6	1.0	V
		I_{OL} = 3.2 mA; V_{DD} = 2.4 V to 3.6 V all ports, all modes except high-Z	[4]	-	0.2	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = −20 µA; V_{DD} = 2.4 V to 3.6 V; all ports, quasi-bidirectional mode		V_{DD} − 0.3	V_{DD} − 0.2	-	V
		I_{OH} = −3.2 mA; V_{DD} = 2.4 V to 3.6 V; all ports, push-pull mode		V_{DD} − 0.7	V_{DD} − 0.4	-	V
		I_{OH} = −20 mA; V_{DD} = 2.4 V to 3.6 V; Port 5, push-pull mode		$0.8V_{DD}$	-	-	V
V_{xtal}	crystal voltage	on XTAL1, XTAL2 pins; with respect to V_{SS}		−0.5	-	+4.0	V
V_n	voltage on any other pin	except XTAL1, XTAL2, V_{DD}; with respect to V_{SS}	[5]	−0.5	-	+5.5	V

Table 11. Static characteristics *…continued*

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
C_{iss}	input capacitance		[6]	-	-	15	pF
I_{IL}	LOW-level input current	V_I = 0.4 V	[7]	-	-	−80	µA
I_{LI}	input leakage current	$V_I = V_{IL}$, V_{IH}, or $V_{th(HL)}$	[8]	-	-	±1	µA
I_{THL}	HIGH-LOW transition current	all ports; V_I = 1.5 V at V_{DD} = 3.6 V	[9]	−30	-	−450	µA
$R_{RST\_N(int)}$	internal pull-up resistance on pin $\overline{RST}$	pin $\overline{RST}$		10	-	30	kΩ
V_{bo}	brownout trip voltage	BOE = 1		2.4	-	2.7	V
$V_{ref(bg)}$	band gap reference voltage			1.19	1.23	1.27	V
TC_{bg}	band gap temperature coefficient			-	10	20	ppm/°C

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] The $I_{DD(oper)}$, $I_{DD(idle)}$, and $I_{DD(pd)}$ specifications are measured using an external clock with the following functions disabled: comparators, real-time clock, and watchdog timer.

[3] The $I_{DD(tpd)}$ specification is measured using an external clock with the following functions disabled: comparators, real-time clock, brownout detect, and watchdog timer.

[4] See Section 9 “Limiting values” for steady state (non-transient) limits on I_{OL} or I_{OH}. If I_{OL}/I_{OH} exceeds the test condition, V_{OL}/V_{OH} may exceed the related specification.

[5] This specification can be applied to pins which have A/D input or analog comparator input functions when the pin is not being used for those analog functions. When the pin is being used as an analog input pin, the maximum voltage on the pin must be limited to 4.0 V with respect to V_{SS}.

[6] Pin capacitance is characterized but not tested.

[7] Measured with port in quasi-bidirectional mode.

[8] Measured with port in high-impedance mode.

[9] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

Table 12. Dynamic characteristics (12 MHz) *…continued*

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
T_{SPICYC}	SPI cycle time	see Figure 20, 21, 22, 23					
	slave		$^{6}/_{CCLK}$	-	500	-	ns
	master		$^{4}/_{CCLK}$	-	333	-	ns
$t_{SPILEAD}$	SPI enable lead time	see Figure 22, 23					
	slave		250	-	250	-	ns
t_{SPILAG}	SPI enable lag time	see Figure 22, 23					
	slave		250	-	250	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 20, 21, 22, 23					
	master		$^{2}/_{CCLK}$	-	165	-	ns
	slave		$^{3}/_{CCLK}$	-	250	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 20, 21, 22, 23					
	master		$^{2}/_{CCLK}$	-	165	-	ns
	slave		$^{3}/_{CCLK}$	-	250	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 20, 21, 22, 23					
	master or slave		100	-	100	-	ns
t_{SPIDH}	SPI data hold time	see Figure 20, 21, 22, 23					
	master or slave		100	-	100	-	ns
t_{SPIA}	SPI access time	see Figure 22, 23					
	slave		0	120	0	120	ns
t_{SPIDIS}	SPI disable time	see Figure 22, 23					
	slave		0	240	-	240	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 20, 21, 22, 23					
	slave		-	240	-	240	ns
	master		-	167	-	167	ns
t_{SPIOH}	SPI output data hold time	see Figure 20, 21, 22, 23	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 20, 21, 22, 23					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 20, 21, 22, 23					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

Table 13. Dynamic characteristics (18 MHz)

V_{DD} = 3.0 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	nominal f = 7.3728 MHz trimmed to ± 1 % at T_{amb} = 25 °C; clock doubler option = OFF (default)	7.189	7.557	7.189	7.557	MHz
		nominal f = 14.7456 MHz; clock doubler option = ON	14.378	15.114	14.378	15.114	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency		320	520	320	520	kHz
f_{osc}	oscillator frequency		0	18	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 19	55	-	-	-	ns
f_{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection time	P1.5/$\overline{RST}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{RST}$	-	15	-	15	ns
t_{sa}	signal acceptance time	P1.5/$\overline{RST}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{RST}$	50	-	50	-	ns
External clock							
t_{CHCX}	clock HIGH time	see Figure 19	22	$T_{cy(clk)} - t_{CLCX}$	22	-	ns
t_{CLCX}	clock LOW time	see Figure 19	22	$T_{cy(clk)} - t_{CHCX}$	22	-	ns
t_{CLCH}	clock rise time	see Figure 19	-	5	-	5	ns
t_{CHCL}	clock fall time	see Figure 19	-	5	-	5	ns
Shift register (UART mode 0)							
T_{XLXL}	serial port clock cycle time	see Figure 18	$16T_{cy(clk)}$	-	888	-	ns
t_{QVXH}	output data set-up to clock rising edge time	see Figure 18	$13T_{cy(clk)}$	-	722	-	ns
t_{XHQX}	output data hold after clock rising edge time	see Figure 18	-	$T_{cy(clk)}$ + 20	-	75	ns
t_{XHDX}	input data hold after clock rising edge time	see Figure 18	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge time	see Figure 18	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	slave		0	$^{CCLK}/_{6}$	0	3.0	MHz
	master		-	$^{CCLK}/_{4}$	-	4.5	MHz
T_{SPICYC}	SPI cycle time	see Figure 20, 21, 22, 23					
	slave		$^{6}/_{CCLK}$	-	333	-	ns
	master		$^{4}/_{CCLK}$	-	222	-	ns

12. Other characteristics

12.1 Comparator electrical characteristics

Table 15. Comparator electrical characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IO}	input offset voltage		-	-	±10	mV
V_{IC}	common-mode input voltage		0	-	V_{DD} − 0.3	V
CMRR	common-mode rejection ratio	[1]	-	-	−50	dB
$t_{res(tot)}$	total response time		-	250	500	ns
$t_{(CE-OV)}$	chip enable to output valid time		-	-	10	µs
I_{LI}	input leakage current	0 V < V_I < V_{DD}	-	-	±10	µA

[1] This parameter is characterized, but not tested in production.

14. Abbreviations

Table 17. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
BOE	BrownOut Enable
CPU	Central Processing Unit
CCU	Capture/Compare Unit
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
EPROM	Erasable Programmable Read-Only Memory
EMI	ElectroMagnetic Interference
IAP	In-Application Programming
LSB	Least Significant Bit
MSB	Most Significant Bit
PWM	Pulse Width Modulator
RAM	Random Access Memory
RC	Resistance-Capacitance
RTC	Real-Time Clock
SAR	Successive Approximation Register
SFR	Special Function Register
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter