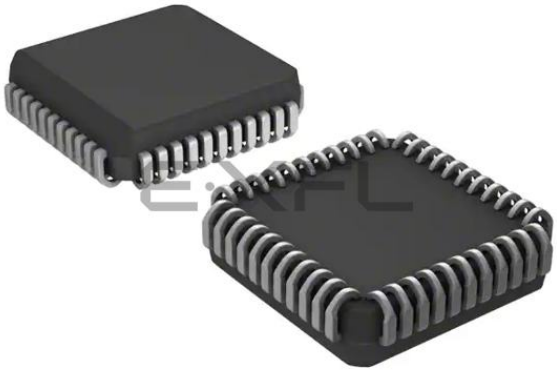

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc954fa-529

3. Ordering information

Table 1. Ordering information

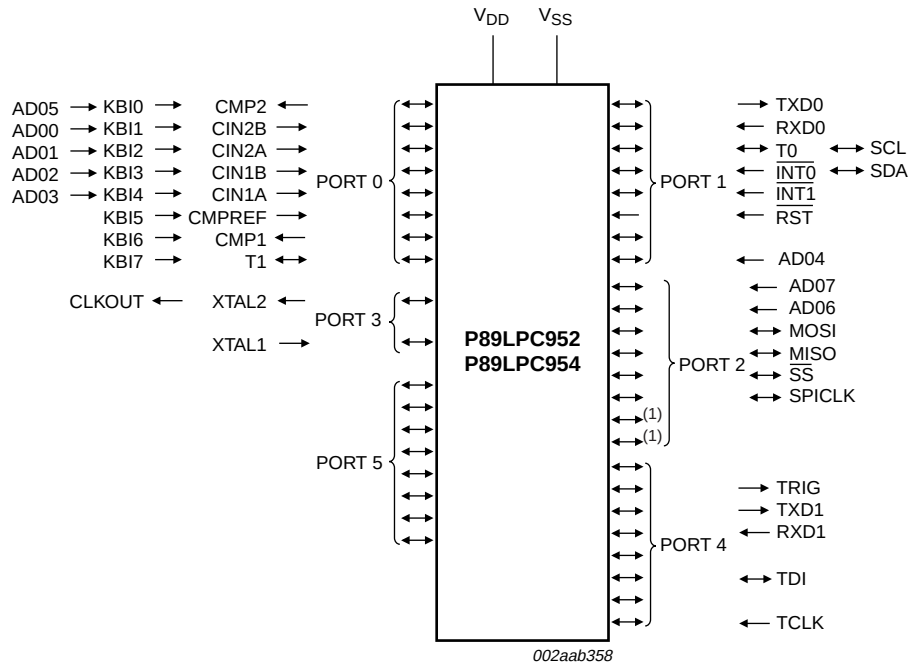
Type number	Package		
	Name	Description	Version
P89LPC952FA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2
P89LPC952FBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 × 10 × 1.4 mm	SOT389-1
P89LPC954FA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2
P89LPC954FBD44	LQFP44	plastic low profile quad flat package; 44 leads; body 10 × 10 × 1.4 mm	SOT389-1
P89LPC954FBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	Temperature range	Frequency
P89LPC952FA	8 kB	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC952FBD	8 kB	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC954FA	16 kB	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC954FBD44	16 kB	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC954FBD48	16 kB	–40 °C to +85 °C	0 MHz to 18 MHz

5. Functional diagram



(1) 48-pin package.

Fig 2. Functional diagram

6. Pinning information

6.1 Pinning

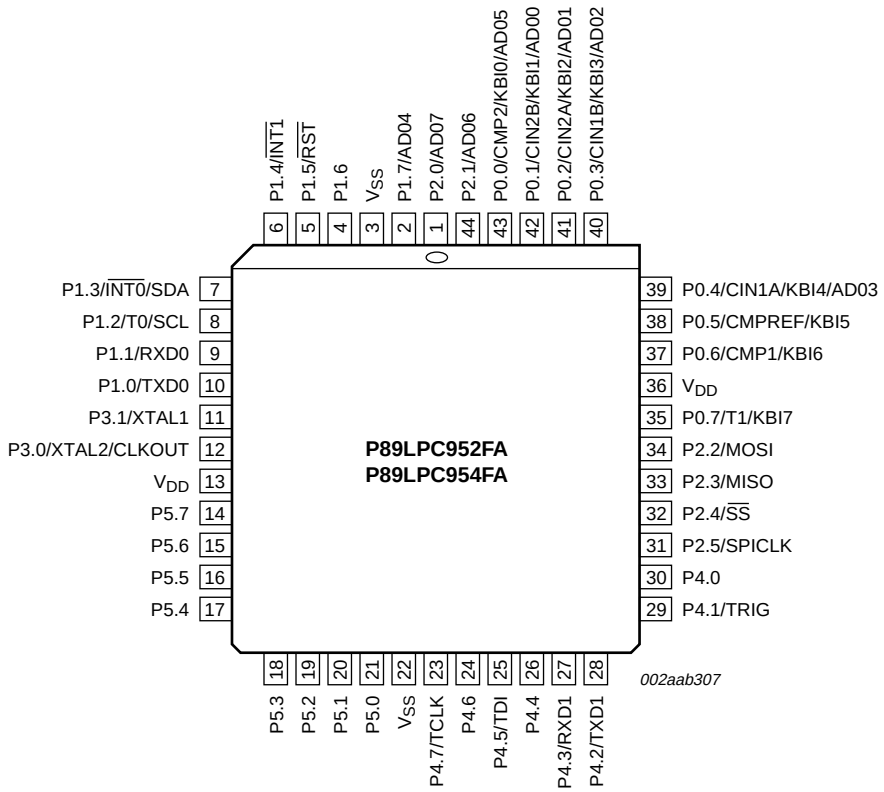


Fig 3. PLCC44 pin configuration

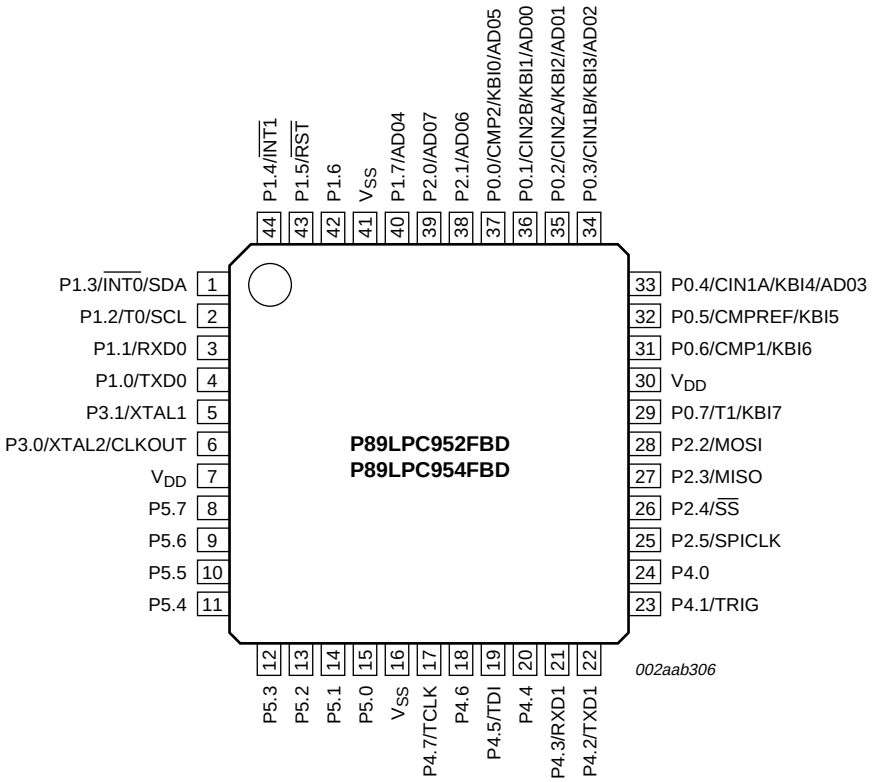


Fig 4. LQFP44 pin configuration

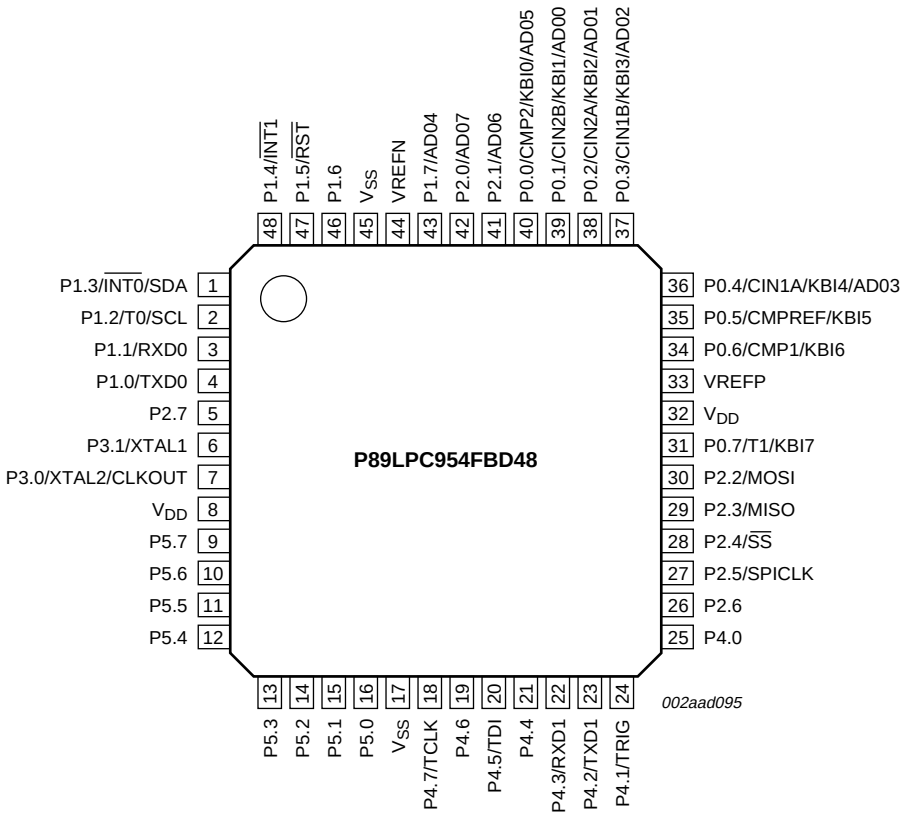


Fig 5. LQFP48 pin configuration

Table 3. Pin description *...continued*

Symbol	Pin			Type	Description
	LQFP48	PLCC44	LQFP44		
P0.6/CMP1/KBI6	34	37	31	I/O	**P0.6 —** Port 0 bit 6.
				O	**CMP1 —** Comparator 1 output.
				I	**KBI6 —** Keyboard input 6.
P0.7/T1/KBI7	31	35	29	I/O	**P0.7 —** Port 0 bit 7.
				I/O	**T1 —** Timer/counter 1 external count input or overflow output.
				I	**KBI7 —** Keyboard input 7.
P1.0 to P1.7				I/O, I [1]	**Port 1:** Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 7.13.1 "Port configurations" and Table 11 "Static characteristics" for details. P1.2 to P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.0/TXD0	4	10	4	I/O	**P1.0 —** Port 1 bit 0.
				O	**TXD0 —** Transmitter output for serial port 0.
P1.1/RXD0	3	9	3	I/O	**P1.1 —** Port 1 bit 1.
				I	**RXD0 —** Receiver input for serial port 0.
P1.2/T0/SCL	2	8	2	I/O	**P1.2 —** Port 1 bit 2 (open-drain when used as output).
				I/O	**T0 —** Timer/counter 0 external count input or overflow output (open-drain when used as output).
				I/O	**SCL —** I^2C-bus serial clock input/output.
P1.3/$\overline{INT0}$/SDA	1	7	1	I/O	**P1.3 —** Port 1 bit 3 (open-drain when used as output).
				I	**$\overline{INT0}$ —** External interrupt 0 input.
				I/O	**SDA —** I^2C-bus serial data input/output.
P1.4/$\overline{INT1}$	48	6	44	I/O	**P1.4 —** Port 1 bit 4.
				I	**$\overline{INT1}$ —** External interrupt 1 input.

Table 3. Pin description *...continued*

Symbol	Pin			Type	Description
	LQFP48	PLCC44	LQFP44		
P1.5/$\overline{\text{RST}}$	47	5	43	I	**P1.5 —** Port 1 bit 5 (input only).
				I	**$\overline{\text{RST}}$ —** External Reset input during power-on or maybe a reset input/output if selected via UCFG1 and UCFG2. When functioning as a reset input or input/output, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. When functioning as a reset output or input/output an internal reset source will drive this pin LOW. Also used during a power-on sequence to force ISP mode. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**
P1.6	46	4	42	I/O	**P1.6 —** Port 1 bit 6.
P1.7/AD04	43	2	40	I/O	**P1.7 —** Port 1 bit 7.
				I	**AD04 —** ADC0 channel 4 analog input.
P2.0 to P2.5				I/O	**Port 2:** Port 2 is an 8-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 “Port configurations” and Table 11 “Static characteristics” for details. All pins have Schmitt triggered inputs. Port 2 also provides various special functions as described below:
P2.0/AD07	42	1	39	I/O	**P2.0 —** Port 2 bit 0.
				I	**AD07 —** ADC0 channel 7 analog input.
P2.1/AD06	41	44	38	I/O	**P2.1 —** Port 2 bit 1.
				I	**AD06 —** ADC0 channel 6 analog input.
P2.2/MOSI	30	34	28	I/O	**P2.2 —** Port 2 bit 2.
				I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.3/MISO	29	33	27	I/O	**P2.3 —** Port 2 bit 3.
				I/O	**MISO —** When configured as master, this pin is input, when configured as slave, this pin is output.
P2.4/$\overline{\text{SS}}$	28	32	26	I/O	**P2.4 —** Port 2 bit 4.
				I/O	**$\overline{\text{SS}}$ —** SPI Slave select.

Table 3. Pin description *...continued*

Symbol	Pin			Type	Description
	LQFP48	PLCC44	LQFP44		
P4.4	21	26	20	I/O	**P4.4 —** Port 4 bit 4.
P4.5/TDI	20	25	19	I/O	**P4.5 —** Port 4 bit 5.
				I/O	**TDI —** Serial data input/output for debugger interface.
P4.6	19	24	18	I/O	**P4.6 —** Port 4 bit 6.
P4.7/TCLK	18	23	17	I/O	**P4.7 —** Port 4 bit 7.
				I	**TCLK —** Serial clock input for debugger interface.
P5.0 to P5.7				I/O	**Port 5:** Port 5 is an 8-bit I/O port with a user-configurable output type. During reset Port 5 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 5 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 “Port configurations” and Table 11 “Static characteristics” for details. All pins have Schmitt triggered inputs. Port 5 also provides various special functions as described below:
P5.0	16	21	15	I/O	**P5.0 —** Port 5 bit 0. High current source.
P5.1	15	20	14	I/O	**P5.1 —** Port 5 bit 1. High current source.
P5.2	14	19	13	I/O	**P5.2 —** Port 5 bit 2. High current source.
P5.3	13	18	12	I/O	**P5.3 —** Port 5 bit 3. High current source.
P5.4	12	17	11	I/O	**P5.4 —** Port 5 bit 4. High current source.
P5.5	11	16	10	I/O	**P5.5 —** Port 5 bit 5. High current source.
P5.6	10	15	9	I/O	**P5.6 —** Port 5 bit 6. High current source.
P5.7	9	14	8	I/O	**P5.7 —** Port 5 bit 7. High current source.
V_{SS}	17, 45	3, 22	16, 41	I	**Ground:** 0 V reference.
VREFN	44	-	-		negative ADC reference voltage
V_{DD}	8, 32	13, 36	7, 30	I	**Power supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.
VREFP	33	-	-		positive ADC reference voltage

[1] Input/output for P1.0 to P1.4, P1.6, P1.7. Input for P1.5.

Table 4. Special function registers *…continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**		
IEN0[1]	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	EX1	ET0	EX0	00	0000 0000
		Bit address	**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**	**E8**		
IEN1[1]	Interrupt enable 1	E8H	-	EST	-	-	ESPI	EC	EKBI	EI2C	00[2]	00x0 0000
IEN2	Interrupt enable 2	D5H	-	-	-	-	EST1	ES1/ESR1	EADC	-	00[2]	00x0 0000
		Bit address	**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**	**B8**		
IP0[1]	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	PX1	PT0	PX0	00[2]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/ PSRH	PT1H	PX1H	PT0H	PX0H	00[2]	x000 0000
		Bit address	**FF**	**FE**	**FD**	**FC**	**FB**	**FA**	**F9**	**F8**		
IP1[1]	Interrupt priority 1	F8H	-	PST	-	-	PSPI	PC	PKBI	PI2C	00[2]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	-	PSTH	-	-	PSPIH	PCH	PKBIH	PI2CH	00[2]	00x0 0000
IP2	Interrupt priority 2	D6H	-	-	-	-	PEST1	PES1/ PESR1	PADC	-	00[2]	00x0 0000
IP2H	Interrupt priority 2 high	D7H	-	-	-	-	PEST1H	PES1H/ PESR1H	PADCH	-	00[2]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN _SEL	KBIF	00[2]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H									00	0000 0000
KBPATN	Keypad pattern register	93H									FF	1111 1111
		Bit address	**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**		
P0[1]	Port 0	80H	T1/KB7	CMP1 /KB6	CMPREF /KB5	CIN1A /KB4	CIN1B /KB3	CIN2A /KB2	CIN2B /KB1	CMP2 /KB0	[2]	
		Bit address	**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P1[1]	Port 1	90H	-	-	$\overline{\text{RST}}$	$\overline{\text{INT1}}$	$\overline{\text{INT0}}$/SDA	T0/SCL	RXD0	TXD0	[2]	

Table 4. Special function registers *...continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	97	96	95	94	93	92	91	90		
P2[1]	Port 2	A0H	-	-	SPICLK	$\overline{SS}$	MISO	MOSI	-	-	[2]	
		Bit address	B7	B6	B5	B4	B3	B2	B1	B0		
P3[1]	Port 3	B0H	-	-	-	-	-	-	XTAL1	XTAL2	[2]	
P4	Port 4	B3H	-	TMS	-	-	RXD1	TXD1	TRIG	T3EX	[2]	
P5	Port 5	B4H	T3	-	-	-	-	-	-	-	[2]	
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF[2]	1111 1111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00[2]	0000 0000
P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3[2]	11x1 xx11
P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00[2]	00x0 xx00
P2M1	Port 2 output mode 1	A4H	(P2M1.7)	(P2M1.6)	(P2M1.5)	(P2M1.4)	(P2M1.3)	(P2M1.2)	(P2M1.1)	(P2M1.0)	FF[2]	1111 1111
P2M2	Port 2 output mode 2	A5H	(P2M2.7)	(P2M2.6)	(P2M2.5)	(P2M2.4)	(P2M2.3)	(P2M2.2)	(P2M2.1)	(P2M2.0)	00[2]	0000 0000
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03[2]	xxxx xx11
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00[2]	xxxx xx00
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD	-	VCPD	ADPD	I2PD	SPPD	SPD	-	00[2]	0000 0000
		Bit address	D7	D6	D5	D4	D3	D2	D1	D0		
PSW[1]	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00 000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX	[4]	

7.10 Memory organization

The various P89LPC952/954 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.

- IDATA

  Indirect Data. 256 bytes of internal data memory space (00H:FFH) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- XDATA

  'External' Data or Auxiliary RAM. Duplicates the classic 80C51 64 kB memory space addressed via the MOVX instruction using the SPTR, R0, or R1. All or part of this space could be implemented on-chip. The P89LPC952/954 has 256 bytes of on-chip XDATA memory, plus extended SFRs located in XDATA.

- CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC952/954 has 8 kB/16 kB of on-chip Code memory.

7.11 Data RAM arrangement

The 768 bytes of on-chip RAM are organized as shown in Table 6.

Table 6. On-chip data memory usages

Type	Data RAM	Size (bytes)
DATA	Memory that can be addressed directly and indirectly	128
IDATA	Memory that can be addressed indirectly	256
XDATA	Auxiliary ('External Data') on-chip memory that is accessed using the MOVX instructions	256

7.12 Interrupts

The P89LPC952/954 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources. The P89LPC952/954 supports 17 interrupt sources: external interrupts 0 and 1, timers 0 and 1, serial port 0 TX, serial port 0 RX, combined serial port 0 RX/TX, serial port 1 TX, serial port 1 RX, combined serial port 1 RX/TX, brownout detect, watchdog/RTC, I^2C-bus, keyboard, comparators 1 and 2, SPI, and ADC completion.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0, IEN1 or IEN2. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

7.17.6 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

7.18 RTC/system timer

The P89LPC952/954 has a simple RTC that allows a user to continue running an accurate timer while the rest of the device is powered down. The RTC can be a wake-up or an interrupt source. The RTC is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all ‘0’s, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator, provided that the XTAL oscillator is not being used as the CPU clock. If the XTAL oscillator is used as the CPU clock, then the RTC will use CCLK as its clock source. Only power-on reset will reset the RTC and its associated SFRs to the default state.

7.19 UARTs

The P89LPC952/954 has two enhanced UARTs that are compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC952/954 does include an independent Baud Rate Generator for each UART (BRG0 for UART 0 and BRG1 for UART 1). The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator associated with the specific UART. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UARTs can be operated in 4 modes: shift register, 8-bit UART, 9-bit UART, and CPU clock/32 or CPU clock/16.

7.19.1 Mode 0

Serial data enters and exits through RXDn. TXDn outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $^{1}/_{16}$ of the CPU clock frequency.

7.19.2 Mode 1

10 bits are transmitted (through TXDn) or received (through RXDn): a start bit (logic 0), 8 data bits (LSB first), and a stop bit (logic 1). When data is received, the stop bit is stored in RB8_n in Special Function Register SnCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in Section 7.19.5 “Baud rate generator and selection”).

7.19.3 Mode 2

11 bits are transmitted (through TXDn) or received (through RXDn): start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). When data is transmitted, the 9th data bit (TB8_n in SnCON) can be assigned the value of ‘0’ or ‘1’. Or, for example, the parity bit (P, in the PSW) could be moved into TB8_n. When data is received, the 9th data bit goes into RB8_n in Special Function Register SnCON, while the

7.23 KBI

The Keypad Interrupt function is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can configure the port via SFRs for different tasks.

The Keypad Interrupt Mask Register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern Register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control Register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control Register (KBCON) is used to define equal or not-equal for the comparison.

In order to use the Keypad Interrupt as an original KBI function like in 87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt may be used to wake-up the CPU from Idle or Power-down modes. This feature is particularly useful in handheld, battery-powered systems that need to carefully manage power consumption yet also need to be convenient to use.

In order to set the flag and cause an interrupt, the pattern on Port 0 must be held longer than six CCLKs.

7.24 Watchdog timer

The watchdog timer causes a system reset when it underflows as a result of a failure to feed the timer prior to the timer reaching its terminal count. It consists of a programmable 12-bit prescaler, and an 8-bit down counter. The down counter is decremented by a tap taken from the prescaler. The clock source for the prescaler is either the PCLK or the nominal 400 kHz watchdog oscillator. The watchdog timer can only be reset by a power-on reset. When the watchdog feature is disabled, it can be used as an interval timer and may generate an interrupt. Figure 16 shows the watchdog timer in Watchdog mode. Feeding the watchdog requires a two-byte sequence. If PCLK is selected as the watchdog clock and the CPU is powered down, the watchdog is disabled. The watchdog timer has a time-out period that ranges from a few µs to a few seconds. Please refer to the P89LPC952/954 *User's Manual* for more details.

7.26.5 Flash programming and erasing

Four different methods of erasing or programming of the flash are available. The flash may be programmed or erased in the end-user application (IAP) under control of the application's firmware. Another option is to use the ICP mechanism. This ICP system provides for programming through a serial clock/serial data interface. As shipped from the factory, the upper 512 bytes of user code space contains a serial ISP routine allowing for the device to be programmed in circuit through the serial port. The flash may also be programmed or erased using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead, this device provides a 32-bit CRC result on either a sector or the entire user code space.

7.26.6 ICP

ICP is performed without removing the microcontroller from the system. The ICP facility consists of internal hardware resources to facilitate remote programming of the P89LPC952/954 through a two-wire serial interface. The Philips ICP facility has made in-circuit programming in an embedded application—using commercially available programmers—possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the P89LPC952/954 *User's Manual*.

7.26.7 IAP

IAP is performed in the application under the control of the microcontroller's firmware. The IAP facility consists of internal hardware resources to facilitate programming and erasing. The Philips IAP has made in-application programming in an embedded application possible without additional components. Two methods are available to accomplish IAP. A set of predefined IAP functions are provided in a Boot ROM and can be called through a common interface, PGM_MTP. Several IAP calls are available for use by an application program to permit selective erasing and programming of flash sectors, pages, security bits, configuration bytes, and device ID. These functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FF03H. The Boot ROM occupies the program memory space at the top of the address space from FF00H to FEFFH, thereby not conflicting with the user program memory space.

In addition, IAP operations can be accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the P89LPC952/954 *User's Manual*.

7.26.8 ISP

ISP is performed without removing the microcontroller from the system. The ISP facility consists of a series of internal hardware resources coupled with internal firmware to facilitate remote programming of the P89LPC952/954 through the serial port. This firmware is provided by Philips and embedded within each P89LPC952/954 device. The Philips ISP facility has made in-system programming in an embedded application possible with a minimum of additional expense in components and circuit board area. The ISP function uses five pins (V_{DD}, V_{SS}, TXD, RXD, and $\overline{RST}$). Only a small connector needs to be available to interface your application to an external circuit in order to use this feature.

8.4 ADC operating modes

8.4.1 Fixed channel, single conversion mode

A single input channel can be selected for conversion. A single conversion will be performed and the result placed in the result register pair which corresponds to the selected input channel. An interrupt, if enabled, will be generated after the conversion completes.

8.4.2 Fixed channel, continuous conversion mode

A single input channel can be selected for continuous conversion. The results of the conversions will be sequentially placed in the eight result register pairs. The user may select whether an interrupt can be generated after every four or every eight conversions. Additional conversion results will again cycle through the result register pairs, overwriting the previous results. Continuous conversions continue until terminated by the user.

8.4.3 Auto scan, single conversion mode

Any combination of the eight input channels can be selected for conversion. A single conversion of each selected input will be performed and the result placed in the result register pair which corresponds to the selected input channel. The user may select whether an interrupt, if enabled, will be generated after either the first four conversions have occurred or all selected channels have been converted. If the user selects to generate an interrupt after the four input channels have been converted, a second interrupt will be generated after the remaining input channels have been converted. If only a single channel is selected this is equivalent to single channel, single conversion mode.

8.4.4 Auto scan, continuous conversion mode

Any combination of the eight input channels can be selected for conversion. A conversion of each selected input will be performed and the result placed in the result register pair which corresponds to the selected input channel. The user may select whether an interrupt, if enabled, will be generated after either the first four conversions have occurred or all selected channels have been converted. If the user selects to generate an interrupt after the four input channels have been converted, a second interrupt will be generated after the remaining input channels have been converted. After all selected channels have been converted, the process will repeat starting with the first selected channel. Additional conversion results will again cycle through the eight result register pairs, overwriting the previous results. Continuous conversions continue until terminated by the user.

8.4.5 Dual channel, continuous conversion mode

This is a variation of the auto scan continuous conversion mode where conversion occurs on two user-selectable inputs. The result of the conversion of the first channel is placed in the result register pair, AD0DAT0R and AD0DAT0L. The result of the conversion of the second channel is placed in result register pair, AD0DAT1R and AD0DAT1L. The first channel is again converted and its result stored in AD0DAT2R and AD0DAT2L. The second channel is again converted and its result placed in AD0DAT3R and AD0DAT3L, etc. An interrupt is generated, if enabled, after every set of four or eight conversions (user selectable).

Table 13. Dynamic characteristics (18 MHz)

V_{DD} = 3.0 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	nominal f = 7.3728 MHz trimmed to ± 1 % at T_{amb} = 25 °C; clock doubler option = OFF (default)	7.189	7.557	7.189	7.557	MHz
		nominal f = 14.7456 MHz; clock doubler option = ON	14.378	15.114	14.378	15.114	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency		320	520	320	520	kHz
f_{osc}	oscillator frequency		0	18	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 19	55	-	-	-	ns
f_{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection time	P1.5/$\overline{RST}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{RST}$	-	15	-	15	ns
t_{sa}	signal acceptance time	P1.5/$\overline{RST}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{RST}$	50	-	50	-	ns
External clock							
t_{CHCX}	clock HIGH time	see Figure 19	22	$T_{cy(clk)} - t_{CLCX}$	22	-	ns
t_{CLCX}	clock LOW time	see Figure 19	22	$T_{cy(clk)} - t_{CHCX}$	22	-	ns
t_{CLCH}	clock rise time	see Figure 19	-	5	-	5	ns
t_{CHCL}	clock fall time	see Figure 19	-	5	-	5	ns
Shift register (UART mode 0)							
T_{XLXL}	serial port clock cycle time	see Figure 18	$16T_{cy(clk)}$	-	888	-	ns
t_{QVXH}	output data set-up to clock rising edge time	see Figure 18	$13T_{cy(clk)}$	-	722	-	ns
t_{XHQX}	output data hold after clock rising edge time	see Figure 18	-	$T_{cy(clk)}$ + 20	-	75	ns
t_{XHDX}	input data hold after clock rising edge time	see Figure 18	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge time	see Figure 18	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	slave		0	$^{CCLK}/_{6}$	0	3.0	MHz
	master		-	$^{CCLK}/_{4}$	-	4.5	MHz
T_{SPICYC}	SPI cycle time	see Figure 20, 21, 22, 23					
	slave		$^{6}/_{CCLK}$	-	333	-	ns
	master		$^{4}/_{CCLK}$	-	222	-	ns

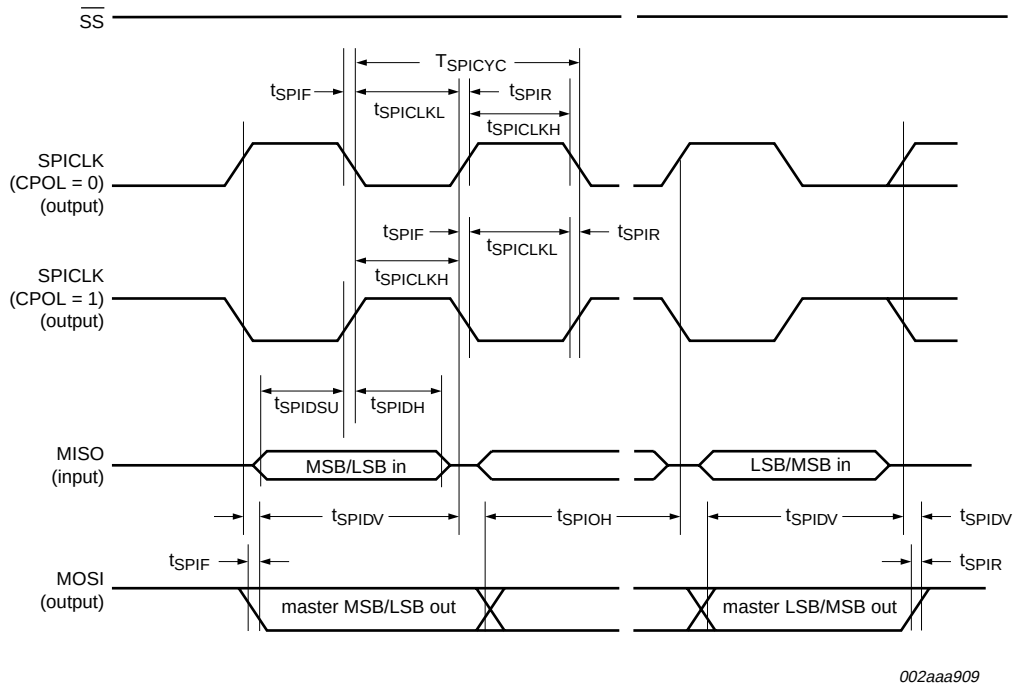


Fig 21. SPI master timing (CPHA = 1)

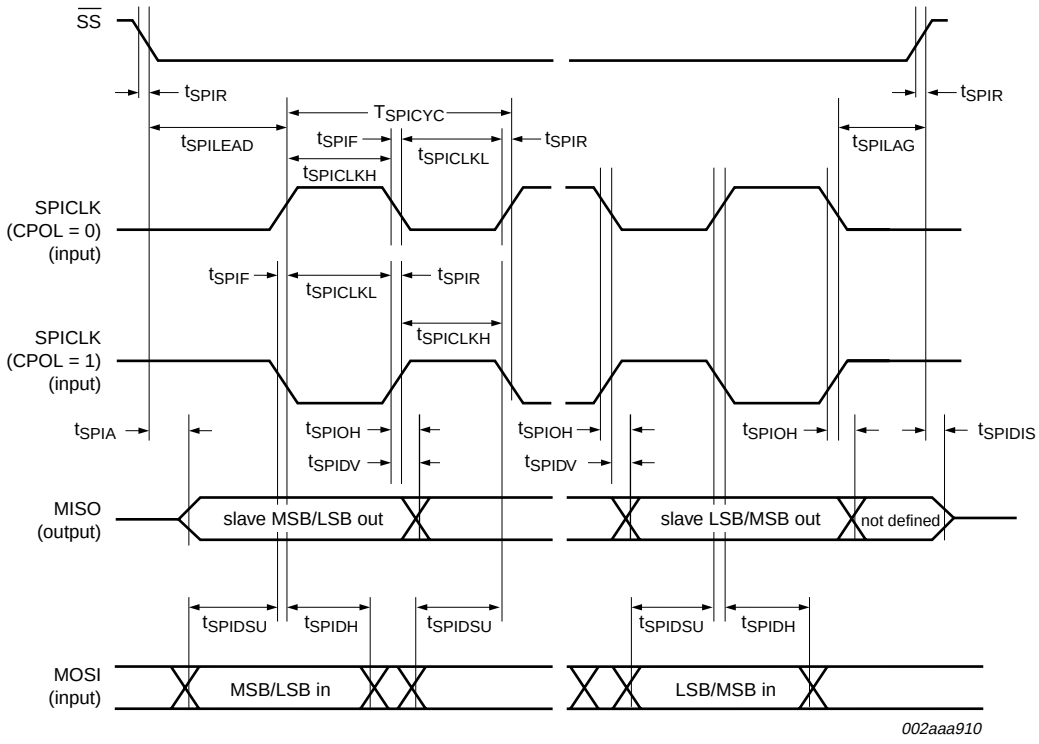


Fig 22. SPI slave timing (CPHA = 0)

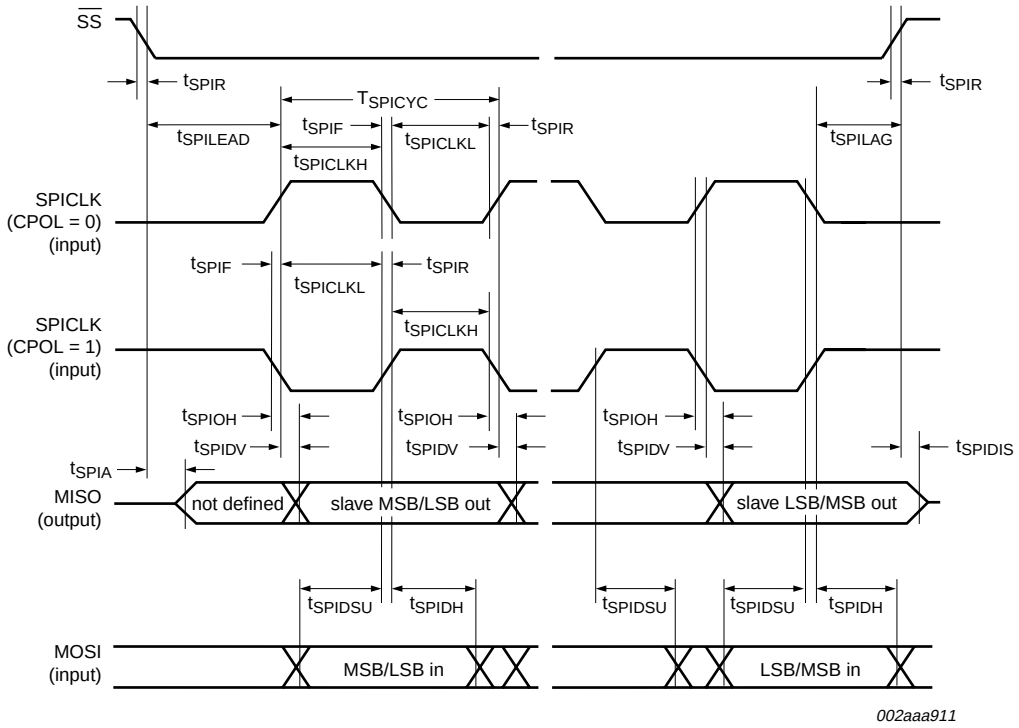


Fig 23. SPI slave timing (CPHA = 1)

11.2 ISP entry mode

Table 14. Dynamic characteristics, ISP entry mode

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VR}	V_{DD} active to $\overline{RST}$ active delay time	pin $\overline{RST}$	50	-	-	µs
t_{RH}	$\overline{RST}$ HIGH time	pin $\overline{RST}$	1	-	32	µs
t_{RL}	$\overline{RST}$ LOW time	pin $\overline{RST}$	1	-	-	µs

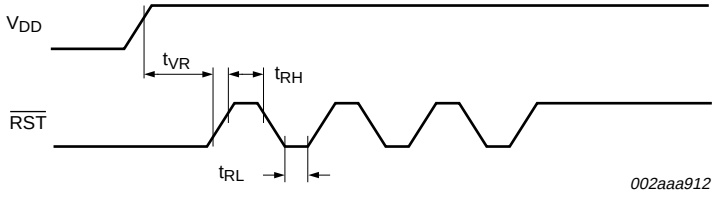


Fig 24. ISP entry waveform

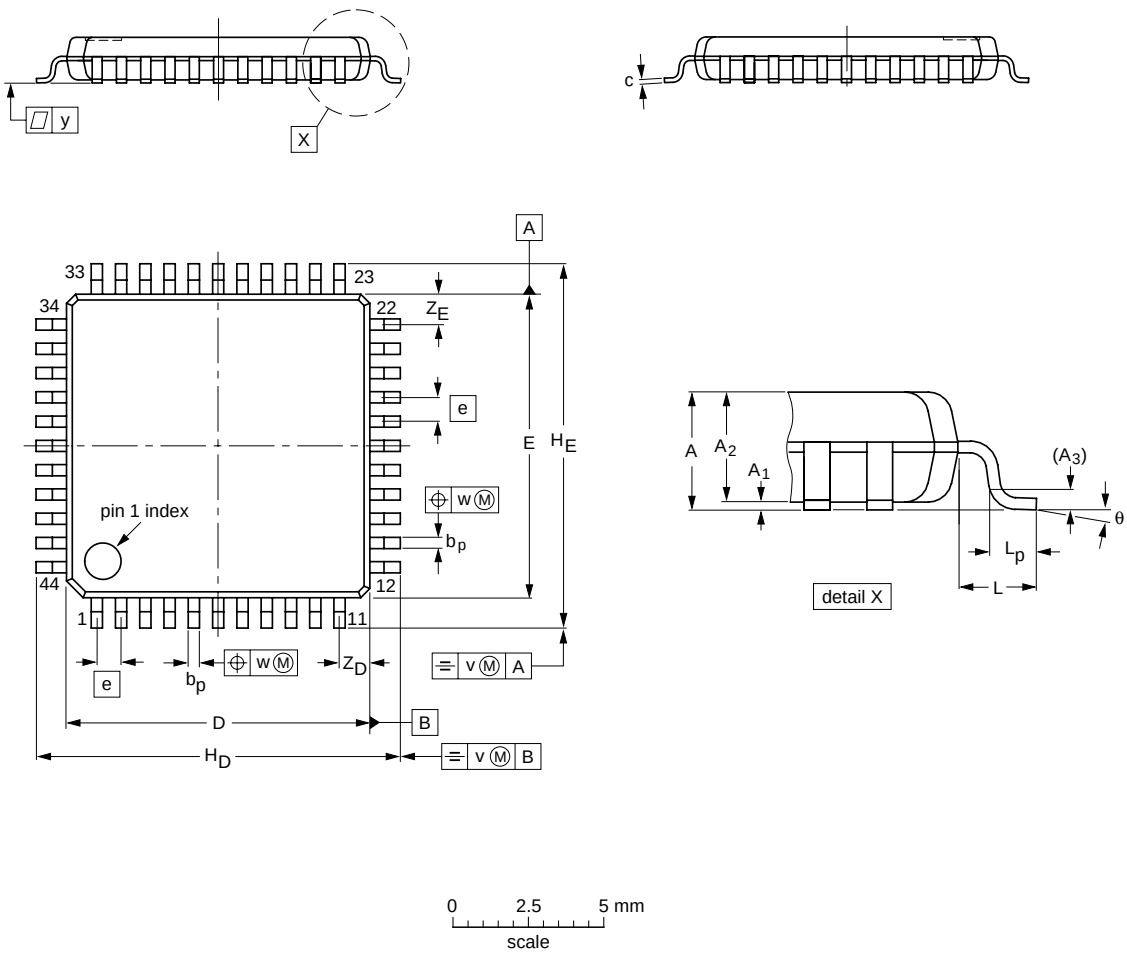
12.2 ADC electrical characteristics

Table 16. ADC electrical characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.
All limits valid for an external source impedance of less than 10 kΩ.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DDA(ADC)}$	ADC analog supply voltage		V_{DD} − 0.4	-	V_{DD} + 0.4	V
V_{SSA}	analog ground voltage		V_{SS} − 0.4	-	V_{SS} + 0.4	V
V_{VREFP}	voltage on pin VREFP		V_{DD} − 0.4	-	V_{DD} + 0.4	V
V_{VREFN}	voltage on pin VREFN		V_{SS} − 0.4	-	V_{SS} + 0.4	V
V_{IA}	analog input voltage		V_{SS} − 0.4	-	V_{DD} + 0.4	V
C_{ia}	analog input capacitance		-	-	15	pF
E_D	differential linearity error		-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		-	-	±2	LSB
E_O	offset error		-	-	±2	LSB
E_G	gain error		-	-	±2	LSB
$E_{u(tot)}$	total unadjusted error		-	-	+4/–3	LSB
M_{CTC}	channel-to-channel matching		-	-	±1	LSB
$\alpha_{ct(port)}$	crosstalk between port inputs	0 kHz to 100 kHz	-	-	–60	dB
SR_{in}	input slew rate		-	-	100	V/ms
$T_{cy(ADC)}$	ADC clock cycle time		111	-	3125	ns
t_{ADC}	ADC conversion time	ADC enabled	-	-	$36T_{cy(ADC)}$	µs

LQFP44: plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm **SOT389-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.45 0.30	0.20 0.12	10.1 9.9	10.1 9.9	0.8	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.2	0.1	1.14 0.85	1.14 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT389-1	136E08	MS-026				~~00-01-19~~ 02-06-07

Fig 26. Package outline SOT389-1 (LQFP44)