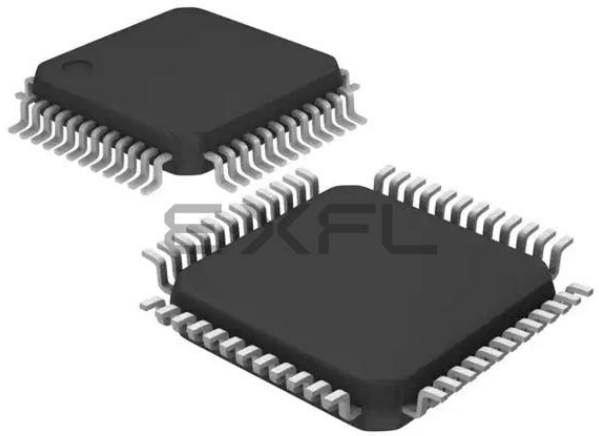

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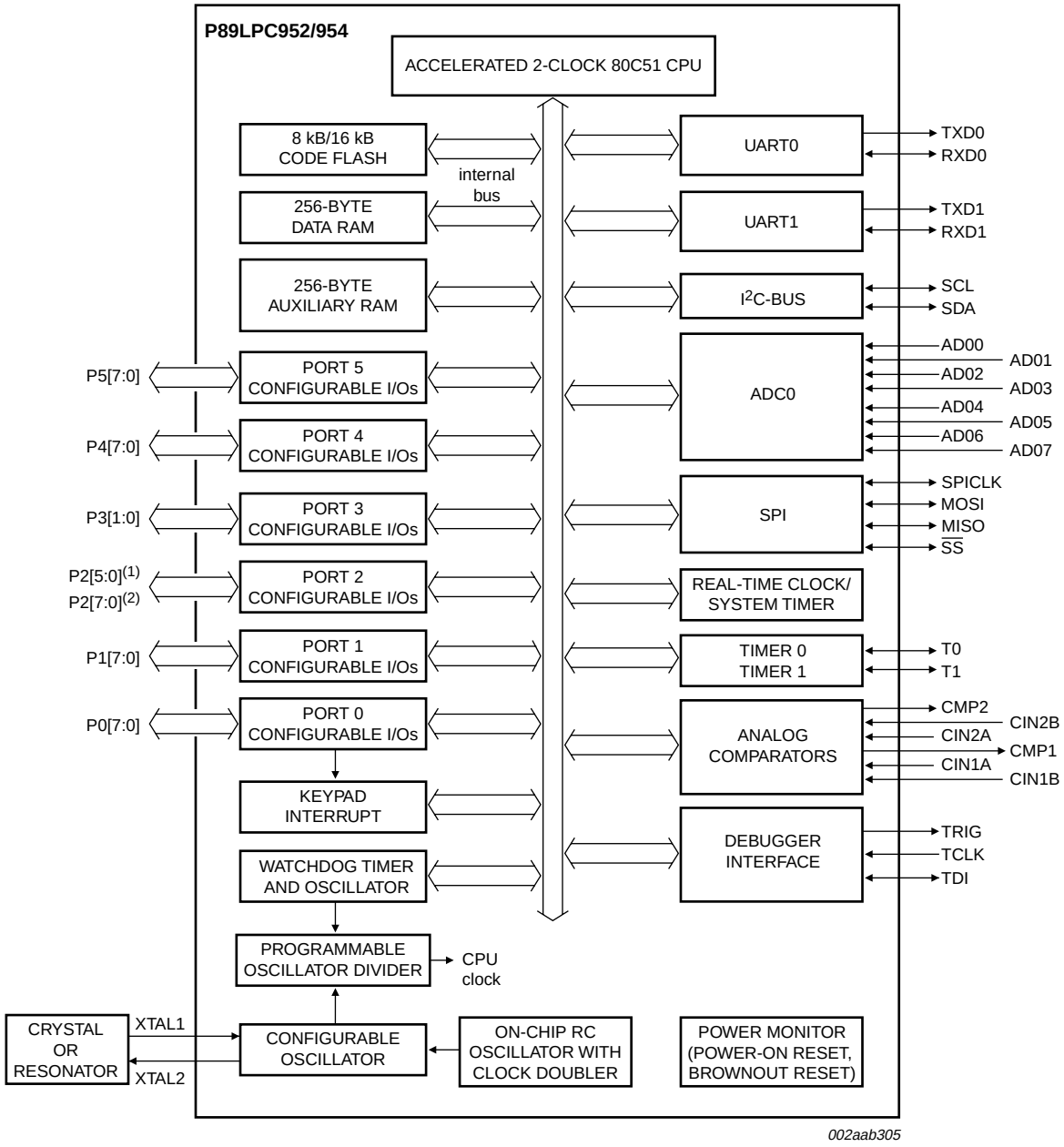
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc954fbd48-151

2.2 Additional features

- A high performance 80C51 CPU provides instruction cycle times of 111 ns to 222 ns for all instructions except multiply and divide when executing at 18 MHz. This is six times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.
- Serial flash In-Circuit Programming (ICP) allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Serial flash In-System Programming (ISP) allows coding while the device is mounted in the end application.
- In-Application Programming (IAP) of the flash code memory. This allows changing the code in a running application.
- Low voltage (brownout) detect allows a graceful system shutdown when power fails. May optionally be configured as an interrupt.
- Idle and two different power-down reduced power modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical power-down current is 1 μA (total power-down with voltage comparators disabled).
- On-chip power-on reset allows operation without external reset components. A software reset function is also available.
- Programmable external reset pin (P1.5) configuration options: open drain bidirectional reset input/output, reset input with pull-up, push-pull reset output, input-only port. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets.
- Only power and ground connections are required to operate the P89LPC952/954 when internal reset option is selected.
- Configurable on-chip oscillator with frequency range options selected by user programmed flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz.
- Oscillator fail detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.
- Port ‘input pattern match’ detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Four interrupt priority levels.
- Eight keypad interrupt inputs, plus two additional external interrupt inputs.
- Schmitt trigger port inputs.
- Second data pointer.
- Extended temperature range.
- Emulation support.

4. Block diagram



(1) 44-pin package.

(2) 48-pin package.

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

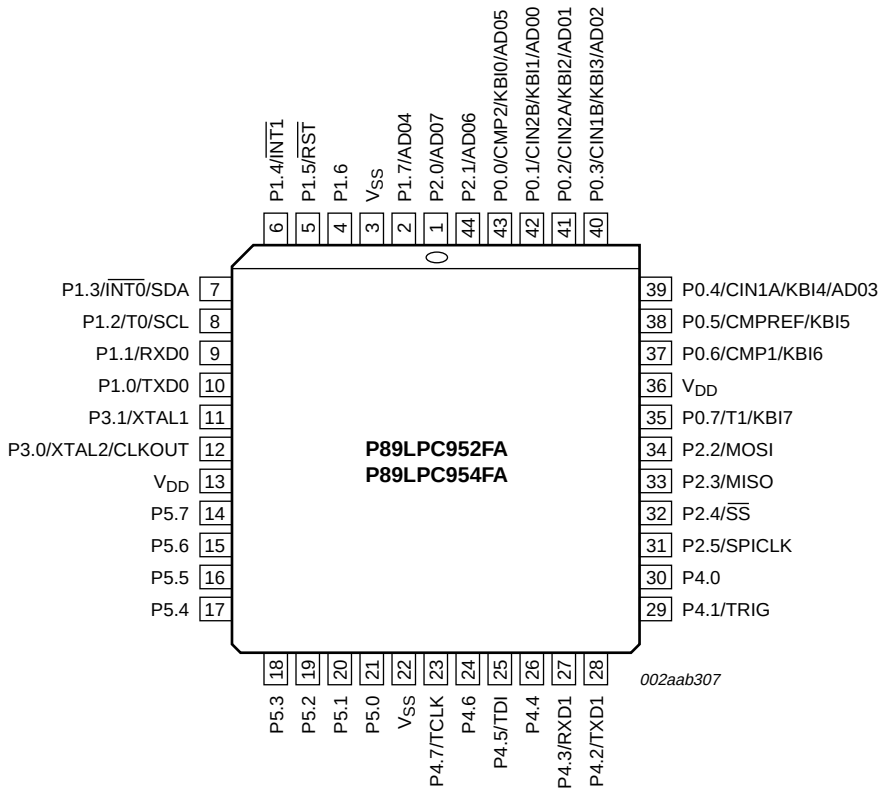


Fig 3. PLCC44 pin configuration

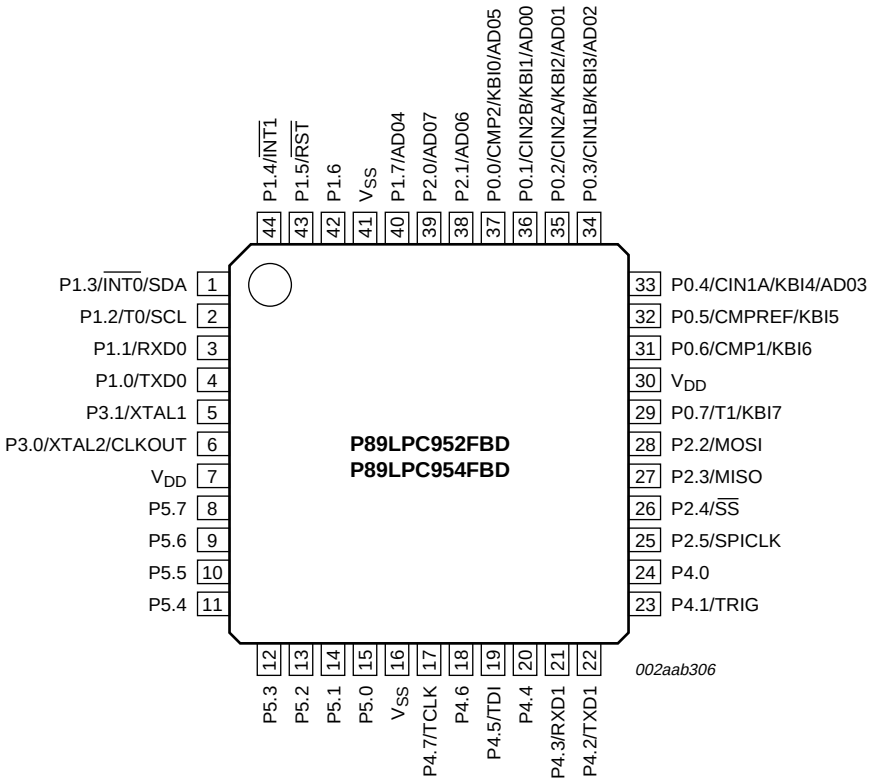


Fig 4. LQFP44 pin configuration

Table 3. Pin description *...continued*

Symbol	Pin			Type	Description
	LQFP48	PLCC44	LQFP44		
P0.6/CMP1/KBI6	34	37	31	I/O	**P0.6 —** Port 0 bit 6.
				O	**CMP1 —** Comparator 1 output.
				I	**KBI6 —** Keyboard input 6.
P0.7/T1/KBI7	31	35	29	I/O	**P0.7 —** Port 0 bit 7.
				I/O	**T1 —** Timer/counter 1 external count input or overflow output.
				I	**KBI7 —** Keyboard input 7.
P1.0 to P1.7				I/O, I [1]	**Port 1:** Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 7.13.1 "Port configurations" and Table 11 "Static characteristics" for details. P1.2 to P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.0/TXD0	4	10	4	I/O	**P1.0 —** Port 1 bit 0.
				O	**TXD0 —** Transmitter output for serial port 0.
P1.1/RXD0	3	9	3	I/O	**P1.1 —** Port 1 bit 1.
				I	**RXD0 —** Receiver input for serial port 0.
P1.2/T0/SCL	2	8	2	I/O	**P1.2 —** Port 1 bit 2 (open-drain when used as output).
				I/O	**T0 —** Timer/counter 0 external count input or overflow output (open-drain when used as output).
				I/O	**SCL —** I^2C-bus serial clock input/output.
P1.3/$\overline{INT0}$/SDA	1	7	1	I/O	**P1.3 —** Port 1 bit 3 (open-drain when used as output).
				I	**$\overline{INT0}$ —** External interrupt 0 input.
				I/O	**SDA —** I^2C-bus serial data input/output.
P1.4/$\overline{INT1}$	48	6	44	I/O	**P1.4 —** Port 1 bit 4.
				I	**$\overline{INT1}$ —** External interrupt 1 input.

Table 3. Pin description *...continued*

Symbol	Pin			Type	Description
	LQFP48	PLCC44	LQFP44		
P2.5/SPICLK	27	31	25	I/O	**P2.5 —** Port 2 bit 5.
				I/O	**SPICLK —** SPI clock. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.6	26	-	-	I/O	**P2.6 —** Port 2 bit 6.
P2.7	5	-	-	I/O	**P2.7 —** Port 2 bit 7.
P3.0 to P3.1				I/O	**Port 3:** Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 “Port configurations” and Table 11 “Static characteristics” for details. All pins have Schmitt triggered inputs. Port 3 also provides various special functions as described below:
P3.0/XTAL2/ CLKOUT	7	12	6	I/O	**P3.0 —** Port 3 bit 0.
				O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration.
				O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK -TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the RTC/system timer.
P3.1/XTAL1	6	11	5	I/O	**P3.1 —** Port 3 bit 1.
				I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the RTC/system timer.
P4.0 to P4.7				I/O	**Port 4:** Port 4 is an 8-bit I/O port with a user-configurable output type. During reset Port 4 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 4 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 “Port configurations” and Table 11 “Static characteristics” for details. All pins have Schmitt triggered inputs. Port 4 also provides various special functions as described below:
P4.0	25	30	24	I/O	**P4.0 —** Port 4 bit 0.
P4.1/TRIG	24	29	23	I/O	**P4.1 —** Port 4 bit 1.
				O	**TRIG —** Debugger trigger output.
P4.2/TXD1	23	28	22	I/O	**P4.2 —** Port 4 bit 2.
				O	**TXD1 —** Transmitter output for serial port 1.
P4.3/RXD1	22	27	21	I/O	**P4.3 —** Port 4 bit 3.
				I	**RXD1 —** Receiver input for serial port 1.

Table 4. Special function registers *…continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
DPH	Data pointer high	83H									00	0000 0000
DPL	Data pointer low	82H									00	0000 0000
FMADRH	Program flash address high	E7H									00	0000 0000
FMADRL	Program flash address low	E6H									00	0000 0000
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash control (Write)	E4H	FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program flash data	E5H									00	0000 0000
I2ADR	I^2C-bus slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	0000 0000
	Bit address		**DF**	**DE**	**DD**	**DC**	**DB**	**DA**	**D9**	**D8**		
I2CON[1]	I^2C-bus control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x000 00x0
I2DAT	I^2C-bus data register	DAH										
I2SCLH	Serial clock generator/SCL duty cycle register high	DDH									00	0000 0000
I2SCLL	Serial clock generator/SCL duty cycle register low	DCH									00	0000 0000
I2STAT	I^2C-bus status register	D9H	STA.4	STA.3	STA.2	STA.1	STA.0	0	0	0	F8	1111 1000

Table 4. Special function registers *…continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**		
IEN0[1]	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	EX1	ET0	EX0	00	0000 0000
		Bit address	**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**	**E8**		
IEN1[1]	Interrupt enable 1	E8H	-	EST	-	-	ESPI	EC	EKBI	EI2C	00[2]	00x0 0000
IEN2	Interrupt enable 2	D5H	-	-	-	-	EST1	ES1/ESR1	EADC	-	00[2]	00x0 0000
		Bit address	**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**	**B8**		
IP0[1]	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	PX1	PT0	PX0	00[2]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/ PSRH	PT1H	PX1H	PT0H	PX0H	00[2]	x000 0000
		Bit address	**FF**	**FE**	**FD**	**FC**	**FB**	**FA**	**F9**	**F8**		
IP1[1]	Interrupt priority 1	F8H	-	PST	-	-	PSPI	PC	PKBI	PI2C	00[2]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	-	PSTH	-	-	PSPIH	PCH	PKBIH	PI2CH	00[2]	00x0 0000
IP2	Interrupt priority 2	D6H	-	-	-	-	PEST1	PES1/ PESR1	PADC	-	00[2]	00x0 0000
IP2H	Interrupt priority 2 high	D7H	-	-	-	-	PEST1H	PES1H/ PESR1H	PADCH	-	00[2]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN _SEL	KBIF	00[2]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H									00	0000 0000
KBPATN	Keypad pattern register	93H									FF	1111 1111
		Bit address	**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**		
P0[1]	Port 0	80H	T1/KB7	CMP1 /KB6	CMPREF /KB5	CIN1A /KB4	CIN1B /KB3	CIN2A /KB2	CIN2B /KB1	CMP2 /KB0	[2]	
		Bit address	**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P1[1]	Port 1	90H	-	-	$\overline{\text{RST}}$	$\overline{\text{INT1}}$	$\overline{\text{INT0}}$/SDA	T0/SCL	RXD0	TXD0	[2]	

Table 4. Special function registers *…continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		8F	8E	8D	8C	8B	8A	89	88		
TCON[1]	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	0000 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	0000 0000
TRIM	Internal oscillator trim register	96H	RCCLK	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[6] [7]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[5] [7]	
WDL	Watchdog load	C1H									FF	1111 1111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] Indicates SFRs that are bit addressable.

[2] All ports are in input only (high-impedance) state after power-up.

[3] BRGR1_0 and BRGR0_0 must only be written if BRGEN_0 in BRGCON_0 SFR is logic 0. If any are written while BRGEN_0 = 1, the result is unpredictable.

[4] The RSTSRC register reflects the cause of the P89LPC952/954 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx11 0000.

[5] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

[6] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[7] The only reset source that affects these SFRs is power-on reset.

Table 5. Extended special function registers *…continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
AD0DAT7L	ADC0 data register 7, left (MSB)	FFF1H	AD0DAT7[9:2]									
BNDSTA0	ADC0 boundary status register	FFEDH										
BRGCON_1	Baud rate generator 1 control	FFB3H	-	-	-	-	-	-	SBRGS_1	BRGEN_1	00[2]	xxxx xx00
BRG0_1	Baud rate generator 1 rate low	FFB4H										
BRG1_1	Baud rate generator 1 rate high	FFB5H										
FREEZE	Peripheral clock freeze	FFD0H	-	-	-	RTC_F	CCU_F	WDT_F	T1_F	T0_F	00	xxx0 0000
P4M1	Port 4 output mode 1	FFB8H	(P4M1.7)	(P4M1.6)	(P4M1.5)	(P4M1.4)	(P4M1.3)	(P4M1.2)	(P4M1.1)	(P4M1.0)	FF[1]	1111 1111
P4M2	Port 4 output mode 2	FFB9H	(P4M2.7)	(P4M2.6)	(P4M2.5)	(P4M2.4)	(P4M2.3)	(P4M2.2)	(P4M2.1)	(P4M2.0)	00[1]	0000 0000
P5M1	Port 5 output mode 1	FFBAH	(P5M1.7)	(P5M1.6)	(P5M1.5)	(P5M1.4)	(P5M1.3)	(P5M1.2)	(P5M1.1)	(P5M1.0)	FF[1]	1111 1111
P5M2	Port 5 output mode 3	FFBBH	(P5M2.7)	(P5M2.6)	(P5M2.5)	(P5M2.4)	(P5M2.3)	(P5M2.2)	(P5M2.1)	(P5M2.0)	00[1]	0000 0000
S1ADDR	Serial port 1 address register	FFB2H									00	0000 0000
S1ADEN	Serial port 1 address enable	FFB1H									00	0000 0000
S1BUF	Serial port 1 data buffer register	FFB0H									xx	xxxx xxxx

[1] Extended SFRs are physically located on-chip but logically located in external data memory address space (XDATA). The MOVX A,@DPTR and MOVX @DPTR,A instructions are used to access these extended SFRs.

[2] BRGR1_1 and BRGR0_1 must only be written if BRGEN_1 in BRGCON_1 SFR is logic 0. If any are written while BRGEN_1 = 1, the result is unpredictable.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1, IP1H, IP2, and IP2H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

7.12.1 External interrupt inputs

The P89LPC952/954 has two external interrupt inputs as well as the Keypad Interrupt function. The two interrupt inputs are identical to those present on the standard 80C51 microcontrollers.

These external interrupts can be programmed to be level-triggered or edge-triggered by setting or clearing bit IT1 or IT0 in Register TCON.

In edge-triggered mode, if successive samples of the $\overline{\text{INTn}}$ pin show a HIGH in one cycle and a LOW in the next cycle, the interrupt request flag IEn in TCON is set, causing an interrupt request.

If an external interrupt is enabled when the P89LPC952/954 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 7.15 “Power reduction modes” for details.

7.13 I/O ports

The P89LPC952/954 has six I/O ports: Port 0, Port 1, Port 2, Port 3, Port 4, and Port 5. Ports 0, 1, 2, 4, and 5 are 8-bit ports, and Port 3 is a 2-bit port. The exact number of I/O pins available depends upon the clock and reset options and package chosen, as shown in Table 7.

Table 7. Number of I/O pins available

Clock source	Reset option	Number of I/O pins (48-pin package)	Number of I/O pins (44-pin package)
On-chip oscillator or watchdog oscillator	No external reset (except during power-up)	42	40
	External $\overline{RST}$ pin supported	41	39
External clock input	No external reset (except during power-up)	41	39
	External $\overline{RST}$ pin supported[1]	40	38
Low/medium/high speed oscillator (external crystal or resonator)	No external reset (except during power-up)	40	38
	External $\overline{RST}$ pin supported[1]	39	37

[1] Required for operation above 12 MHz.

7.13.1 Port configurations

All but three I/O port pins on the P89LPC952/954 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

1. P1.5/$\overline{RST}$ can only be an input and cannot be configured.
2. P1.2/T0/SCL and P1.3/$\overline{INT0}$/SDA may only be configured to be either input-only or open-drain.

7.13.1.1 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC952/954 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt triggered input that also has a glitch suppression circuit.

7.13.1.2 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

7.16 Reset

The P1.5/$\overline{\text{RST}}$ pin can function as either a digital input (P1.5), an active-LOW reset input with an internal pull-up, a bidirectional reset input/output (open drain output with an internal pull-up), or as push-pull reset output. These modes are selected by the RPE (Reset Pin Enable) bit in UCFG1 and the RPE1 (Reset Pin Enable 1) bit in UCFG2.

Table 8. Reset pin modes

P1.5/$\overline{\text{RST}}$ mode	RPE1 (UCFG2.0)	RPE (UCFG1.6)
General purpose input	0	0
Reset input with pull-up	0	1
Bidirectional reset input/output (open drain with pull-up)	1	0
Reset output	1	1

Remark: During a power-up sequence, the RPE and RPE1 selection is overridden and this pin always functions as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this pin will function as defined by the RPE and RPE1 bits. Only a power-up reset will temporarily override the selection defined by RPE and RPE1 bits. Other sources of reset will not override the RPE and RPE1 bits.

Remark: During a power cycle, V_{DD} must fall below V_{POR} before power is reapplied, in order to ensure a power-on reset (see Table 11 “Static characteristics” on page 51).

Remark: When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user configured via UCFG1, UCGF2);
- Power-on detect;
- Brownout detect;
- Watchdog timer;
- Software reset;
- UART break character detect reset.

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a ‘0’ to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

stop bit is not saved. The baud rate is programmable to either $^1/_{16}$ or $^1/_{32}$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON. The SMOD1 bit controls the Timer 1 output rate available to both UARTs.

7.19.4 Mode 3

11 bits are transmitted (through TXDn) or received (through RXDn): a start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in Section 7.19.5 “Baud rate generator and selection”).

7.19.5 Baud rate generator and selection

Each enhanced UART has an independent Baud Rate Generator. The baud rate is determined by a baud-rate preprogrammed into the BRGR1_n and BRGR0_n SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1 but is much more accurate. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UARTs can use either Timer 1 or their respective baud rate generator output (see Figure 8). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is cleared. The independent Baud Rate Generators use OSCCLK.

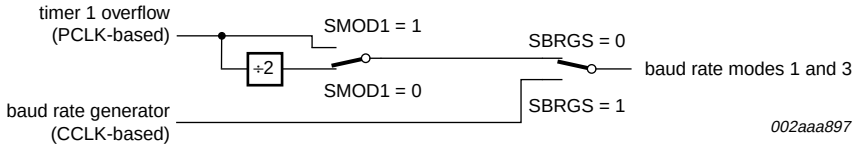


Fig 8. Baud rate sources for UART (Modes 1, 3)

7.19.6 Framing error

Framing error is reported in the status register (SnSTAT). In addition, if SMOD0 (PCON.6) is ‘1’, framing errors can be made available in SnCON.7 respectively. If SMOD0 is ‘0’, SnCON.7 is SM0_n. It is recommended that SM0_n and SM1_n (SnCON.7:6) are set up when SMOD0 is ‘0’.

7.19.7 Break detect

Break detect is reported in the status register (SnSTAT). A break is detected when 11 consecutive bits are sensed LOW. The break detect can be used to reset the device and force the device into ISP mode.

7.19.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SnBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

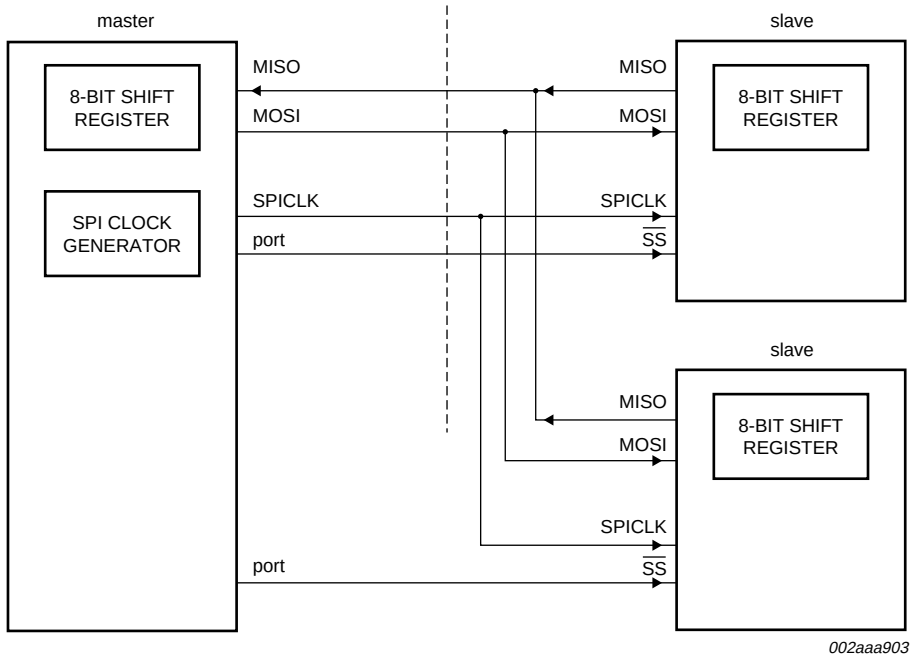


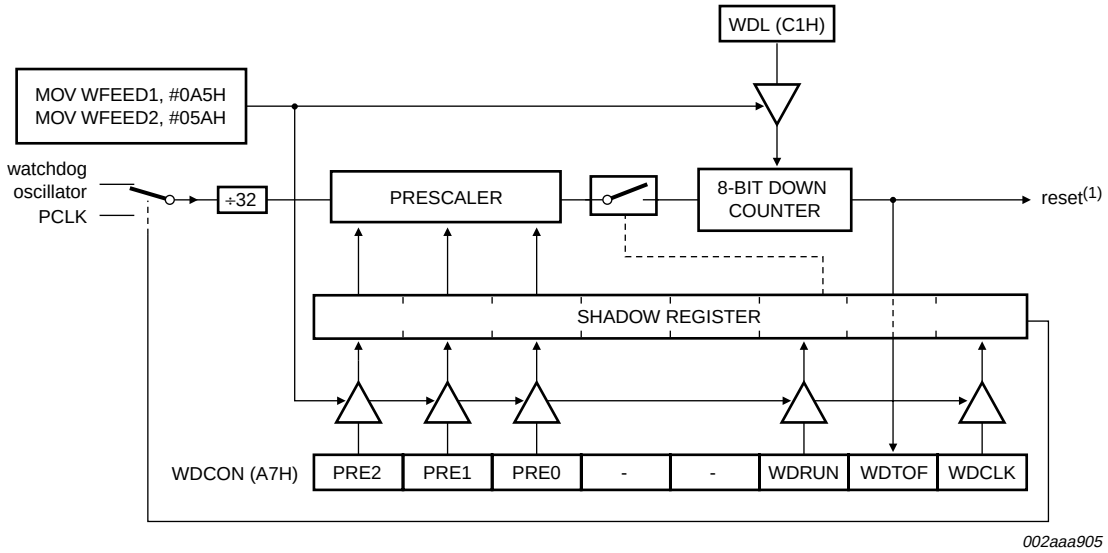
Fig 14. SPI single master multiple slaves configuration

7.22 Analog comparators

Two analog comparators are provided on the P89LPC952/954. Input and output options allow use of the comparators in a number of different configurations. Comparator operation is such that the output is a logical one (which may be read in a register and/or routed to a pin) when the positive input (one of two selectable pins) is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be configured to cause an interrupt when the output value changes.

The overall connections to both comparators are shown in Figure 15. The comparators function to V_{DD} = 2.4 V.

When each comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 µs. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.



(1) Watchdog reset can also be caused by an invalid feed sequence, or by writing to WDCON not immediately followed by a feed sequence.

Fig 16. Watchdog timer in Watchdog mode (WDTE = 1)

7.25 Additional features

7.25.1 Software reset

The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

7.25.2 Dual data pointers

The dual Data Pointers (DPTR) provides two different Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic 0 so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

7.25.3 Debugger interface

This device contains a two-wire serial debugger interface designed to be used with commercially available debugging tools. An additional trigger output is provided that maybe triggered using the two-wire debugger interface.

The Freeze register allows the user to selectively disable clocking of peripheral device timers while in the debugger mode.

The two-wire serial debugger interface can also be used be used to program the code memory of these devices.

7.26 Flash program memory

7.26.1 General description

The P89LPC952/954 flash memory provides in-circuit electrical erasure and programming. The flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any flash sector (1 kB) or page (64 bytes). The Chip Erase operation will erase the entire program memory. ICP using standard commercial programmers is available. In addition, IAP and byte-erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC952/954 flash reliably stores memory contents even after 400,000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. The P89LPC952/954 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms.

7.26.2 Features

- Programming and erase over the full operating voltage range.
- Byte erase allows code memory to be used for data storage.
- Read/Programming/Erase using ISP, IAP, ICP, or two-wire serial debugger.
- Internal fixed boot ROM, containing low-level IAP routines available to user code.
- Default loader providing ISP via the serial port, located in upper end of user program memory.
- Boot vector allows user-provided flash loader code to reside anywhere in the flash memory space, providing flexibility to the user.
- Any flash program/erase operation in 2 ms.
- Programming with industry-standard commercial programmers.
- Programmable security for the code in the flash for each sector.
- 400,000 typical erase/program cycles for each byte.
- 20 year minimum data retention.

7.26.3 Flash organization

The program memory consists of eight/sixteen 1 kB sectors on the P89LPC952/954 devices. Each sector can be further divided into 64-byte pages. In addition to sector erase, page erase, and byte erase, a 64-byte page register is included which allows from 1 to 64 bytes of a given page to be programmed at the same time, substantially reducing overall programming time.

7.26.4 Using flash as data storage

The flash code memory array of this device supports individual byte erasing and programming. Any byte in the code memory array may be read using the MOVC instruction, provided that the sector containing the byte has not been secured (a MOVC instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

8.4.6 Single step mode

This special mode allows ‘single-stepping’ in an auto scan conversion mode. Any combination of the eight input channels can be selected for conversion. After each channel is converted, an interrupt is generated, if enabled, and the ADC waits for the next start condition. May be used with any of the start modes.

8.5 Conversion start modes

8.5.1 Timer triggered start

An A/D conversion is started by the overflow of Timer 0. Once a conversion has started, additional Timer 0 triggers are ignored until the conversion has completed. The Timer triggered start mode is available in all ADC operating modes.

8.5.2 Start immediately

Programming this mode immediately starts a conversion. This start mode is available in all ADC operating modes.

8.5.3 Edge triggered

An A/D conversion is started by rising or falling edge of P1.4. Once a conversion has started, additional edge triggers are ignored until the conversion has completed. The edge triggered start mode is available in all ADC operating modes.

8.6 Boundary limits interrupt

The ADC has both a high and low boundary limit register. The user may select whether an interrupt is generated when the conversion result is within (or equal to) the high and low boundary limits or when the conversion result is outside the boundary limits. An interrupt will be generated, if enabled, if the result meets the selected interrupt criteria. The boundary limit may be disabled by clearing the boundary limit interrupt enable.

An early detection mechanism exists when the interrupt criteria has been selected to be outside the boundary limits. In this case, after the four MSBs have been converted, these four bits are compared with the four MSBs of the boundary high and low registers. If the four MSBs of the conversion meet the interrupt criteria (i.e., outside the boundary limits) an interrupt will be generated, if enabled. If the four MSBs do not meet the interrupt criteria, the boundary limits will again be compared after all 8 MSBs have been converted. A boundary status register (BNDSTA0) flags the channels which caused a boundary interrupt.

8.7 Clock divider

The ADC requires that its internal clock source be in the range of 320 kHz to 9 MHz to maintain accuracy. A programmable clock divider that divides the clock from 1 to 8 is provided for this purpose.

8.8 Power-down and Idle mode

In Idle mode the ADC, if enabled, will continue to function and can cause the device to exit Idle mode when the conversion is completed if the A/D interrupt is enabled. In Power-down mode or Total Power-down mode, the ADC does not function. If the ADC is enabled, it will consume power. Power can be reduced by disabling the ADC.

11. Dynamic characteristics

Table 12. Dynamic characteristics (12 MHz)

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	nominal f = 7.3728 MHz trimmed to ± 1 % at T_{amb} = 25 °C; clock doubler option = OFF (default)	7.189	7.557	7.189	7.557	MHz
		nominal f = 14.7456 MHz; clock doubler option = ON, V_{DD} = 2.7 V to 3.6 V	14.378	15.114	14.378	15.114	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency		320	520	320	520	kHz
f_{osc}	oscillator frequency		0	12	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 19	83	-	-	-	ns
f_{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection time	P1.5/$\overline{\text{RST}}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{\text{RST}}$	-	15	-	15	ns
t_{sa}	signal acceptance time	P1.5/$\overline{\text{RST}}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{\text{RST}}$	50	-	50	-	ns
External clock							
t_{CHCX}	clock HIGH time	see Figure 19	33	$T_{cy(clk)} - t_{CLCX}$	33	-	ns
t_{CLCX}	clock LOW time	see Figure 19	33	$T_{cy(clk)} - t_{CHCX}$	33	-	ns
t_{CLCH}	clock rise time	see Figure 19	-	8	-	8	ns
t_{CHCL}	clock fall time	see Figure 19	-	8	-	8	ns
Shift register (UART mode 0)							
T_{XLXL}	serial port clock cycle time	see Figure 18	$16T_{cy(clk)}$	-	1333	-	ns
t_{QVXH}	output data set-up to clock rising edge time	see Figure 18	$13T_{cy(clk)}$	-	1083	-	ns
t_{XHQX}	output data hold after clock rising edge time	see Figure 18	-	$T_{cy(clk)}$ + 20	-	103	ns
t_{XHDX}	input data hold after clock rising edge time	see Figure 18	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge time	see Figure 18	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	slave		0	CCLK/6	0	2.0	MHz
	master		-	CCLK/4	-	3.0	MHz

18. Contents

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