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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, WDT
Number of I/O	20
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 5x16b, 4x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFLGA Exposed Pad
Supplier Device Package	44-MAPLGA (5x5)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mkm14z64chh5

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

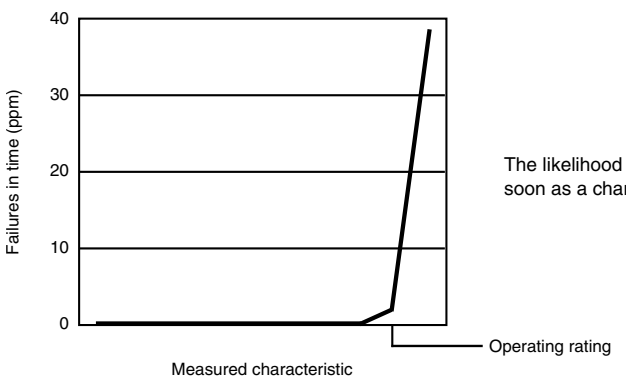
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

This is an example of an operating rating:

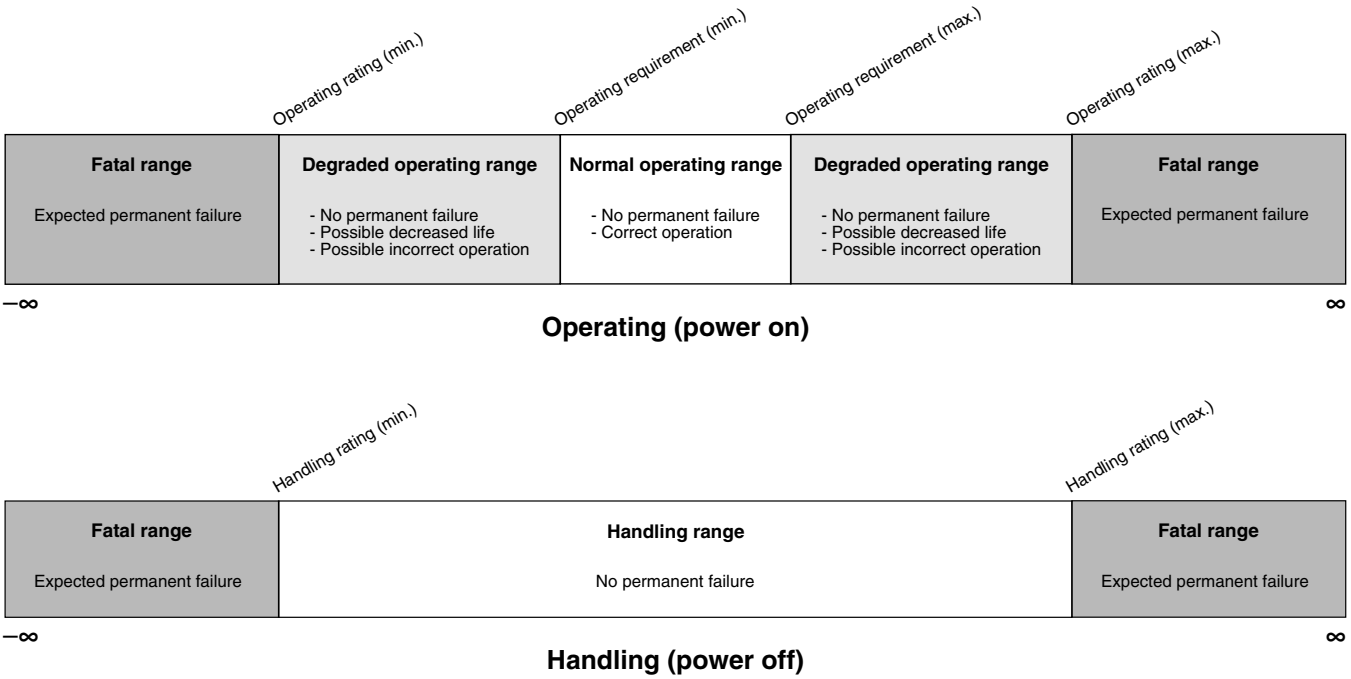
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

3.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

3.6 Relationship between ratings and operating requirements



3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

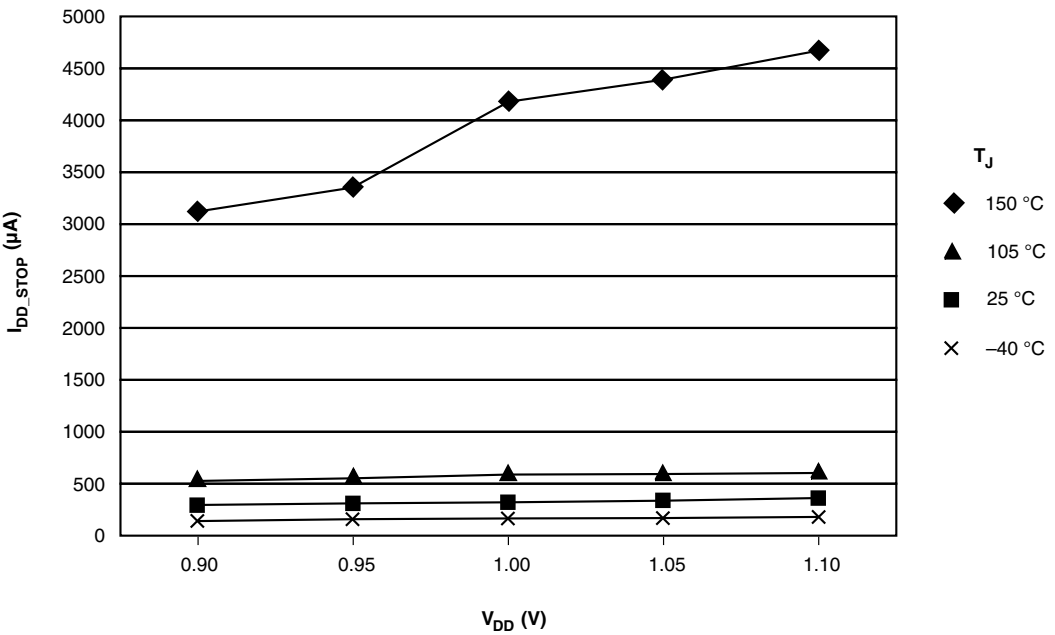
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

6.1 Core modules

6.1.1 Single Wire Debug (SWD)

Table 12. SWD switching characteristics at 2.7 V (2.7-3.6 V)

Symbol	Description	Value	Unit	Notes
SWD CLK	Frequency of SWD operation	20	MHz	1
Inputs, tSUI	Data setup time	5	ns	1
inputs,tHI	Data hold time	0	ns	1
after clock edge, tDVO	Data valid Time	32	ns	1
tHO	Data Valid Hold	0	ns	1

1. Input transition assumed =1 ns. Output transition assumed = 50 pf.

Table 13. Switching characteristics at 1.7 V (1.7-3.6 V)

Symbol	Description	Value	Unit	Notes
SWD CLK	Frequency of SWD operation	18	MHz	
Inputs, tSUI	Data setup time	4.7	ns	
inputs,tHI	Data hold time	0	ns	
after clock edge, tDVO	Data valid Time	49.4	ns	2
tHO	Data Valid Hold	0	ns	

1. Frequency of SWD clock (18 Mhz) is applicable only in case the input setup time of the device outside is not more than 6.15 ns, else the frequency of SWD clock would need to be lowered.

6.1.2 Analog Front End (AFE)

AFE switching characteristics at (2.7 V-3.6 V)

Case1: Clock is coming In and Data is also coming In (XBAR ports timed with respect to the XBAR ports timed with respect to AFE clock defined at pad ptb[7] and pte[3])

Table 14. AFE switching characteristics (2.7 V-3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	10	MHz	1
Inputs, tSUI	Data setup time	5	ns	1
inputs,tHI	Data hold time	0	ns	1

1. Input Transition: 1ns. Output Load: 50 pf.

Table 18. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{vco}	VCO operating frequency	11.71875	12.288	14.6484375	MHz	
I_{pll}	PLL operating current • IO 3.3 V current • Max core voltage current	—	300 100	—	µA	9
f_{pll_ref}	PLL reference frequency range	31.25	32.768	39.0625	kHz	
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 12 MHz			700	ps	10
D_{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	11
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	12

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. Chip max freq is 50 MHz, so Mid-range with DRS = 10 and High-range of DCO cannot be used and should not be configured.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. Chip max freq is 50 MHz, so Mid-range with DRS = 10 and High-range of DCO cannot be used and should not be configured.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
9. Excludes any oscillator currents that are also consuming power while PLL is in operation.
10. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
11. Will be updated later
12. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.2.2 Oscillator electrical specifications

6.2.2.1 Oscillator DC electrical specifications

Table 19. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	

Table continues on the next page...

Table 19. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 1 MHz	—	200	—	µA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz (RANGE=01)	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high-gain mode (HGO=1)					1
	• 32 kHz	—	25	—	µA	
	• 1 MHz	—	300	—	µA	
	• 4 MHz	—	400	—	µA	
	• 8 MHz (RANGE=01)	—	500	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
	Capacitance of EXTAL • Die level (100 LQFP) • Package level (100 LQFP)	247 0.495	—	—	ff pF	
	Capacitance of XTAL • Die level (100 LQFP) • Package level (100 LQFP)	265 0.495	—	—	ff pF	
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	

Table continues on the next page...

Table 20. Oscillator frequency specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	48	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—		—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—		—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

6.2.3 32 kHz oscillator electrical characteristics

6.2.3.1 32 kHz oscillator DC electrical specifications

Table 21. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

6.2.3.2 32 kHz oscillator frequency specifications

Table 22. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	

Table continues on the next page...

Table 22. 32 kHz oscillator frequency specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{start}	Crystal start-up time	—	1000	—	ms	1
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2 , 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

6.3 Memories and memory interfaces

6.3.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

6.3.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 23. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

6.3.1.2 Flash timing specifications — commands

Table 24. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1

Table continues on the next page...

Table 29. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

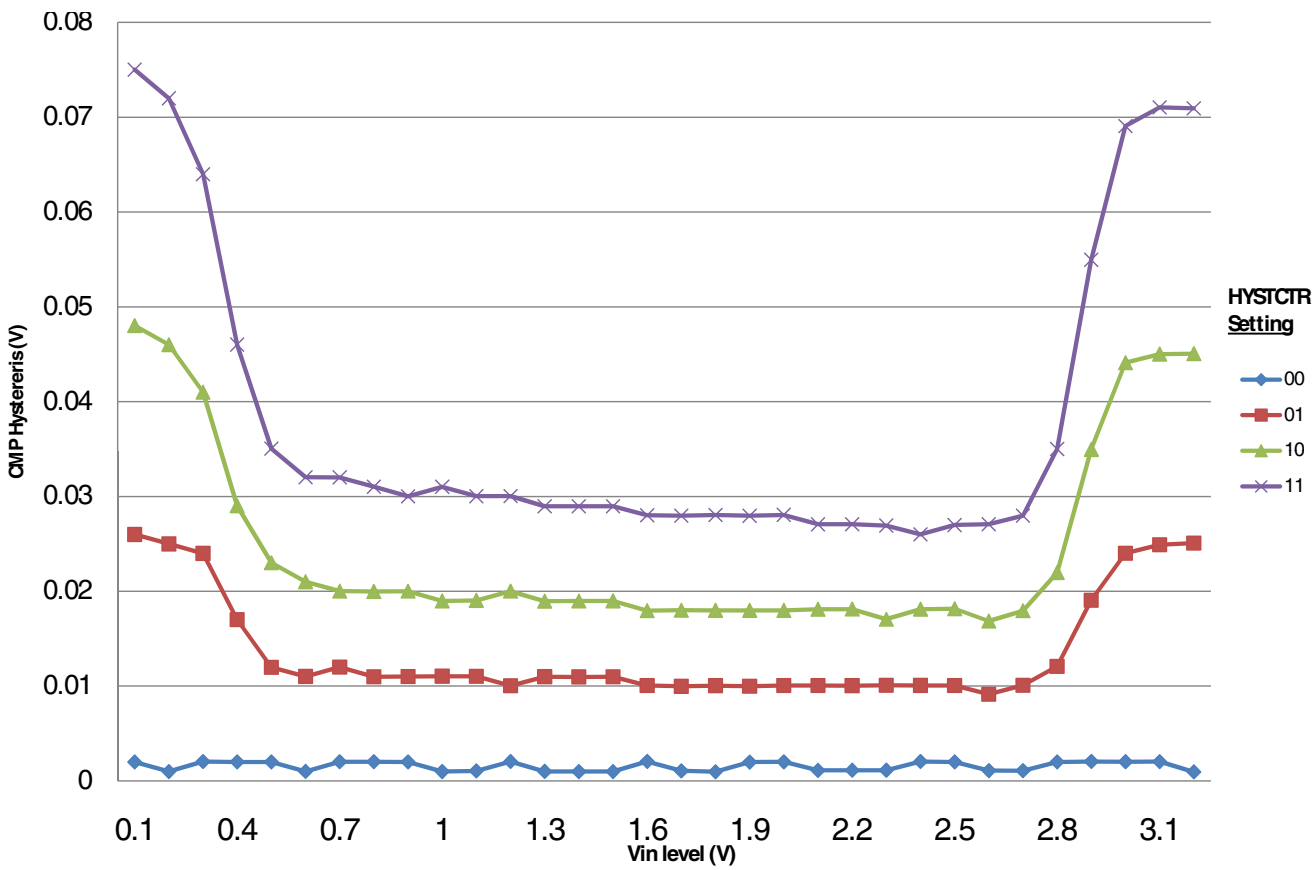


Figure 4. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

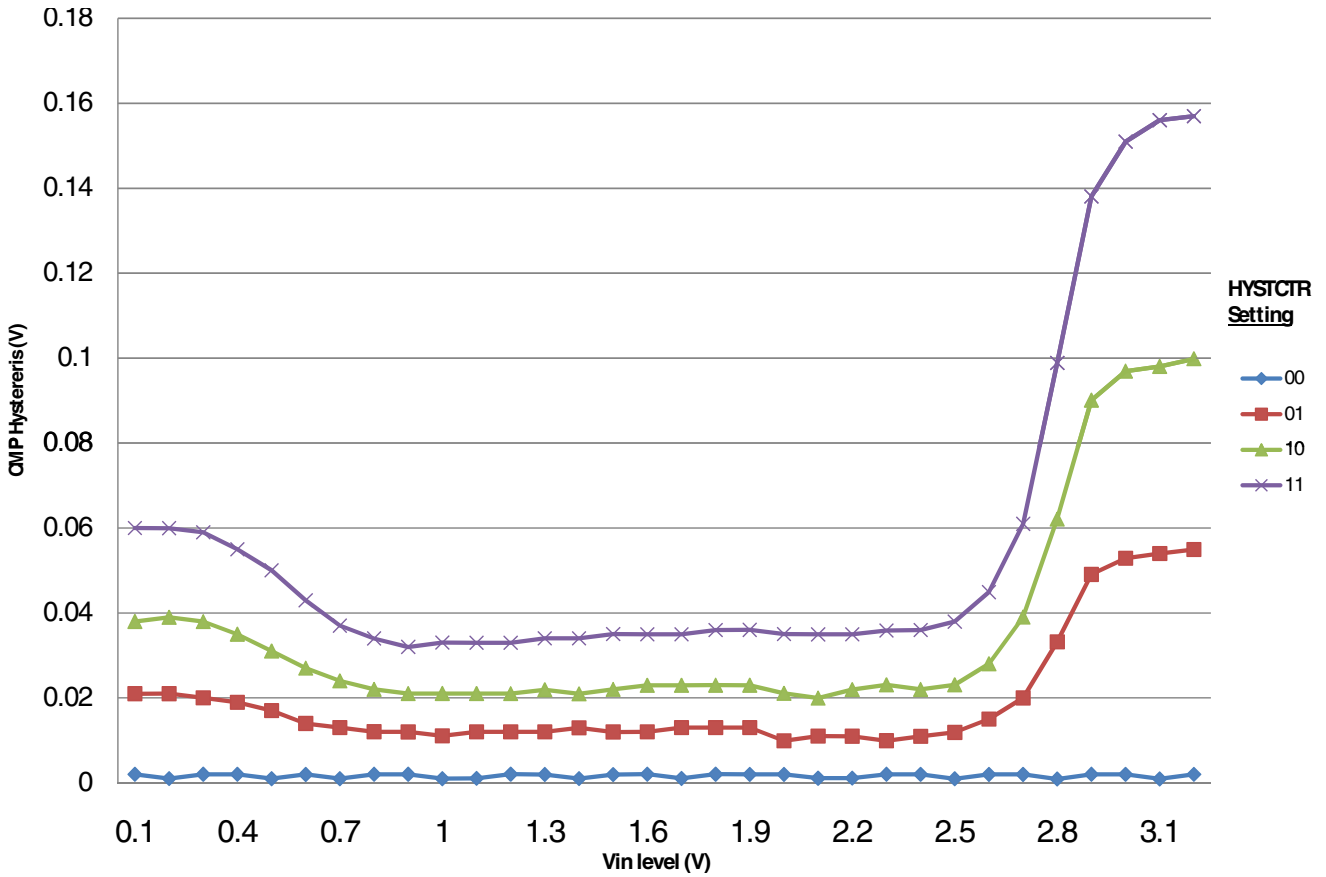


Figure 5. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

6.4.3 Voltage reference electrical specifications

Table 30. 1.2 VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71[1]	3.6	V	
T_A	Temperature	–40	85	°C	
C_L	Output load capacitance	100		nF	2, 3

1. AFE is enabled.
2. C_L must be connected between VREFH and VREFL.
3. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 31. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VREFH	Voltage reference output with factory trim at nominal V_{DDA} and temperature = 25 °C	1.1915	1.2	1.2027	V	
VREFH	Voltage reference output with — factory trim	1.1584	—	1.2376	V	

Table continues on the next page...

Table 31. VREF full-range operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VREFH	Voltage reference output — user trim	1.178	—	1.202	V	
VREFL	Voltage reference output	0.38	0.4	0.42	V	
V_{step}	Voltage reference trim step	—	0.5	—	mV	
V_{tdrift}	Temperature drift (Vmax - Vmin across the full temperature range)	—	5	—	mV	1
Ac	Aging coefficient	—	—	400	uV/yr	
I_{bg}	Bandgap only current	—	—	80	µA	2
I_{lp}	Low-power buffer current	—	—	0.19	µA	2
I_{hp}	High-power buffer current	—	—	0.5	mA	2
I_{LOAD}	VREF buffer current	—	—	1	mA	3
ΔV_{LOAD}	Load regulation • current = + 1.0 mA • current = - 1.0 mA	—	 2 5	—	mV	2, 4
T_{stup}	Buffer startup time	—	—	20	ms	
V_{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range)	—	0.5	—	mV	2

1. For temp range -40 °C to 105 °C, this value is 15 mV
2. See the chip's Reference Manual for the appropriate settings of VREF Status and Control register.
3. See the chip's Reference Manual for the appropriate settings of SIM Miscellaneous Control Register.
4. Load regulation voltage is the difference between VREFH voltage with no load vs. voltage with defined load.

Table 32. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	°C	

Table 33. VREF limited-range operating behaviours

Symbol	Description	Min.	Max.	Unit	Notes
VREFH	Voltage reference output with factory trim	1.173	1.225	V	
VREFL	Voltage reference output	0.38	0.42	V	

6.4.4 AFE electrical specifications

Table 34. ΣΔ ADC + PGA specifications (continued)

Symbol	Description	Conditions	Min	Typ[1]	Max	Unit	Notes
SINAD	Signal-to-Noise + Distortion Ratio	Normal Mode • f_{IN}=50Hz; gain=01, common mode=0V, V_{pp}=500mV (differential ended)		78		dB	
		Low-Power Mode • f_{IN}=50Hz; gain=01, common mode=0V, V_{pp}=500mV (differential ended)		74		dB	
CMMR	Common Mode Rejection Ratio	• f_{IN}=50Hz; gain=01, common mode=0V, Vid=100 mV • f_{IN}=50Hz; gain=32, common mode=0V, V_{id}=100 mV		70 70		dB	
E_{offset}	Offset Error	Gain=01, V_{pp}=1000 mV (full range diff.)			+/- 5	mV	
ΔOffset Temp	Offset Temperature Drift[3]	Gain=01, V_{pp}=1000mV (full range diff.)			+/- 25	ppm/°C	
$\Delta Gain_{Temp}$	Gain Temperate Drift - Gain error caused by temperature drifts[4]	• Gain=01, V_{pp}=500mV (differential ended) • Gain=32, V_{pp}=15mV (differential ended)			+/- 75	ppm/°C	
$PSRR_{AC}$	AC Power Supply Rejection Ratio	Gain=01, VCC = 3V ± 100mV, f_{IN} = 50 Hz		60		dB	
XT	Crosstalk (with the input of the affected channel grounded)	Gain=01, V_{id} = 500 mV, f_{IN} = 50 Hz			-100	dB	
f_{MCLK}	Modulator Clock Frequency Range	Normal Mode Low-Power Mode	0.03 0.03		6.5 1.6	MHz	
I_{DDA_PGA}	Current consumption by PGA (each channel)	Normal Mode (f_{MCLK} = 6.144 MHz, OSR= 2048) Low-Power Mode (f_{MCLK} = 0.768MHz, OSR= 256)			2.6 0	mA	5
I_{DDA_ADC}	Current Consumption by ADC (each chanel)	Normal Mode (f_{MCLK} = 6.144 MHz, OSR= 2048) Low-Power Mode (f_{MCLK} = 0.768MHz, OSR= 256)			1.4 0.5	mA	

1. Typical values assume VDDA = 3.0 V, Temp = 25°C, f_{MCLK} = 6.144 MHz, OSR = 2048 for Normal mode and f_{MCLK} = 768 kHz, OSR = 256 for Low-Power Mode unless otherwise stated. Typical values are for reference only and are not tested in production.
2. The full-scale input range in single-ended mode is 0.5Vpp
3. Represents combined offset temperature drift of the PGA, SD ADC and Internal 1.2 VREF blocks; Defined by shorting both differential inputs to ground.
4. Represents combined gain temperature drift of the PGA, SD ADC and Internal 1.2 VREF blocks.
5. PGA is disabled in low-power modes.

1. Typical values assume VDDA = 3.0 V, Temp = 25°C, f_{MCLK} = 6.144 MHz, OSR = 2048 for Normal mode and f_{MCLK} = 768 kHz, OSR = 256 for Low-Power Mode unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Represent combined gain temperature drift of the SD ADC, and Internal 1.2 VREF blocks.
3. Represent combined offset temperature drift of the SD ADC, and Internal 1.2 VREF blocks; Defined by shorting both differential inputs to ground.

6.4.4.3 External modulator interface

The external modulator interface on this device comprises of a Clock signal and 1-bit data signal. Depending on the modulator device being used the interface works as follows:

- Clock supplied to external modulator which drives data on rising edge and the KM device captures it on falling edge or next rising edge.
- Clock and data are supplied by external modulator and KM device can sample it on falling edge or next rising edge.

Depending on control bit in AFE, the sampling edge is changed.

6.5 Timers

See General switching specifications.

6.6 Communication interfaces

6.6.1 I2C switching specifications

See General switching specifications.

6.6.2 UART switching specifications

See General switching specifications.

6.6.3 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following table provides some reference values to be met on SoC.

Table 36. SPI switching characteristics at 2.7 V (2.7 - 3.6)

Description	Min.	Max.	Unit	Notes
Frequency of operation (F_{sys})	—	50	MHz	1
SCK frequency • Master • Slave	2	12.5 12.5	MHz Mhz	3
SCK Duty Cycle	50%	—	—	
Data Setup Time (inputs, tSUI) • Master • Slave	25 3		ns	
Input Data Hold Time (inputs, tHI) • Master • Slave	0 1		ns	
Data hold time (outputs, tHO) • Master • Slave	0 0		ns	
Data Valid Out Time (after SCK edge, tDVO) • Master • Slave	13 28		ns	
Rise time input • Master • Slave	1 1		ns	
Fall time input • Master • Slave	1 1		ns	
Rise time output • Master • Slave	8.9 8.9		ns	
Fall time output • Master • Slave	7.8 7.8		ns	

1. SPI modules will work on core clock.
2. F_{sys}/(Max Divider Value from registers)
3. F_{SYS}/2 in Master mode and F_{SYS}/4 in Slave mode. F_{SYS}/4 in Master as well as Slave Modes, where F_{SYS}=50Mhz

NOTE

The values assumed for input transition and output load are:
Input transition = 1 ns Output load = 50 pF

Table 37. SPI switching characteristics at 1.7 V (1.7 - 3.6)

Description	Min.	Max.	Unit	Notes
Frequency of operation (F_{sys})	—	50	MHz	

Table continues on the next page...

6.7.1 LCD electrical characteristics

Table 40. LCD electricals

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{Frame}	LCD frame frequency	28	30	58	Hz	
C_{LCD}	LCD charge pump capacitance — nominal value	—	100	—	nF	1
C_{BYLCD}	LCD bypass capacitance — nominal value	—	100	—	nF	1
C_{Glass}	LCD glass capacitance	—	2000	8000	pF	2
V_{IREG}	V_{IREG}					3
	• HREFSEL=0, RVTRIM=1111	—	1.11	—	V	
	• HREFSEL=0, RVTRIM=1000	—	1.01	—	V	
	• HREFSEL=0, RVTRIM=0000	—	0.91	—	V	
Δ_{RTRIM}	V_{IREG} TRIM resolution	—	—	3.0	% V_{IREG}	
I_{VIREG}	V_{IREG} current adder — RVEN = 1	—	1	—	µA	4
I_{RBIAS}	RBIAS current adder	—	15	—	µA	
	• LADJ = 10 or 11 — High load (LCD glass capacitance ≤ 8000 pF)	—	3	—	µA	
	• LADJ = 00 or 01 — Low load (LCD glass capacitance ≤ 2000 pF)					
VLL2	VLL2 voltage					
	• HREFSEL = 0	2.0 – 5%	2.0	—	V	
VLL3	VLL3 voltage	3.0 – 5%	3.0	—	V	

1. The actual value used could vary with tolerance.
2. For highest glass capacitance values, LCD_GCR[LADJ] should be configured as specified in the LCD Controller chapter within the device's reference manual.
3. V_{IREG} maximum should never be externally driven to any level other than V_{DD} - 0.15 V.
4. 2000 pF load LCD, 32 Hz frame frequency.

NOTE

KM family devices have a 1/3 bias controller that works with a 1/3 bias LCD glass. To avoid ghosting, the LCD OFF threshold should be greater than VLL1 level. If the LCD glass has an OFF threshold less than VLL1 level, use the internal VREG mode and generate VLL1 internally using RVTRIM option. This can reduce VLL1 level to allow for a lower OFF threshold LCD glass.

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
44-pin LGA	98ASA00239D
64-pin LQFP	98ASS23234W
100-pin LQFP	98ASS23308W

8 Pinout

NOTE

VSS also connects to flag on 44 LGA.

8.1 KM Signal multiplexing and pin assignments

100 QFP	64 QFP	44 LGA	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	1	—	Disabled	LCD23	PTA0						
2	2	—	Disabled	LCD24	PTA1						
3	3	—	Disabled	LCD25	PTA2						
4	—	—	Disabled	LCD26	PTA3						
5	4	1	NMI_B	LCD27	PTA4	LLWU_P15					NMI_B
6	5	2	Disabled	LCD28	PTA5	CMP0OUT					
7	6	3	Disabled	LCD29	PTA6	XBAR_IN0	LLWU_P14				
8	7	4	Disabled	LCD30	PTA7	XBAR_OUT0					
9	—	—	Disabled	LCD31	PTB0						
10	8	5	VDD	VDD							
11	9	6	VSS	VSS							
12	—	—	Disabled	LCD32	PTB1						
13	—	—	Disabled	LCD33	PTB2						
14	—	—	Disabled	LCD34	PTB3						
15	—	—	Disabled	LCD35	PTB4						
16	—	—	Disabled	LCD36	PTB5						
17	—	—	Disabled	LCD37/ CMP1P0	PTB6						

100 QFP	64 QFP	44 LGA	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
55	—	—	Disabled		PTE0	I2C0_SDA	XBAR_OUT4	UART3_TxD	CLKOUT		
56	35	25	RESET_B		PTE1						RESET_B
57	—	26	EXTAL1	EXTAL1	PTE2	EWM_IN	XBAR_IN6	I2C1_SDA			
58	—	27	XTAL1	XTAL1	PTE3	EWM_OUT	AFE_CLK	I2C1_SCL			
59	36	28	VSS	VSS							
60	—	29	SAR_VSSA	SAR_VSSA							
61	—	30	SAR_VDDA	SAR_VDDA							
62	37	31	VDD	VDD							
63	—	—	Disabled		PTE4	LPTMR0	UART2_CTS	EWM_IN			
64	—	—	Disabled		PTE5	TMR_3	UART2_RTS	EWM_OUT	LLWU_P6		
65	38	32	SWD_IO	CMP0P2	PTE6	XBAR_IN5	UART2_RxD	LLWU_P5			SWD_IO
66	39	33	SWD_CLK	AD6	PTE7	XBAR_OUT5	UART2_TxD				SWD_CLK
67	40	—	Disabled	AD7	PTF0	RTCCLKOUT	TMR_2	CMP0OUT			
68	41	34	Disabled	LCD0/ AD8	PTF1	TMR_0	XBAR_OUT6				
69	42	35	Disabled	LCD1/ AD9	PTF2	CMP1OUT	RTCCLKOUT				
70	43	—	Disabled	LCD2	PTF3	SPI1_SS_B	LPTMR1	UART0_RxD			
71	44	—	Disabled	LCD3	PTF4	SPI1_SCK	LPTMR0	UART0_TxD			
72	45	—	Disabled	LCD4	PTF5	SPI1_MISO	I2C1_SCL	LLWU_P4			
73	46	—	Disabled	LCD5	PTF6	SPI1_MOSI	I2C1_SDA	LLWU_P3			
74	47	—	Disabled	LCD6	PTF7	TMR_2	CLKOUT				
75	48	—	Disabled	LCD7	PTG0	TMR_1	LPTMR2				
76	49	36	Disabled	LCD8/ AD10	PTG1	LLWU_P2	LPTMR0				
77	50	37	Disabled	LCD9/ AD11	PTG2	SPI0_SS_B	LLWU_P1				
78	51	38	Disabled	LCD10	PTG3	SPI0_SCK	I2C0_SCL				
79	52	39	Disabled	LCD11	PTG4	SPI0_MOSI	I2C0_SDA				
80	53	40	Disabled	LCD12	PTG5	SPI0_MISO	LPTMR1				
81	54	—	Disabled	LCD13	PTG6	LLWU_P0	LPTMR2				
82	—	—	Disabled	LCD14	PTG7						
83	—	—	Disabled	LCD15	PTH0						
84	—	—	Disabled	LCD16	PTH1						
85	—	—	Disabled	LCD17	PTH2						
86	—	—	Disabled	LCD18	PTH3						
87	—	—	Disabled	LCD19	PTH4						
88	—	—	Disabled	LCD20	PTH5						
89	—	41	Disabled		PTH6	UART1_CTS	SPI1_SS_B	XBAR_IN7			
90	—	42	Disabled		PTH7	UART1_RTS	SPI1_SCK	XBAR_OUT7			
91	55	43	Disabled	CMP0P5	PTI0	UART1_RxD	XBAR_IN8	SPI1_MISO	SPI1_MOSI		
92	56	44	Disabled		PTI1	UART1_TxD	XBAR_OUT8	SPI1_MOSI	SPI1_MISO		

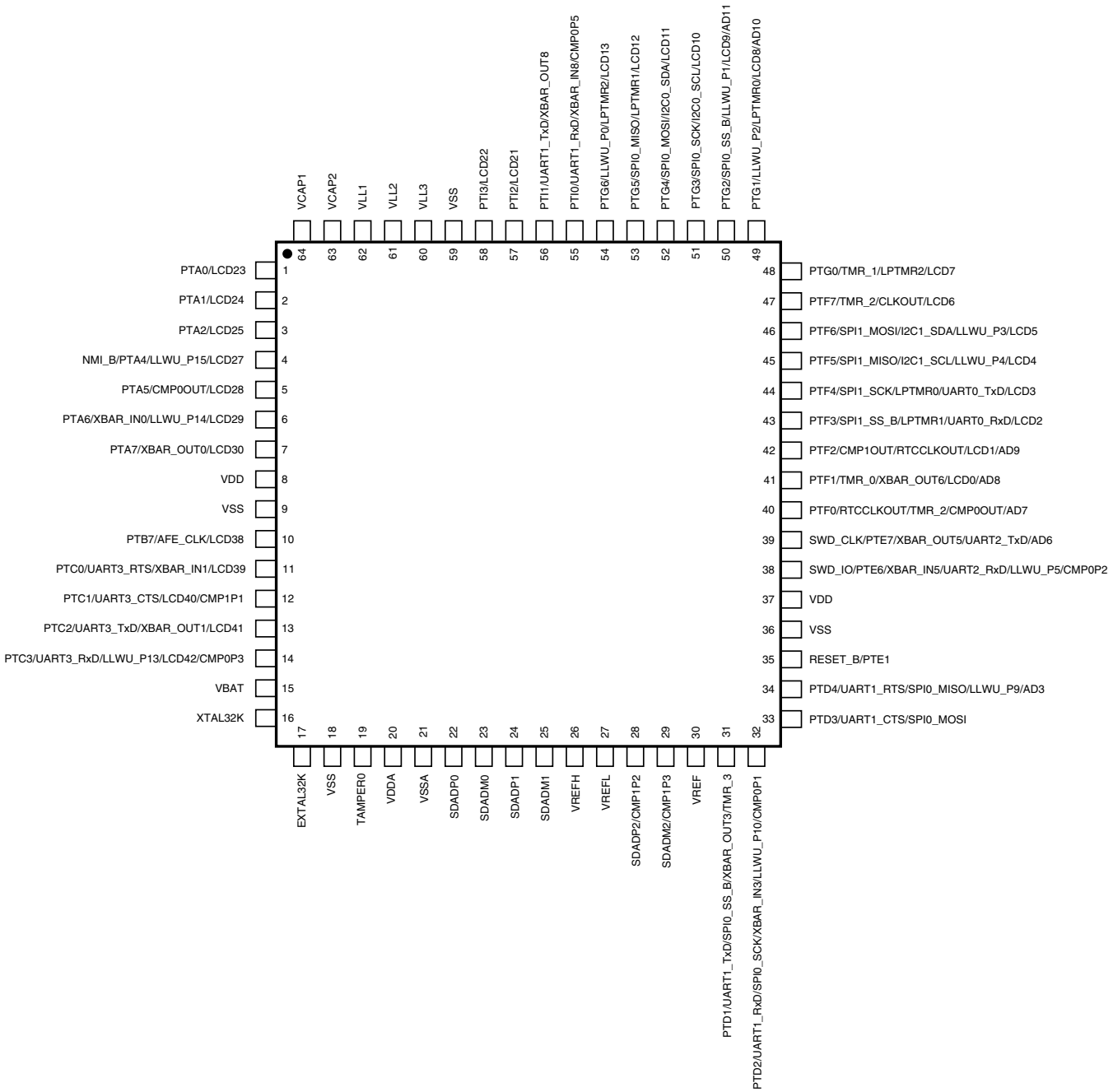


Figure 7. 64-pin LQFP Pinout Diagram

8.2.3 44-pin LGA

The following figure represents44-pin LGA pinouts:

Table 41. Revision History

Rev. No.	Date	Substantial Changes
Rev1	10/2012	Initial release
Rev2	01/2013	Updated part numbers Updated Table: Power mode transition operating behaviors Updated Table: Power consumption operating behaviors. Included readings for temperature - 40 °C, 25 °C, and 85 °C Updated AFE Modulator clock maximum value in table “Device clock specifications” Updated Table: General switching specifications Updated Table: Thermal operating requirements Updated Table: SWD switching specifications Added Table: AFE (Analog Frontend) Switching characteristics Updated Table: Oscillator DC electrical specifications Updated Table: ΣΔ ADC + PGA specifications Under section SPI switching specification, • Table SPI timing renamed to SPI switching characteristics at 2.7 V (2.7 - 3.6) • Modified row: “Data Hold Time (inputs, tHI)” to “Input Data Hold Time (inputs, tHI)” • Modified row: “Data valid time (after SCK edge, tDVO)” to “Data Valid Out Time (after SCK edge, tDVO)” Added table: SPI Switching characteristics at 1.7V (1.7 - 3.6V) NOTE added to KM Signal Multiplexing and Pin Assignments topic
Rev3	04/2013	Updated orderable part numbers Updated Table: ESD handling ratings • Add new row: Electrostatic discharge voltage, charged-device mode Updated Table: Voltage and current operating behaviors Updated Table: Power consumption operating behaviors Updated "Inputs, tSUI" row in Table: SWD switching characteristics at 2.7 V (2.7 - 3.6 V) Updated "Inputs, tSUI" row in Table: AFE switching characteristics (1.7 V - 3.6 V) Updated "Supply voltage" minimum value in table: Voltage reference electrical specifications Added table: OD cells in SPI Switching specification Updated Table: VREF full-range operating behaviors Updated Table: ΣΔ ADC + PGA specifications Updated Table: ADC standalone specifications

Table continues on the next page...