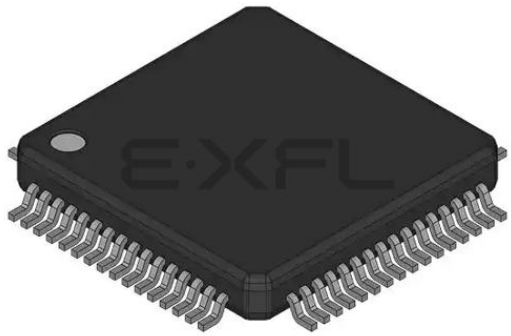

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, LCD, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 6x16b, 4x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mkm33z64clh5

Table of Contents

2.3 Fields

Following table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Pre-qualification (Proto)
K	Main family	• K = Kinetis
M	Sub family	• M1 = Metering only (No LCD support) • M3 = Metering with LCD support
S	Number of Sigma Delta (SD) ADC	• 2 = 1 SD ADC with PGA and 1 SD ADC • 3 = 2 SD ADC with PGA and 1 SD ADC • 4 = 2 SD ADC with PGA and 2 SD ADC • 8 = Same as '4'.
R	Silicon revision	• Z = Initial • (Blank) = Main • A = Revision after main
FFF	Program flash memory size	• 64 = 64 KB • 128 = 128 KB
T	Temperature range (°C)	• C = –40 to 85
PP	Package identifier	• HH = 44 LGA (5 mm x 5 mm) • LH = 64 LQFP (10 mm x 10 mm) • LL = 100 LQFP (14 mm x 14 mm)
CC	Maximum CPU frequency (MHz)	• 5 = 50 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

- MKM34Z128CLL5

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

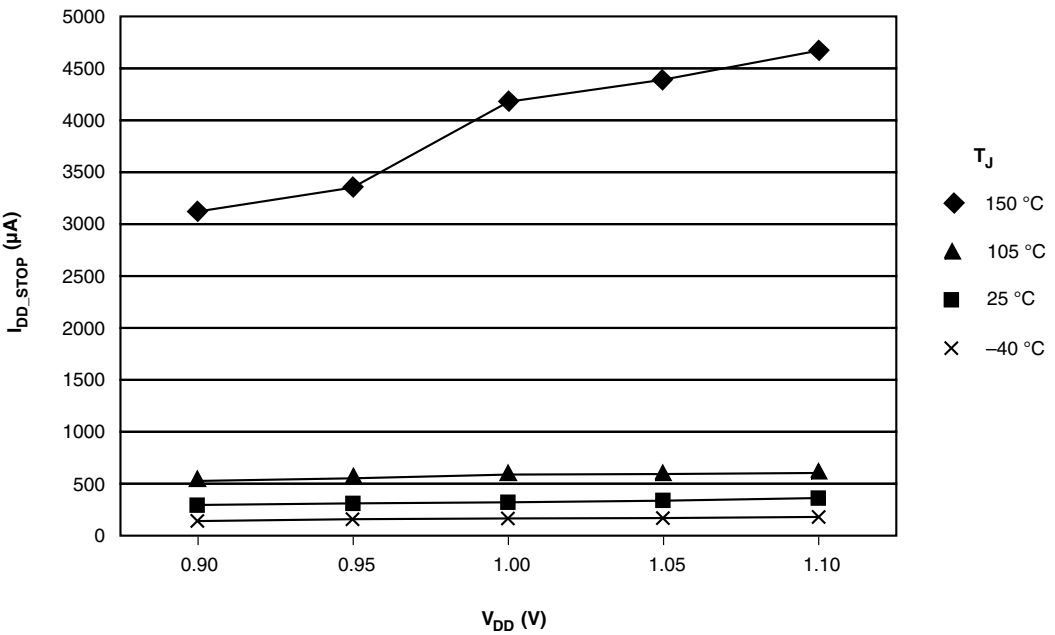
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

Table 2. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — high-drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = 20 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = 10 mA	V_{DD} – 0.5	—	V	
	Output high voltage — low-drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = 5 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = 2.5 mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	

Table continues on the next page...

5.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and I^2C signals.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Asynchronous path	16	—	ns	2
	External reset pulse width (digital glitch filter disabled)	100	—	ns	2
	Port rise and fall time—Low (All pins) and high drive (only PTC2) strength				3
	• Slew disabled				
	• $1.71 \le V_{DD} \le 2.7$ V	—	8	ns	
	• $2.7 \le V_{DD} \le 3.6$ V	—	5	ns	
	• Slew enabled				
	• $1.71 \le V_{DD} \le 2.7$ V	—	27	ns	
	• $2.7 \le V_{DD} \le 3.6$ V	—	16	ns	

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. Only PTC2 has high drive capability and load is 75 pF, other pins load (low drive) is 25 pF.

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	105	°C
T_A	Ambient temperature	–40	85	°C

6.1 Core modules

6.1.1 Single Wire Debug (SWD)

Table 12. SWD switching characteristics at 2.7 V (2.7-3.6 V)

Symbol	Description	Value	Unit	Notes
SWD CLK	Frequency of SWD operation	20	MHz	1
Inputs, tSUI	Data setup time	5	ns	1
inputs,tHI	Data hold time	0	ns	1
after clock edge, tDVO	Data valid Time	32	ns	1
tHO	Data Valid Hold	0	ns	1

1. Input transition assumed =1 ns. Output transition assumed = 50 pf.

Table 13. Switching characteristics at 1.7 V (1.7-3.6 V)

Symbol	Description	Value	Unit	Notes
SWD CLK	Frequency of SWD operation	18	MHz	
Inputs, tSUI	Data setup time	4.7	ns	
inputs,tHI	Data hold time	0	ns	
after clock edge, tDVO	Data valid Time	49.4	ns	2
tHO	Data Valid Hold	0	ns	

1. Frequency of SWD clock (18 Mhz) is applicable only in case the input setup time of the device outside is not more than 6.15 ns, else the frequency of SWD clock would need to be lowered.

6.1.2 Analog Front End (AFE)

AFE switching characteristics at (2.7 V-3.6 V)

Case1: Clock is coming In and Data is also coming In (XBAR ports timed with respect to the XBAR ports timed with respect to AFE clock defined at pad ptb[7] and pte[3])

Table 14. AFE switching characteristics (2.7 V-3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	10	MHz	1
Inputs, tSUI	Data setup time	5	ns	1
inputs,tHI	Data hold time	0	ns	1

1. Input Transition: 1ns. Output Load: 50 pf.

Case 2: Clock is going Out and Data is coming In (XBAR ports timed with respect to generated clock defined at the XBAR out ports)

Table 15. AFE switching characteristics (2.7V-3.6V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	6.2	MHz	
Inputs, tSUI	Data setup time	36	ns	
inputs,tHI	Data hold time	0	ns	

AFE switching characteristics at (1.7 V-3.6 V)

Case1: Clock is coming In and Data is also coming In (XBAR ports timed with respect to AFE clock defined at pad ptb[7] and pte[3])

Table 16. AFE switching characteristics (1.7 V-3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	10	MHz	
Inputs, tSUI	Data setup time	5.1	ns	
inputs,tHI	Data hold time	0	ns	

Case 2: Clock is going Out and Data is coming In (XBAR ports timed with respect to generated clock defined at XBAR out ports)

Table 17. AFE switching characteristics (1.7 V-3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	6.2	MHz	
Inputs, tSUI	Data setup time	54	ns	
inputs,tHI	Data hold time	0	ns	

6.2 Clock modules

6.2.1 MCG specifications

Table 18. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	

Table continues on the next page...

Table 19. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)					
	• 1 MHz resonator	—	6.6	—	kΩ	
	• 2 MHz resonator	—	3.3	—	kΩ	
	• 4 MHz resonator	—	0	—	kΩ	
	• 8 MHz resonator	—	0	—	kΩ	
	• 16 MHz resonator	—	0	—	kΩ	
	• 20 MHz resonator	—	0	—	kΩ	
	• 32 MHz resonator	—	0	—	kΩ	
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x and C_y can be provided by using either integrated capacitors or external components.
4. When low-power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

6.2.2.2 Oscillator frequency specifications

Table 20. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	1	—	8	MHz	

Table continues on the next page...

Table 24. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{pgm4}	Program Longword execution time	—	65	145	µs	
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	
t_{ersall}	Erase All Blocks execution time	—	88	650	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

6.3.1.3 Flash high voltage current behaviors

Table 25. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

6.3.1.4 Reliability specifications

Table 26. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40 °C ≤ T_j ≤ 125 °C.

6.4 Analog

6.4.1 ADC electrical specifications

All ADC channels meet the 12-bit single-ended accuracy specifications.

6.4.1.1 16-bit ADC operating conditions

Table 27. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD} – V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSA})	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input series resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance (external)	12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	3
f_{ADCK}	ADC conversion clock frequency	≤ 12-bit mode	1.0	—	18.0	MHz	4
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C_{rate}	ADC conversion rate	≤ 12-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	5
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	5

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

Table 29. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

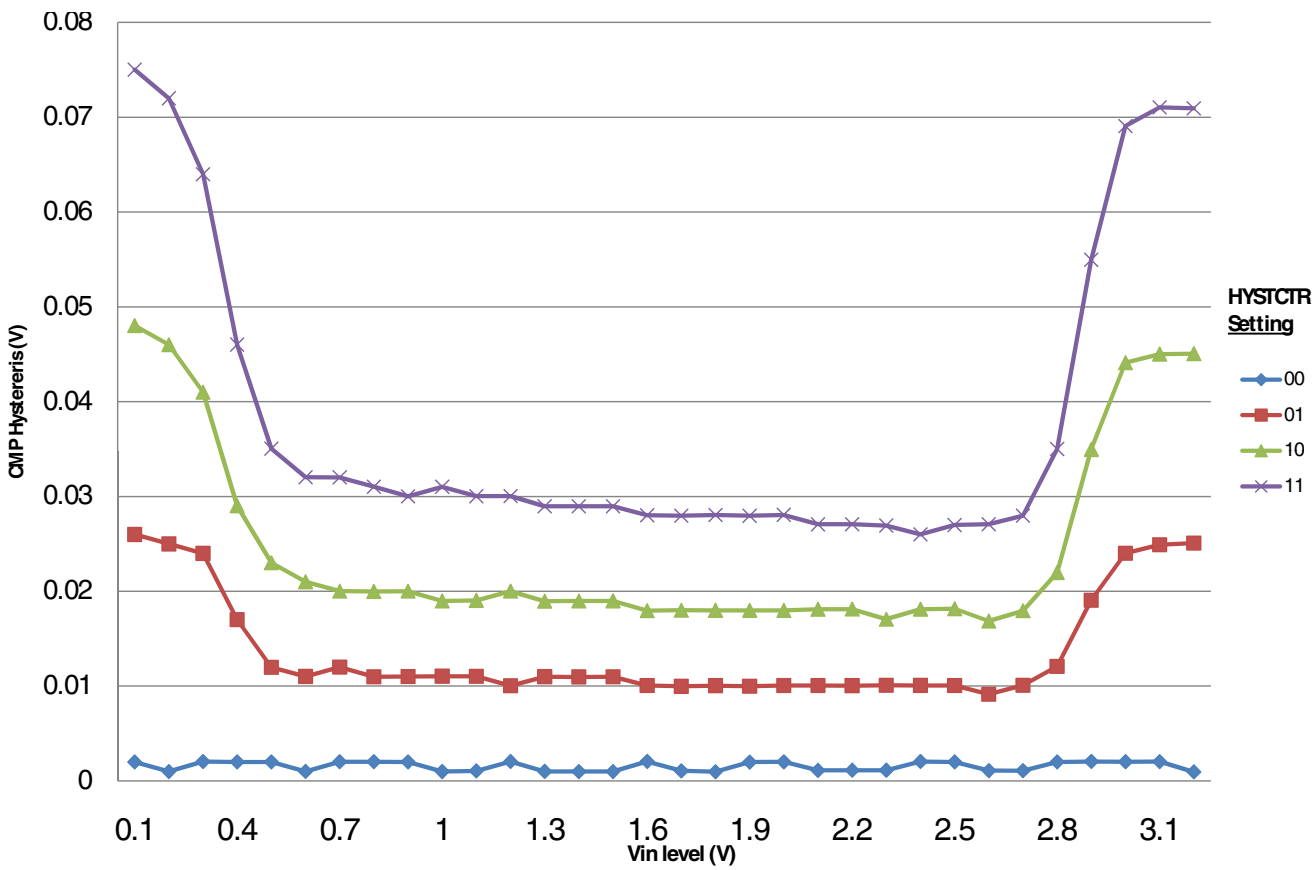


Figure 4. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

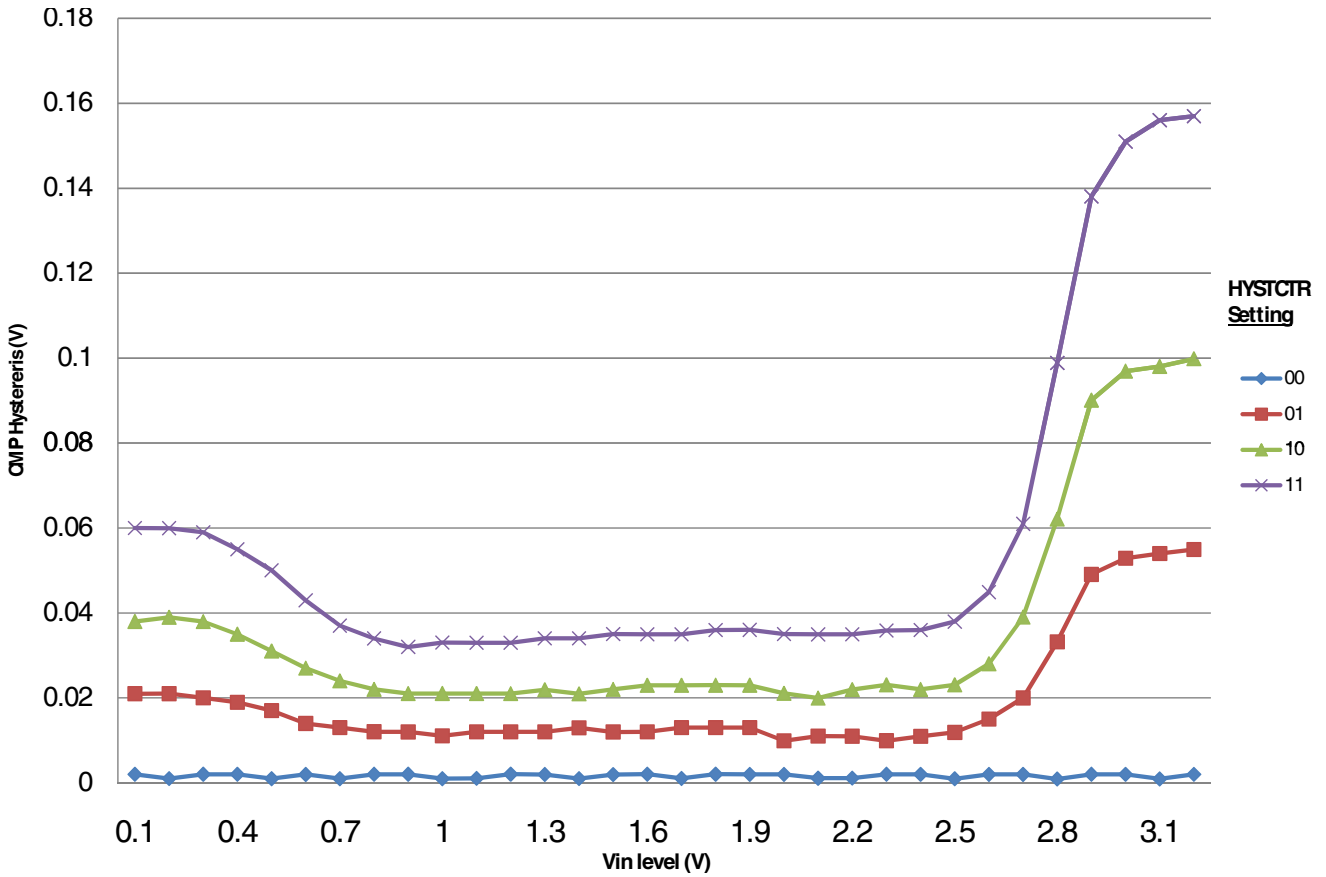


Figure 5. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

6.4.3 Voltage reference electrical specifications

Table 30. 1.2 VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71[1]	3.6	V	
T_A	Temperature	–40	85	°C	
C_L	Output load capacitance	100		nF	2, 3

1. AFE is enabled.
2. C_L must be connected between VREFH and VREFL.
3. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 31. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VREFH	Voltage reference output with factory trim at nominal V_{DDA} and temperature = 25 °C	1.1915	1.2	1.2027	V	
VREFH	Voltage reference output with — factory trim	1.1584	—	1.2376	V	

Table continues on the next page...

Table 34. ΣΔ ADC + PGA specifications (continued)

Symbol	Description	Conditions	Min	Typ[1]	Max	Unit	Notes
SINAD	Signal-to-Noise + Distortion Ratio	Normal Mode • f_{IN}=50Hz; gain=01, common mode=0V, V_{pp}=500mV (differential ended)		78		dB	
		Low-Power Mode • f_{IN}=50Hz; gain=01, common mode=0V, V_{pp}=500mV (differential ended)		74		dB	
CMMR	Common Mode Rejection Ratio	• f_{IN}=50Hz; gain=01, common mode=0V, Vid=100 mV • f_{IN}=50Hz; gain=32, common mode=0V, V_{id}=100 mV		70 70		dB	
E_{offset}	Offset Error	Gain=01, V_{pp}=1000 mV (full range diff.)			+/- 5	mV	
ΔOffset Temp	Offset Temperature Drift[3]	Gain=01, V_{pp}=1000mV (full range diff.)			+/- 25	ppm/°C	
$\Delta Gain_{Temp}$	Gain Temperate Drift - Gain error caused by temperature drifts[4]	• Gain=01, V_{pp}=500mV (differential ended) • Gain=32, V_{pp}=15mV (differential ended)			+/- 75	ppm/°C	
$PSRR_{AC}$	AC Power Supply Rejection Ratio	Gain=01, VCC = 3V ± 100mV, f_{IN} = 50 Hz		60		dB	
XT	Crosstalk (with the input of the affected channel grounded)	Gain=01, V_{id} = 500 mV, f_{IN} = 50 Hz			-100	dB	
f_{MCLK}	Modulator Clock Frequency Range	Normal Mode Low-Power Mode	0.03 0.03		6.5 1.6	MHz	
I_{DDA_PGA}	Current consumption by PGA (each channel)	Normal Mode (f_{MCLK} = 6.144 MHz, OSR= 2048) Low-Power Mode (f_{MCLK} = 0.768MHz, OSR= 256)			2.6 0	mA	5
I_{DDA_ADC}	Current Consumption by ADC (each chanel)	Normal Mode (f_{MCLK} = 6.144 MHz, OSR= 2048) Low-Power Mode (f_{MCLK} = 0.768MHz, OSR= 256)			1.4 0.5	mA	

1. Typical values assume VDDA = 3.0 V, Temp = 25°C, f_{MCLK} = 6.144 MHz, OSR = 2048 for Normal mode and f_{MCLK} = 768 kHz, OSR = 256 for Low-Power Mode unless otherwise stated. Typical values are for reference only and are not tested in production.
2. The full-scale input range in single-ended mode is 0.5Vpp
3. Represents combined offset temperature drift of the PGA, SD ADC and Internal 1.2 VREF blocks; Defined by shorting both differential inputs to ground.
4. Represents combined gain temperature drift of the PGA, SD ADC and Internal 1.2 VREF blocks.
5. PGA is disabled in low-power modes.

6.4.4.2 ΣΔ ADC Standalone specifications

Table 35. ΣΔ ADC standalone specifications

Symbol	Description	Conditions	Min	Typ[1]	Max	Unit	Notes
f_{Nyq}	Input bandwidth	Normal Mode	1.5	1.5	1.5	kHz	
		Low-Power Mode	1.5	1.5	1.5		
V_{CM}	Input Common Mode Reference		0		0.8	V	
VIN_{diff}	Input range	Differential		+/- 500		mV	
		Single Ended		+/- 250		mV	
SNR	Signal to Noise Ratio	Normal Mode • f_{IN}=50Hz; common mode=0V, V_{pp}= 500mV (differential ended) • f_{IN}=50Hz; common mode=0V, V_{pp}= 500mV (full range se.) Low-Power Mode • f_{IN}=50Hz; common mode=0V, V_{pp}=500mV (diff.) • f_{IN}=50Hz; common mode=0V, V_{pp}=500mV (full range se.)	88 76	90 78		dB	
$\Delta Gain_{Temp}$	Gain Temperate Drift - Gain error caused by temperature drifts [2]	• Gain bypassed Vpp = 500 mV (differential) • PGA bypassed Vpp = 500 mV (differential), VCM = 0 V			55	ppm/°C	
$\Delta Offset_{Temp}$	Offset Temperate Drift - Offset error caused by temperature drifts [3]	• Gain bypassed Vpp = 500 mV (differential), VCM = 0 V			30	ppm/°C	
SINAD	Signal-to-Noise + Distortion Ratio	Normal Mode • f_{IN}=50Hz; common mode=0V, V_{pp}= 500mV (diff.) • f_{IN}=50Hz; common mode=0V, V_{pp}= 500mV (full range se.) Low-Power Mode • f_{IN}=50Hz; common mode=0V, V_{pp}=500mV (diff.) • f_{IN}=50Hz; common mode=0V, V_{pp}=500mV (full range se.)		80 74		dB	
CMMR	Common Mode Rejection Ratio	• f_{IN}=50Hz; common mode=0V, V_{id}=100 mV		90		dB	
$PSRR_{AC}$	AC Power Supply Rejection Ratio	Gain=01, VCC = 3V ± 100mV, f_{IN} = 50 Hz		60		dB	
XT	Crosstalk	Gain=01, V_{id} = 500 mV, f_{IN} = 50 Hz			-100	dB	
f_{MCLK}	Modulator Clock Frequency Range	Normal Mode	0.03		6.5	MHz	
		Low-Power Mode	0.03		1.6		
I_{DDA_ADC}	Current Consumption by ADC (each channel)	Normal Mode (f_{MCLK} = 6.144 MHz, OSR= 2048)			1.4	mA	
		Low-Power Mode (f_{MCLK} = 0.768MHz, OSR= 256)			0.5		

1. Typical values assume VDDA = 3.0 V, Temp = 25°C, f_{MCLK} = 6.144 MHz, OSR = 2048 for Normal mode and f_{MCLK} = 768 kHz, OSR = 256 for Low-Power Mode unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Represent combined gain temperature drift of the SD ADC, and Internal 1.2 VREF blocks.
3. Represent combined offset temperature drift of the SD ADC, and Internal 1.2 VREF blocks; Defined by shorting both differential inputs to ground.

6.4.4.3 External modulator interface

The external modulator interface on this device comprises of a Clock signal and 1-bit data signal. Depending on the modulator device being used the interface works as follows:

- Clock supplied to external modulator which drives data on rising edge and the KM device captures it on falling edge or next rising edge.
- Clock and data are supplied by external modulator and KM device can sample it on falling edge or next rising edge.

Depending on control bit in AFE, the sampling edge is changed.

6.5 Timers

See General switching specifications.

6.6 Communication interfaces

6.6.1 I2C switching specifications

See General switching specifications.

6.6.2 UART switching specifications

See General switching specifications.

6.6.3 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following table provides some reference values to be met on SoC.

Table 36. SPI switching characteristics at 2.7 V (2.7 - 3.6)

Description	Min.	Max.	Unit	Notes
Frequency of operation (F_{sys})	—	50	MHz	1
SCK frequency • Master • Slave	2	12.5 12.5	MHz Mhz	3
SCK Duty Cycle	50%	—	—	
Data Setup Time (inputs, tSUI) • Master • Slave	25 3		ns	
Input Data Hold Time (inputs, tHI) • Master • Slave	0 1		ns	
Data hold time (outputs, tHO) • Master • Slave	0 0		ns	
Data Valid Out Time (after SCK edge, tDVO) • Master • Slave	13 28		ns	
Rise time input • Master • Slave	1 1		ns	
Fall time input • Master • Slave	1 1		ns	
Rise time output • Master • Slave	8.9 8.9		ns	
Fall time output • Master • Slave	7.8 7.8		ns	

1. SPI modules will work on core clock.
2. F_{sys}/(Max Divider Value from registers)
3. F_{SYS}/2 in Master mode and F_{SYS}/4 in Slave mode. F_{SYS}/4 in Master as well as Slave Modes, where F_{SYS}=50Mhz

NOTE

The values assumed for input transition and output load are:
Input transition = 1 ns Output load = 50 pF

Table 37. SPI switching characteristics at 1.7 V (1.7 - 3.6)

Description	Min.	Max.	Unit	Notes
Frequency of operation (F_{sys})	—	50	MHz	

Table continues on the next page...

6.7.1 LCD electrical characteristics

Table 40. LCD electricals

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{Frame}	LCD frame frequency	28	30	58	Hz	
C_{LCD}	LCD charge pump capacitance — nominal value	—	100	—	nF	1
C_{BYLCD}	LCD bypass capacitance — nominal value	—	100	—	nF	1
C_{Glass}	LCD glass capacitance	—	2000	8000	pF	2
V_{IREG}	V_{IREG}					3
	• HREFSEL=0, RVTRIM=1111	—	1.11	—	V	
	• HREFSEL=0, RVTRIM=1000	—	1.01	—	V	
	• HREFSEL=0, RVTRIM=0000	—	0.91	—	V	
Δ_{RTRIM}	V_{IREG} TRIM resolution	—	—	3.0	% V_{IREG}	
I_{VIREG}	V_{IREG} current adder — RVEN = 1	—	1	—	µA	4
I_{RBIAS}	RBIAS current adder	—	15	—	µA	
	• LADJ = 10 or 11 — High load (LCD glass capacitance ≤ 8000 pF)	—	3	—	µA	
	• LADJ = 00 or 01 — Low load (LCD glass capacitance ≤ 2000 pF)					
VLL2	VLL2 voltage					
	• HREFSEL = 0	2.0 – 5%	2.0	—	V	
VLL3	VLL3 voltage	3.0 – 5%	3.0	—	V	

1. The actual value used could vary with tolerance.
2. For highest glass capacitance values, LCD_GCR[LADJ] should be configured as specified in the LCD Controller chapter within the device's reference manual.
3. V_{IREG} maximum should never be externally driven to any level other than V_{DD} - 0.15 V.
4. 2000 pF load LCD, 32 Hz frame frequency.

NOTE

KM family devices have a 1/3 bias controller that works with a 1/3 bias LCD glass. To avoid ghosting, the LCD OFF threshold should be greater than VLL1 level. If the LCD glass has an OFF threshold less than VLL1 level, use the internal VREG mode and generate VLL1 internally using RVTRIM option. This can reduce VLL1 level to allow for a lower OFF threshold LCD glass.

7 Dimensions

100 QFP	64 QFP	44 LGA	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
18	10	—	Disabled	LCD38	PTB7	AFE_CLK					
19	11	—	Disabled	LCD39	PTC0	UART3_RTS	XBAR_IN1				
20	12	—	Disabled	LCD40/ CMP1P1	PTC1	UART3_CTS					
21	13	—	Disabled	LCD41	PTC2	UART3_TxD	XBAR_OUT1				
22	14	—	Disabled	LCD42/ CMP0P3	PTC3	UART3_RxD	LLWU_P13				
23	—	—	Disabled	LCD43	PTC4						
24	15	7	VBAT	VBAT							
25	16	8	XTAL32K	XTAL32K							
26	17	9	EXTAL32K	EXTAL32K							
27	18	10	VSS	VSS							
28	—	—	TAMPER2	TAMPER2							
29	—	—	TAMPER1	TAMPER1							
30	19	11	TAMPER0	TAMPER0							
31	20	12	VDDA	VDDA							
32	21	13	VSSA	VSSA							
33	22	14	SDADP0	SDADP0							
34	23	15	SDADM0	SDADM0							
35	24	16	SDADP1	SDADP1							
36	25	17	SDADM1	SDADM1							
37	26	18	VREFH	VREFH							
38	27	19	VREFL	VREFL							
39	28	20	SDADP2/ CMP1P2	SDADP2/ CMP1P2							
40	29	21	SDADM2/ CMP1P3	SDADM2/ CMP1P3							
41	30	22	VREF	VREF							
42	—	24	SDADP3/ CMP1P4	SDADP3/ CMP1P4							
43	—	23	SDADM3/ CMP1P5	SDADM3/ CMP1P5							
44	—	—	Disabled	AD0	PTC5	UART0_RTS	LLWU_P12				
45	—	—	Disabled	AD1	PTC6	UART0_CTS	TMR_1				
46	—	—	Disabled	AD2	PTC7	UART0_TxD	XBAR_OUT2				
47	—	—	Disabled	CMP0P0	PTD0	UART0_RxD	XBAR_IN2	LLWU_P11			
48	31	—	Disabled		PTD1	UART1_TxD	SPI0_SS_B	XBAR_OUT3	TMR_3		
49	32	—	Disabled	CMP0P1	PTD2	UART1_RxD	SPI0_SCK	XBAR_IN3	LLWU_P10		
50	33	—	Disabled		PTD3	UART1_CTS	SPI0_MOSI				
51	34	—	Disabled	AD3	PTD4	UART1_RTS	SPI0_MISO	LLWU_P9			
52	—	—	Disabled	AD4	PTD5	LPTMR2	TMR_0	UART3_CTS			
53	—	—	Disabled	AD5	PTD6	LPTMR1	CMP1OUT	UART3_RTS	LLWU_P8		
54	—	—	Disabled	CMP0P4	PTD7	I2C0_SCL	XBAR_IN4	UART3_RxD	LLWU_P7		

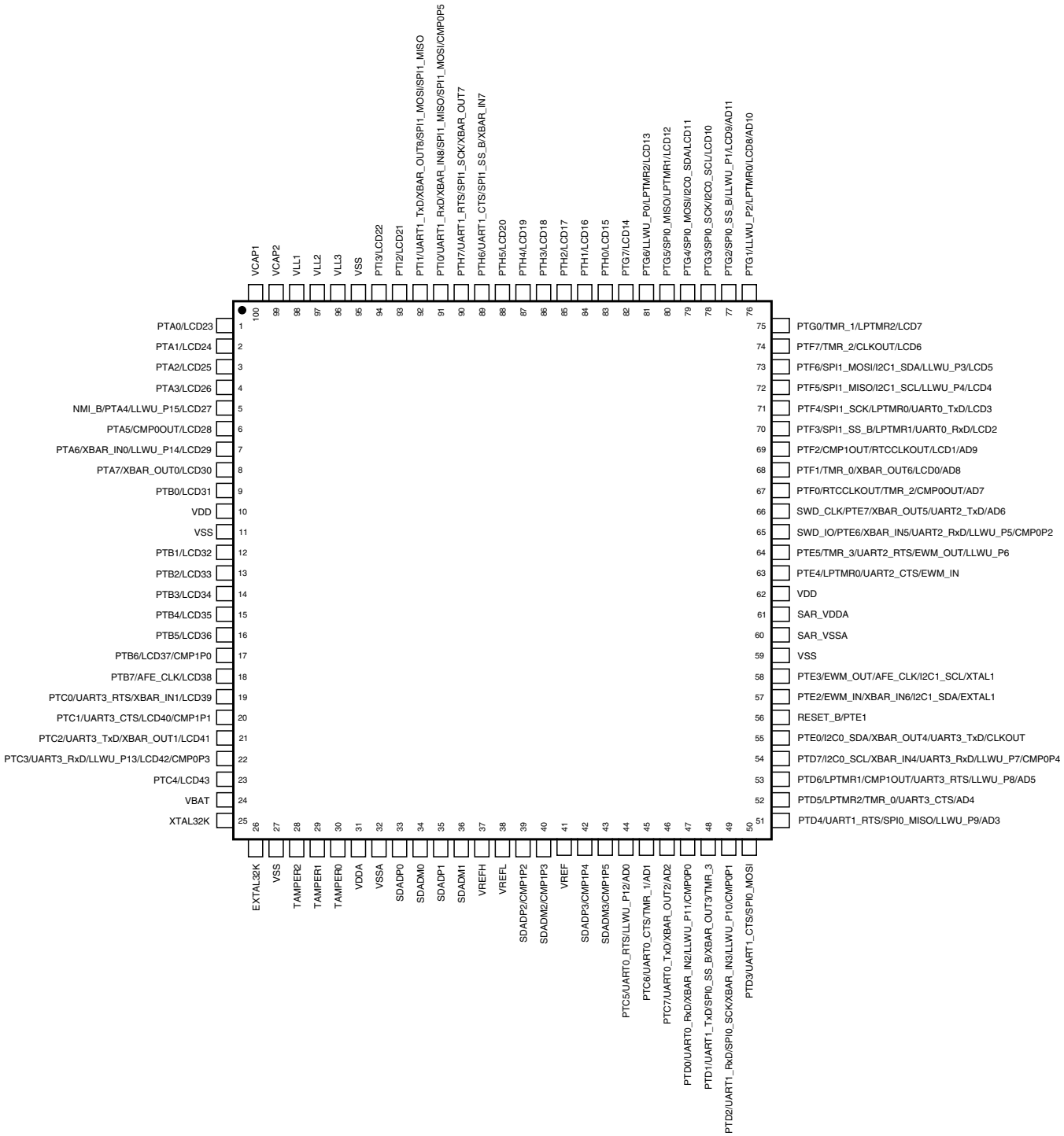


Figure 6. 100-pin LQFP Pinout Diagram

8.2.2 64-pin LQFP

The following figure represents 64-pin LQFP pinouts: