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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, LCD, WDT
Number of I/O	68
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x16b, 4x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkm33z64cll5r

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2.3 Fields

Following table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Pre-qualification (Proto)
K	Main family	• K = Kinetis
M	Sub family	• M1 = Metering only (No LCD support) • M3 = Metering with LCD support
S	Number of Sigma Delta (SD) ADC	• 2 = 1 SD ADC with PGA and 1 SD ADC • 3 = 2 SD ADC with PGA and 1 SD ADC • 4 = 2 SD ADC with PGA and 2 SD ADC • 8 = Same as '4'.
R	Silicon revision	• Z = Initial • (Blank) = Main • A = Revision after main
FFF	Program flash memory size	• 64 = 64 KB • 128 = 128 KB
T	Temperature range (°C)	• C = –40 to 85
PP	Package identifier	• HH = 44 LGA (5 mm x 5 mm) • LH = 64 LQFP (10 mm x 10 mm) • LL = 100 LQFP (14 mm x 14 mm)
CC	Maximum CPU frequency (MHz)	• 5 = 50 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

- MKM34Z128CLL5

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

3.3 Definition: Attribute

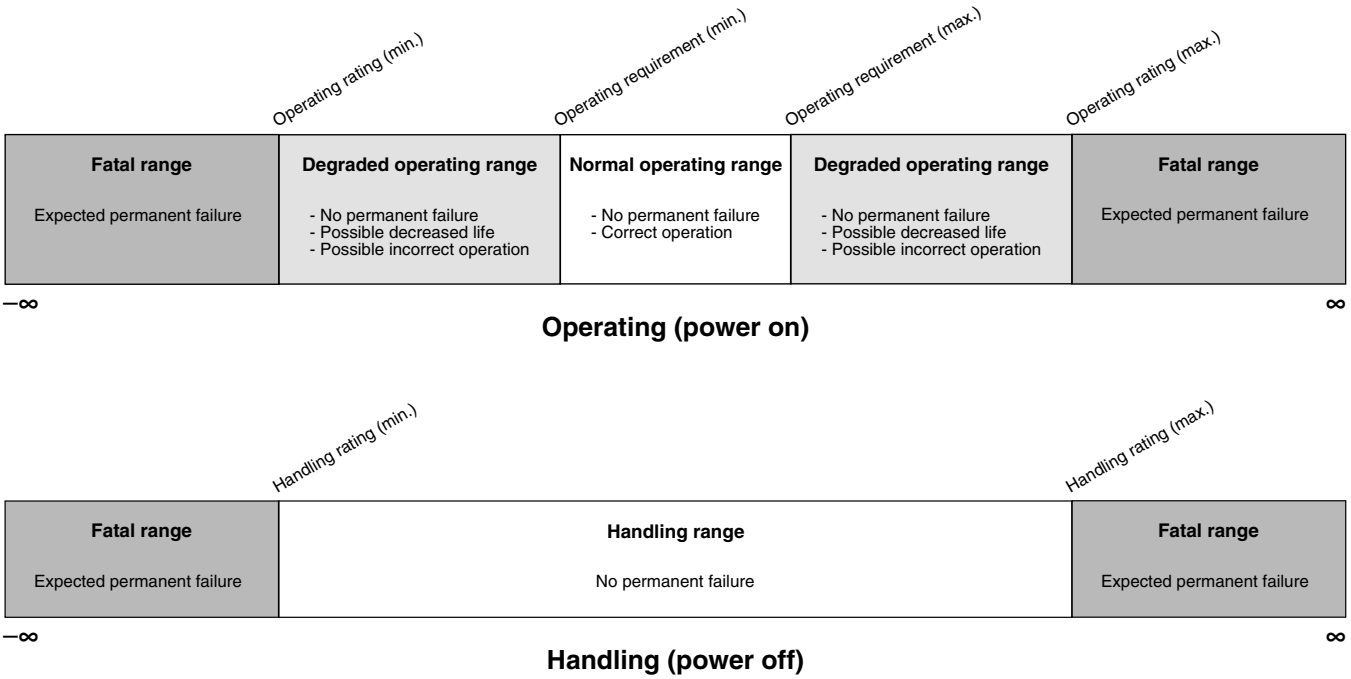
An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.6 Relationship between ratings and operating requirements



3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

Table 2. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — high-drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = 20 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = 10 mA	V_{DD} – 0.5	—	V	
	Output high voltage — low-drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = 5 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = 2.5 mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	

Table continues on the next page...

Table 5. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• STOP → RUN	—	5.0	µs	

1. Normal boot (FTFA_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					2
	• @ 3.0 V					
	• 25 °C	—	6.17	7.1	mA	
	• -40 °C	—	6.39	6.7	mA	
	• 105 °C	—	6.93	8.3	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					2
	• @ 3.0 V					
	• 25 °C	—	8.24	10.4	mA	
	• -40 °C	—	8.26	9.8	mA	
	• 105 °C	—	9.00	11.5	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V— all peripheral clocks disabled and Flash is not in low-power	—	3.95	4.65	mA	2
	• 25 °C	—		4.4	mA	
	• -40 °C	—		6	mA	
	• 105 °C					
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V— all peripheral clocks disabled and Flash disabled (put in low-power)	—	3.81	4.4	mA	2, 3
	• 25 °C	—		4.2	mA	
	• -40 °C	—		5.8	mA	
	• 105 °C					
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled					4
	• 25 °C	—	248.8	500	µA	
	• -40 °C	—	245.30	470	µA	
	• 105 °C	—	535.40	1800	µA	
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled					5
	• 25 °C	—	343.4	530	µA	
	• -40 °C	—	336.62	500	µA	
	• 105 °C	—	626.18	2000	µA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled					6
	• 25 °C	—	162	350	µA	
	• -40 °C	—	158.50	330	µA	
	• 105 °C	—	446.94	1700	µA	
I_{DD_STOP}	Stop mode current at 3.0 V					
	• 25 °C	—	311.90	730	µA	
	• -40 °C	—	364	700	µA	
	• 105 °C	—	645.13	2250	µA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• 25 °C	—	8.56	46	µA	
	• -40 °C	—		44	µA	
	• 105 °C	—		1500	µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					
	• 25 °C	—	1.98	3.5	µA	
	• -40 °C	—		3.3	µA	
	• 105 °C	—		85	µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	• 25 °C	—	1.24	2.6	µA	
	• -40 °C	—		2.5	µA	
	• 105 °C	—		59.5	µA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• 25 °C	—	0.89	1.7	µA	
	• -40 °C	—		1.6	µA	
	• 105 °C	—		38.8	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	• 25 °C	—	0.35	0.67	µA	
	• -40 °C	—		0.64	µA	
	• 105 °C	—		38	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled					
	• 25 °C	—	0.472	0.76	µA	
	• -40 °C	—		0.72	µA	
	• 105 °C	—		38.4	µA	
I_{DD_VBAT}	Average current with RTC and 32 kHz disabled at 3.0 V and VDD is OFF					
	• 25 °C	—	0.3	1	µA	
	• -40 °C	—		0.95	µA	
	• 105 °C	—		15	µA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes

I_{DD_VBAT}	Average current when VDD is OFF and LFSR and Tamper clocks set to 2 Hz.
	• @ 3.0 V
	  • 25 °C
	  • -40 °C
	  • 105 °C
		—	1.3 [7]	3
				2.5
				16
					µA
					µA
					µA
						8, 9

1. See AFE specification for IDDA.
2. 50 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FBE mode. All peripheral clocks disabled.
3. Should be reduced by 500 µA.
4. 2 MHz core, system, bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing while (1) loop from flash.
5. 2 MHz core, system and bus clock, and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing while (1) loop from flash.
6. 2 MHz core, system and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. No flash accesses; some activity on DMA & RAM assumed.
7. Current consumption will vary with number of CPU accesses done and is dependent on the frequency of the accesses and frequency of bus clock. Number of CPU accesses should be optimized to get optimal current value.
8. Includes 32 kHz oscillator current and RTC operation.
9. An external power switch for VBAT should be present on board to have better battery life and keep VBAT pin powered in all conditions. There is no internal power switch in RTC.

5.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	14	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	16	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	12	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	5	dBµV	
V_{RE_IEC}	IEC level	0.15–1000	M	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 10 MHz (crystal), f_{SYS} = 50 MHz, f_{BUS} = 25 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF
$C_{IN\_D\_io60}$	Input capacitance: fast digital pins	—	9	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock		50	MHz	
f_{BUS}	Bus clock		25	MHz	
f_{FLASH}	Flash clock		25	MHz	
f_{AFE}	AFE Modulator clock		6.5	MHz	
VLPR mode[1]					
f_{SYS}	System and core clock		2	MHz	
f_{BUS}	Bus clock		1	MHz	
f_{FLASH}	Flash clock		1	MHz	
f_{AFE}	AFE Modulator clock[2]		1.6	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.
2. AFE working in low-power mode.

5.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and I^2C signals.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Asynchronous path	16	—	ns	2
	External reset pulse width (digital glitch filter disabled)	100	—	ns	2
	Port rise and fall time—Low (All pins) and high drive (only PTC2) strength				3
	• Slew disabled				
	• $1.71 \le V_{DD} \le 2.7$ V	—	8	ns	
	• $2.7 \le V_{DD} \le 3.6$ V	—	5	ns	
	• Slew enabled				
	• $1.71 \le V_{DD} \le 2.7$ V	—	27	ns	
	• $2.7 \le V_{DD} \le 3.6$ V	—	16	ns	

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. Only PTC2 has high drive capability and load is 75 pF, other pins load (low drive) is 25 pF.

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	105	°C
T_A	Ambient temperature	–40	85	°C

Table 18. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{vco}	VCO operating frequency	11.71875	12.288	14.6484375	MHz	
I_{pll}	PLL operating current • IO 3.3 V current • Max core voltage current	—	300 100	—	µA	9
f_{pll_ref}	PLL reference frequency range	31.25	32.768	39.0625	kHz	
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 12 MHz			700	ps	10
D_{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	11
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	12

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. Chip max freq is 50 MHz, so Mid-range with DRS = 10 and High-range of DCO cannot be used and should not be configured.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. Chip max freq is 50 MHz, so Mid-range with DRS = 10 and High-range of DCO cannot be used and should not be configured.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
9. Excludes any oscillator currents that are also consuming power while PLL is in operation.
10. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
11. Will be updated later
12. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.2.2 Oscillator electrical specifications

6.2.2.1 Oscillator DC electrical specifications

Table 19. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	

Table continues on the next page...

8. ADC conversion clock < 3 MHz

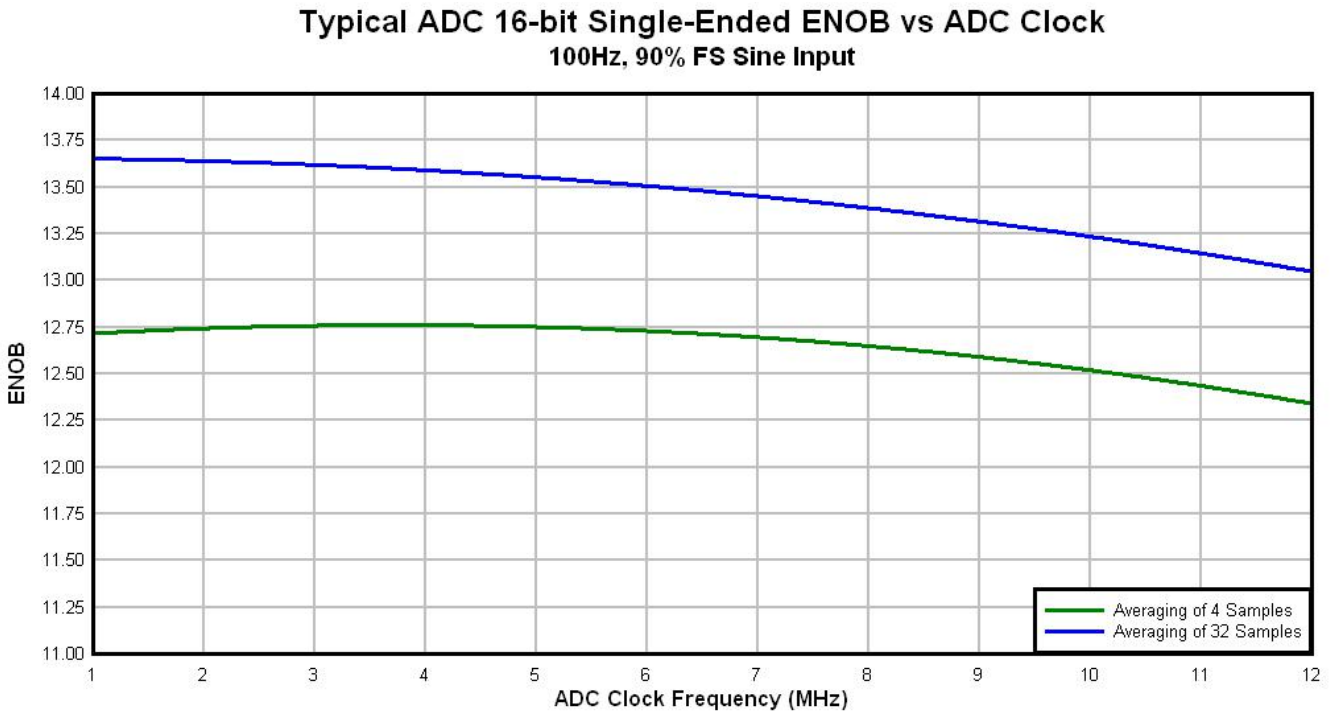


Figure 3. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

6.4.2 CMP and 6-bit DAC electrical specifications

Table 29. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns

Table continues on the next page...

6.4.4.2 ΣΔ ADC Standalone specifications

Table 35. ΣΔ ADC standalone specifications

Symbol	Description	Conditions	Min	Typ[1]	Max	Unit	Notes
f_{Nyq}	Input bandwidth	Normal Mode	1.5	1.5	1.5	kHz	
		Low-Power Mode	1.5	1.5	1.5		
V_{CM}	Input Common Mode Reference		0		0.8	V	
VIN_{diff}	Input range	Differential		+/- 500		mV	
		Single Ended		+/- 250		mV	
SNR	Signal to Noise Ratio	Normal Mode • f_{IN}=50Hz; common mode=0V, V_{pp}= 500mV (differential ended) • f_{IN}=50Hz; common mode=0V, V_{pp}= 500mV (full range se.) Low-Power Mode • f_{IN}=50Hz; common mode=0V, V_{pp}=500mV (diff.) • f_{IN}=50Hz; common mode=0V, V_{pp}=500mV (full range se.)	88 76	90 78		dB	
$\Delta Gain_{Temp}$	Gain Temperate Drift - Gain error caused by temperature drifts [2]	• Gain bypassed Vpp = 500 mV (differential) • PGA bypassed Vpp = 500 mV (differential), VCM = 0 V			55	ppm/°C	
$\Delta Offset_{Temp}$	Offset Temperate Drift - Offset error caused by temperature drifts [3]	• Gain bypassed Vpp = 500 mV (differential), VCM = 0 V			30	ppm/°C	
SINAD	Signal-to-Noise + Distortion Ratio	Normal Mode • f_{IN}=50Hz; common mode=0V, V_{pp}= 500mV (diff.) • f_{IN}=50Hz; common mode=0V, V_{pp}= 500mV (full range se.) Low-Power Mode • f_{IN}=50Hz; common mode=0V, V_{pp}=500mV (diff.) • f_{IN}=50Hz; common mode=0V, V_{pp}=500mV (full range se.)		80 74		dB	
CMMR	Common Mode Rejection Ratio	• f_{IN}=50Hz; common mode=0V, V_{id}=100 mV		90		dB	
$PSRR_{AC}$	AC Power Supply Rejection Ratio	Gain=01, VCC = 3V ± 100mV, f_{IN} = 50 Hz		60		dB	
XT	Crosstalk	Gain=01, V_{id} = 500 mV, f_{IN} = 50 Hz			-100	dB	
f_{MCLK}	Modulator Clock Frequency Range	Normal Mode	0.03		6.5	MHz	
		Low-Power Mode	0.03		1.6		
I_{DDA_ADC}	Current Consumption by ADC (each channel)	Normal Mode (f_{MCLK} = 6.144 MHz, OSR= 2048)			1.4	mA	
		Low-Power Mode (f_{MCLK} = 0.768MHz, OSR= 256)			0.5		

1. Typical values assume VDDA = 3.0 V, Temp = 25°C, f_{MCLK} = 6.144 MHz, OSR = 2048 for Normal mode and f_{MCLK} = 768 kHz, OSR = 256 for Low-Power Mode unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Represent combined gain temperature drift of the SD ADC, and Internal 1.2 VREF blocks.
3. Represent combined offset temperature drift of the SD ADC, and Internal 1.2 VREF blocks; Defined by shorting both differential inputs to ground.

6.4.4.3 External modulator interface

The external modulator interface on this device comprises of a Clock signal and 1-bit data signal. Depending on the modulator device being used the interface works as follows:

- Clock supplied to external modulator which drives data on rising edge and the KM device captures it on falling edge or next rising edge.
- Clock and data are supplied by external modulator and KM device can sample it on falling edge or next rising edge.

Depending on control bit in AFE, the sampling edge is changed.

6.5 Timers

See General switching specifications.

6.6 Communication interfaces

6.6.1 I2C switching specifications

See General switching specifications.

6.6.2 UART switching specifications

See General switching specifications.

Table 38. SPI switching characteristics at 1.7 V (1.7 - 3.6) (continued)

Description	Min.	Max.	Unit	Notes
Rise time input • Master • Slave	 1 1		ns	
Fall time input • Master • Slave	 1 1		ns	
Rise time output • Master • Slave	 30.4 30.4		ns	
Fall time output • Master • Slave	 33.5 29.0		ns	

Table 39. SPI switching characteristics at 2.7 V (2.7 - 3.6)

Description	Min.	Max.	Unit	Notes
Data Setup Time (inputs, tSUI) • Master • Slave	 29 4		ns	
Input Data Hold Time (inputs, tHI) • Master • Slave	 0 1		ns	
Data hold time (outputs, tHO) • Master • Slave	 0 0		ns	
Data Valid Out Time (after SCK edge, tDVO) • Master • Slave	 49 49		ns	
Rise time input • Master • Slave	 1 1		ns	
Fall time input • Master • Slave	 1 1		ns	
Rise time output • Master • Slave	 17.3 17.3		ns	
Fall time output • Master • Slave	 16.6 16.0		ns	

6.7 Human-Machine Interfaces (HMI)

6.7.1 LCD electrical characteristics

Table 40. LCD electricals

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{Frame}	LCD frame frequency	28	30	58	Hz	
C_{LCD}	LCD charge pump capacitance — nominal value	—	100	—	nF	1
C_{BYLCD}	LCD bypass capacitance — nominal value	—	100	—	nF	1
C_{Glass}	LCD glass capacitance	—	2000	8000	pF	2
V_{IREG}	V_{IREG}					3
	• HREFSEL=0, RVTRIM=1111	—	1.11	—	V	
	• HREFSEL=0, RVTRIM=1000	—	1.01	—	V	
	• HREFSEL=0, RVTRIM=0000	—	0.91	—	V	
Δ_{RTRIM}	V_{IREG} TRIM resolution	—	—	3.0	% V_{IREG}	
I_{VIREG}	V_{IREG} current adder — RVEN = 1	—	1	—	µA	4
I_{RBIAS}	RBIAS current adder	—	15	—	µA	
	• LADJ = 10 or 11 — High load (LCD glass capacitance ≤ 8000 pF)	—	3	—	µA	
	• LADJ = 00 or 01 — Low load (LCD glass capacitance ≤ 2000 pF)					
VLL2	VLL2 voltage					
	• HREFSEL = 0	2.0 – 5%	2.0	—	V	
VLL3	VLL3 voltage	3.0 – 5%	3.0	—	V	

1. The actual value used could vary with tolerance.
2. For highest glass capacitance values, LCD_GCR[LADJ] should be configured as specified in the LCD Controller chapter within the device's reference manual.
3. V_{IREG} maximum should never be externally driven to any level other than V_{DD} - 0.15 V.
4. 2000 pF load LCD, 32 Hz frame frequency.

NOTE

KM family devices have a 1/3 bias controller that works with a 1/3 bias LCD glass. To avoid ghosting, the LCD OFF threshold should be greater than VLL1 level. If the LCD glass has an OFF threshold less than VLL1 level, use the internal VREG mode and generate VLL1 internally using RVTRIM option. This can reduce VLL1 level to allow for a lower OFF threshold LCD glass.

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
44-pin LGA	98ASA00239D
64-pin LQFP	98ASS23234W
100-pin LQFP	98ASS23308W

8 Pinout

NOTE

VSS also connects to flag on 44 LGA.

8.1 KM Signal multiplexing and pin assignments

100 QFP	64 QFP	44 LGA	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	1	—	Disabled	LCD23	PTA0						
2	2	—	Disabled	LCD24	PTA1						
3	3	—	Disabled	LCD25	PTA2						
4	—	—	Disabled	LCD26	PTA3						
5	4	1	NMI_B	LCD27	PTA4	LLWU_P15					NMI_B
6	5	2	Disabled	LCD28	PTA5	CMP0OUT					
7	6	3	Disabled	LCD29	PTA6	XBAR_IN0	LLWU_P14				
8	7	4	Disabled	LCD30	PTA7	XBAR_OUT0					
9	—	—	Disabled	LCD31	PTB0						
10	8	5	VDD	VDD							
11	9	6	VSS	VSS							
12	—	—	Disabled	LCD32	PTB1						
13	—	—	Disabled	LCD33	PTB2						
14	—	—	Disabled	LCD34	PTB3						
15	—	—	Disabled	LCD35	PTB4						
16	—	—	Disabled	LCD36	PTB5						
17	—	—	Disabled	LCD37/ CMP1P0	PTB6						

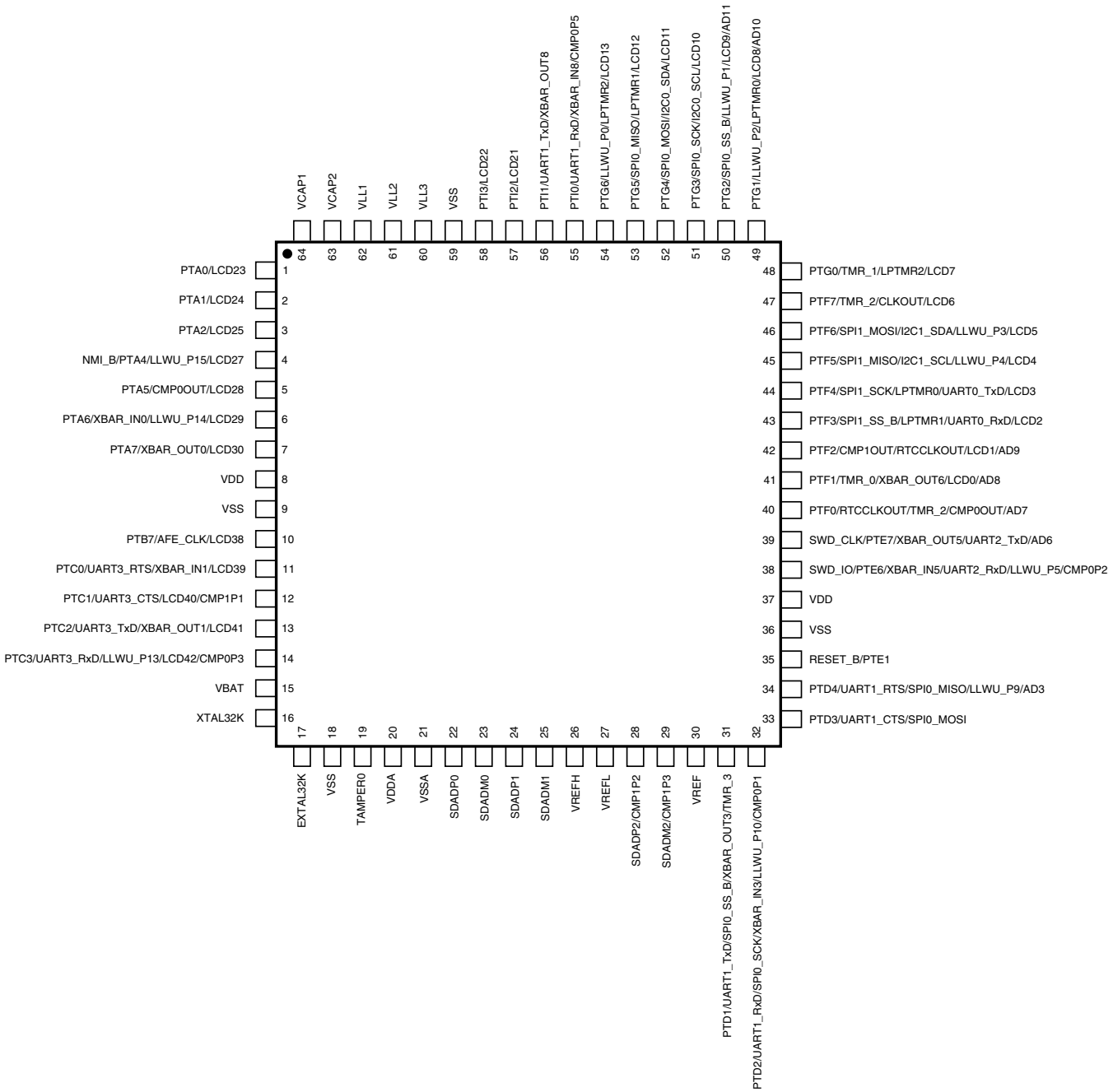


Figure 7. 64-pin LQFP Pinout Diagram

8.2.3 44-pin LGA

The following figure represents44-pin LGA pinouts:

Table 41. Revision History

Rev. No.	Date	Substantial Changes
Rev1	10/2012	Initial release
Rev2	01/2013	Updated part numbers Updated Table: Power mode transition operating behaviors Updated Table: Power consumption operating behaviors. Included readings for temperature - 40 °C, 25 °C, and 85 °C Updated AFE Modulator clock maximum value in table “Device clock specifications” Updated Table: General switching specifications Updated Table: Thermal operating requirements Updated Table: SWD switching specifications Added Table: AFE (Analog Frontend) Switching characteristics Updated Table: Oscillator DC electrical specifications Updated Table: ΣΔ ADC + PGA specifications Under section SPI switching specification, • Table SPI timing renamed to SPI switching characteristics at 2.7 V (2.7 - 3.6) • Modified row: “Data Hold Time (inputs, tHI)” to “Input Data Hold Time (inputs, tHI)” • Modified row: “Data valid time (after SCK edge, tDVO)” to “Data Valid Out Time (after SCK edge, tDVO)” Added table: SPI Switching characteristics at 1.7V (1.7 - 3.6V) NOTE added to KM Signal Multiplexing and Pin Assignments topic
Rev3	04/2013	Updated orderable part numbers Updated Table: ESD handling ratings • Add new row: Electrostatic discharge voltage, charged-device mode Updated Table: Voltage and current operating behaviors Updated Table: Power consumption operating behaviors Updated "Inputs, tSUI" row in Table: SWD switching characteristics at 2.7 V (2.7 - 3.6 V) Updated "Inputs, tSUI" row in Table: AFE switching characteristics (1.7 V - 3.6 V) Updated "Supply voltage" minimum value in table: Voltage reference electrical specifications Added table: OD cells in SPI Switching specification Updated Table: VREF full-range operating behaviors Updated Table: ΣΔ ADC + PGA specifications Updated Table: ADC standalone specifications

Table continues on the next page...