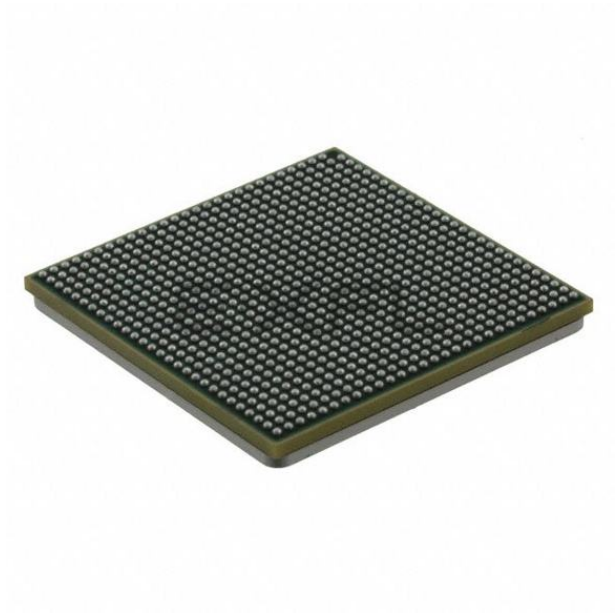

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3850 Six Core
Interface	Ethernet, I²C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	6.375MB
Voltage - I/O	1.0V, 1.5V, 2.5V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8157esag1000a

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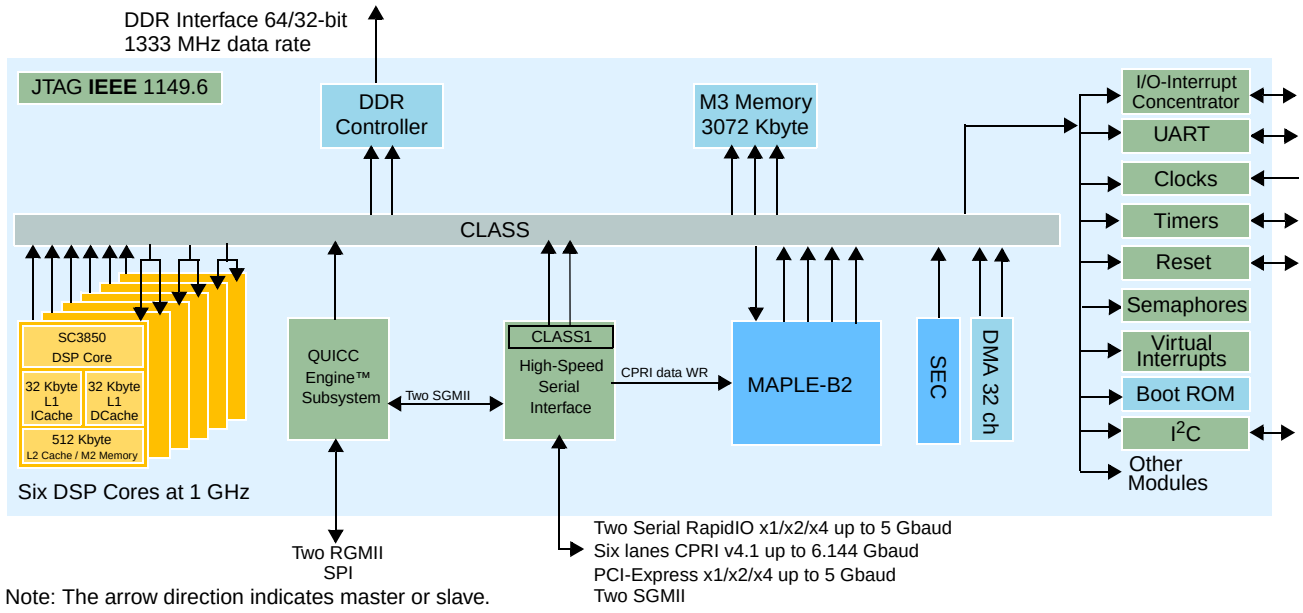


Figure 1. MSC8157E Block Diagram

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
E17	TCK	I	QVDD
E18	VSS	Ground	N/A
E19	NVDD	Power	N/A
E20	GE2_RD3\CP_LOS2	I	NVDD
E21	VSS	Ground	N/A
E22	VSS	Non-user	N/A
E23	NVDD	Power	N/A
E24	GPIO27/TMR4/RCW_SRC0	I/O	NVDD
E25	VSS	Ground	N/A
E26	GPIO0/$\overline{\text{IRQ0}}$/RC0/CP_SYNC1	I/O	NVDD
E27	GPIO17/SPI_SCK/CP_LOS3	I/O	NVDD
E28	GPIO1/$\overline{\text{IRQ1}}$/RC1/CP_SYNC2	I/O	NVDD
F1	MDQ40	I/O	GVDD
F2	MDQ41	I/O	GVDD
F3	$\overline{\text{MDQS5}}$	I/O	GVDD
F4	MDQS5	I/O	GVDD
F5	MDQ43	I/O	GVDD
F6	MDQ47	I/O	GVDD
F7	MDM6	O	GVDD
F8	VDD	Power	N/A
F9	VSS	Ground	N/A
F10	VDD	Power	N/A
F11	NC	Non-user	N/A
F12	NC	Non-user	N/A
F13	VSS	Ground	N/A
F14	NC	Non-user	N/A
F15	$\overline{\text{NMI\_OUT}}$/$\overline{\text{CP\_RX\_INT}}$	O	QVDD
F16	VSS	Ground	N/A
F17	TDI	I	QVDD
F18	VSS	Ground	N/A
F19	GE2_RD2/CP_LOS1	I	NVDD
F20	GE2_RX_CTL	I	NVDD
F21	GE2_RD0/CP_LOS6	I	NVDD
F22	GE2_RX_CLK	I	NVDD
F23	GE2_RD1	I	NVDD
F24	GPIO26/TMR3	I/O	NVDD
F25	GPIO6/$\overline{\text{IRQ6}}$/RC6/CP_SYNC5	I/O	NVDD
F26	GPIO22	I/O	NVDD
F27	GPIO23/TMR0/$\overline{\text{BOOT\_SPI\_SL}}$	I/O	NVDD
F28	GPIO8/$\overline{\text{IRQ8}}$/RC8	I/O	NVDD
G1	VSS	Ground	N/A
G2	GVDD	Power	N/A
G3	MDM5	O	GVDD
G4	VSS	Ground	N/A
G5	GVDD	Power	N/A
G6	MDQ46	I/O	GVDD

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
AH17	NC	NC	N/A
AH18	SXCVDD	Power	N/A
AH19	SD_REF_CLK2	I	SXCVDD
AH20	SXCVDD	Power	N/A
AH21	SD_J_RX	I	SXCVDD
AH22	SXCVDD	Power	N/A
AH23	SD_I_RX	I	SXCVDD
AH24	SXCVDD	Power	N/A
AH25	SXPVDD	Power	N/A
AH26	SXPVSS	Ground	N/A
AH27	$\overline{\text{SD\_H\_RX}}$	I	SXCVDD
AH28	SD_H_RX	I	SXCVDD

Notes:
1. Signal function during power-on reset is determined by the RCW source type. Selection of RapidIO, SGMII, CPRI, and PCI Express functionality during normal operation is configured by the RCW bit values. Selection of the GPIO function and other functions is done by GPIO register setup. For signals with GPIO functionality, the open-drain and internal 20 KΩ pull-up resistor can be configured by GPIO register programming. For configuration details, see the *GPIO* chapter in the *MSC8157E Reference Manual*.
2. NC signals should be disconnected for compatibility with future revisions of the device. Non-user signals are reserved for manufacturing and test purposes only. The assigned signal name is used to indicate whether the signal must be unconnected (Reserved), pulled down (VSS or SXCVSS), or pulled up (VDD).
3. Pin types are: Ground = all VSS connections; Power = all VDD connections; I = Input; O = Output; I/O = Input/Output; NC = not connected; non-user = connect as specified under Signal Name.
4. Connect power inputs to the power supplies via external filters. See the *MSC8157 Design Checklist* (AN4110) for details.

Table 2. Signal List by Primary Signal Name

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
A18	CLKIN	I	QVDD
A13	CLKOUT	O	QVDD
AA15	CPRIVDD	Power	N/A
AA17	CPRIVDD	Power	N/A
AA19	CPRIVDD	Power	N/A
AB16	CPRIVDD	Power	N/A
AB18	CPRIVDD	Power	N/A
AC15	CPRIVDD	Power	N/A
W17	CPRIVDD	Power	N/A
Y16	CPRIVDD	Power	N/A
Y18	CPRIVDD	Power	N/A
N11	CRPEVDD	Power	N/A
N7	CRPEVDD	Power	N/A
N9	CRPEVDD	Power	N/A
P10	CRPEVDD	Power	N/A
P8	CRPEVDD	Power	N/A
R11	CRPEVDD	Power	N/A
C16	DFT_TEST	I	QVDD
A14	EE0	I	QVDD
C14	EE1	O	QVDD

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
B26	GE_MDC	O	NVDD
C27	GE_MDIO	I/O	NVDD
A23	GE1_GTX_CLK	O	NVDD
H22	GE1_RD0	I	NVDD
H24	GE1_RD1	I	NVDD
G21	GE1_RD2	I	NVDD
G20	GE1_RD3	I	NVDD
G22	GE1_RX_CLK	I	NVDD
G24	GE1_RX_CTL	I	NVDD
A24	GE1_TD0	O	NVDD
A27	GE1_TD1	O	NVDD
A26	GE1_TD2	O	NVDD
A28	GE1_TD3	O	NVDD
A25	GE1_TX_CLK	I	NVDD
A22	GE1_TX_CTL	O	NVDD
C21	GE2_GTX_CLK/CP_LOS4	I/O	NVDD
F21	GE2_RD0/CP_LOS6	I	NVDD
F23	GE2_RD1	I	NVDD
F19	GE2_RD2/CP_LOS1	I	NVDD
E20	GE2_RD3/CP_LOS2	I	NVDD
F22	GE2_RX_CLK	I	NVDD
F20	GE2_RX_CTL	I	NVDD
C24	GE2_TD0	O	NVDD
C23	GE2_TD1	O	NVDD
C20	GE2_TD2/CP_LOS3	I/O	NVDD
D22	GE2_TD3/CP_LOS5	I/O	NVDD
B20	GE2_TX_CLK	I	NVDD
C22	GE2_TX_CTL	O	NVDD
E26	GPIO0/$\overline{\text{IRQ0}}$/RC0/CP_SYNC1	I/O	NVDD
E28	GPIO1/$\overline{\text{IRQ1}}$/RC1/CP_SYNC2	I/O	NVDD
D28	GPIO10/$\overline{\text{IRQ10}}$/RC10	I/O	NVDD
G28	GPIO11/$\overline{\text{IRQ11}}$/RC11	I/O	NVDD
H28	GPIO12/$\overline{\text{IRQ12}}$/RC12	I/O	NVDD
D20	GPIO13/$\overline{\text{IRQ13}}$/RC13	I/O	NVDD
H26	GPIO14/DRQ0/$\overline{\text{IRQ14}}$/RC14	I/O	NVDD
C19	GPIO15/DDN0/$\overline{\text{IRQ15}}$/RC15	I/O	NVDD
D26	GPIO16/TMR5/RC16	I/O	NVDD
E27	GPIO17/SPI_SCK/CP_LOS3	I/O	NVDD
B28	GPIO18/SPI_MOSI/CP_LOS4	I/O	NVDD
G26	GPIO19/SPI_MISO/CP_LOS5	I/O	NVDD
K28	GPIO2/$\overline{\text{IRQ2}}$/RC2/CP_SYNC3	I/O	NVDD
C26	GPIO20/$\overline{\text{SPI\_SL}}$/CP_LOS6	I/O	NVDD
C28	GPIO21/TMR6	I/O	NVDD
F26	GPIO22	I/O	NVDD
F27	GPIO23/TMR0/$\overline{\text{BOOT\_SPI\_SL}}$	I/O	NVDD
J22	GPIO24/TMR1/RCW_SRC2	I/O	NVDD

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
AD22	NC	NC	N/A
AD23	NC	NC	N/A
AD24	NC	NC	N/A
AE17	NC	NC	N/A
AE19	NC	NC	N/A
AE24	NC	NC	N/A
AF17	NC	NC	N/A
AF18	NC	NC	N/A
AF19	NC	NC	N/A
AF24	NC	NC	N/A
AG17	NC	NC	N/A
AH17	NC	NC	N/A
B10	NC	Non-user	N/A
B12	NC	Non-user	N/A
B8	NC	Non-user	N/A
C10	NC	Non-user	N/A
C11	NC	Non-user	N/A
C12	NC	Non-user	N/A
C13	NC	Non-user	N/A
C15	NC	Non-user	N/A
C8	NC	Non-user	N/A
C9	NC	Non-user	N/A
D10	NC	Non-user	N/A
D12	NC	Non-user	N/A
D14	NC	Non-user	N/A
D8	NC	Non-user	N/A
E10	NC	Non-user	N/A
E11	NC	Non-user	N/A
E12	NC	Non-user	N/A
E13	NC	Non-user	N/A
E14	NC	Non-user	N/A
E9	NC	Non-user	N/A
F11	NC	Non-user	N/A
F12	NC	Non-user	N/A
F14	NC	Non-user	N/A
G11	NC	Non-user	N/A
G12	NC	Non-user	N/A
G13	NC	Non-user	N/A
G14	NC	Non-user	N/A
H13	NC	Non-user	N/A
L22	NC	NC	N/A
L23	NC	NC	N/A
L3	NC	Non-user	N/A
M21	NC	NC	N/A
M22	NC	NC	N/A
M5	NC	Non-user	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
V18	VDD	Power	N/A
V20	VDD	Power	N/A
W19	VDD	Power	N/A
W9	VDD	Power	N/A
Y10	VDD	Power	N/A
Y20	VDD	Power	N/A
A15	VSS	Ground	N/A
A17	VSS	Ground	N/A
A19	VSS	Ground	N/A
A2	VSS	Ground	N/A
A5	VSS	Ground	N/A
AA10	VSS	Ground	N/A
AA12	VSS	Ground	N/A
AA14	VSS	Ground	N/A
AA16	VSS	Ground	N/A
AA18	VSS	Ground	N/A
AA2	VSS	Ground	N/A
AA5	VSS	Ground	N/A
AA8	VSS	Ground	N/A
AB11	VSS	Ground	N/A
AB13	VSS	Ground	N/A
AB15	VSS	Ground	N/A
AB17	VSS	Ground	N/A
AC1	VSS	Ground	N/A
AC10	VSS	Ground	N/A
AC12	VSS	Ground	N/A
AC14	VSS	Ground	N/A
AC16	VSS	Ground	N/A
AC4	VSS	Ground	N/A
AC7	VSS	Ground	N/A
AD12	VSS	Non-user	N/A
AD13	VSS	Non-user	N/A
AD14	VSS	Non-user	N/A
AD15	VSS	Ground	N/A
AD16	VSS	Ground	N/A
AE11	VSS	Ground	N/A
AE13	VSS	Non-user	N/A
AE14	VSS	Ground	N/A
AE15	VSS	Ground	N/A
AE16	VSS	Ground	N/A
AE2	VSS	Ground	N/A
AE5	VSS	Ground	N/A
AE8	VSS	Ground	N/A
AF13	VSS	Non-user	N/A
AF14	VSS	Ground	N/A
AF15	VSS	Ground	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
AF16	VSS	Ground	N/A
AG1	VSS	Ground	N/A
AG10	VSS	Ground	N/A
AG13	VSS	Ground	N/A
AG14	VSS	Ground	N/A
AG15	VSS	Ground	N/A
AG16	VSS	Ground	N/A
AG4	VSS	Ground	N/A
AG7	VSS	Ground	N/A
AH13	VSS	Ground	N/A
B11	VSS	Ground	N/A
B13	VSS	Ground	N/A
B16	VSS	Ground	N/A
B17	VSS	Ground	N/A
B18	VSS	Ground	N/A
B19	VSS	Ground	N/A
B21	VSS	Ground	N/A
B22	VSS	Non-user	N/A
B23	VSS	Ground	N/A
B25	VSS	Ground	N/A
B27	VSS	Ground	N/A
B9	VSS	Ground	N/A
C1	VSS	Ground	N/A
C18	VSS	Ground	N/A
C4	VSS	Ground	N/A
C7	VSS	Ground	N/A
D11	VSS	Ground	N/A
D13	VSS	Ground	N/A
D16	VSS	Ground	N/A
D18	VSS	Ground	N/A
D19	VSS	Non-user	N/A
D23	VSS	Ground	N/A
D9	VSS	Ground	N/A
E18	VSS	Ground	N/A
E2	VSS	Ground	N/A
E21	VSS	Ground	N/A
E22	VSS	Non-user	N/A
E25	VSS	Ground	N/A
E5	VSS	Ground	N/A
E8	VSS	Ground	N/A
F13	VSS	Ground	N/A
F16	VSS	Ground	N/A
F18	VSS	Ground	N/A
F9	VSS	Ground	N/A
G1	VSS	Ground	N/A
G10	VSS	Ground	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
M15	VSS	Ground	N/A
M17	VSS	Ground	N/A
M19	VSS	Ground	N/A
M7	VSS	Ground	N/A
M9	VSS	Ground	N/A
N10	VSS	Ground	N/A
N12	VSS	Ground	N/A
N14	VSS	Ground	N/A
N16	VSS	Ground	N/A
N18	VSS	Ground	N/A
N2	VSS	Ground	N/A
N20	VSS	Ground	N/A
N5	VSS	Ground	N/A
N8	VSS	Ground	N/A
P11	VSS	Ground	N/A
P13	VSS	Ground	N/A
P15	VSS	Ground	N/A
P17	VSS	Ground	N/A
P19	VSS	Ground	N/A
P7	VSS	Ground	N/A
P9	VSS	Ground	N/A
R10	VSS	Ground	N/A
R12	VSS	Ground	N/A
R14	VSS	Ground	N/A
R16	VSS	Ground	N/A
R18	VSS	Ground	N/A
R20	VSS	Ground	N/A
R4	VSS	Ground	N/A
R8	VSS	Ground	N/A
T1	VSS	Ground	N/A
T11	VSS	Ground	N/A
T13	VSS	Ground	N/A
T15	VSS	Ground	N/A
T17	VSS	Ground	N/A
T19	VSS	Ground	N/A
T2	VSS	Ground	N/A
T7	VSS	Ground	N/A
T9	VSS	Ground	N/A
U10	VSS	Ground	N/A
U12	VSS	Ground	N/A
U14	VSS	Ground	N/A
U16	VSS	Ground	N/A
U18	VSS	Ground	N/A
U2	VSS	Ground	N/A
U20	VSS	Ground	N/A
U5	VSS	Ground	N/A

2.2 Recommended Operating Conditions

Table 4 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 4. Recommended Operating Conditions

Rating	Supply	Min	Nominal	Max	Unit
Core supply voltage[1]	VDD	0.97	1.0	1.05	V
PLL supply voltage[1,3]	PLL0_AVDD PLL1_AVDD PLL2_AVDD MAVDD SD_PLL1_AVDD SD_PLL2_AVDD	0.97	1.0	1.05	V
CRPE supply voltage[1]	CRPEVDD	0.97	1.0	1.05	V
CPRI supply voltage[1]	CPRIVDD	0.97	1.0	1.05	V
Switchable M3 memory supply voltage[1]	M3VDD	0.97	1.0	1.05	V
DDR memory supply voltage DDR reference voltage	GVDD MVREF	1.425 0.49 × GVDD (nom)	1.5 0.5 × GVDD (nom)	1.575 0.51 × GVDD (nom)	V V
RGMII Ethernet and GPIO supply voltage[2]	NVDD	2.375	2.5	2.625	V
Input/output clocks, reset signal, and JTAG supply voltage[2]	QVDD	2.375	2.5	2.625	V
SerDes pad supply voltage	SXPVDD	1.425	1.5	1.575	V
SerDes core supply voltage[1]	SXCVDD	0.97	1.0	1.05	V
Operating temperature range: • Standard • Extended	 T_J T_A T_J	 0 –40 —		 105 — 105	 °C °C °C

Notes:
1. Designates supplies that use the same 1.0 V nominal voltage level.
2. Designates supplies that use the same 2.5 V nominal voltage level.
3. PLL supply voltage is specified at the input of the filter and not at the MSC8157E pin for the supply.

2.3 Thermal Characteristics

Table 5 describes thermal characteristics of the MSC8157E for the FC-PBGA packages.

Table 5. Thermal Characteristics for the MSC8157E

Characteristic	Symbol	FC-PBGA 29 × 29 mm^2		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	18	12	°C/W
Junction-to-ambient, four-layer board[1, 2]	$R_{\theta JA}$	13	9	°C/W
Junction-to-board (bottom)[3]	$R_{\theta JB}$	4		°C/W
Junction-to-case[4]	$R_{\theta JC}$	0.4		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESDC51-6. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-board thermal resistance determined per JEDEC JESD 51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-case at the top of the package determined using MIL- STD-883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer

2.4 CLKIN/MCLKIN Requirements

Table 6 summarizes the required characteristics for the CLKIN/MCLKIN signal.

Table 6. CLKIN/MCLKIN Requirements

Parameter/Condition[1]	Symbol	Min	Typ	Max	Unit	Notes
CLKIN/MCLKIN duty cycle	—	40	—	60	%	2
CLKIN/MCLKIN slew rate	—	1	—	4	V/ns	3
CLKIN/MCLKIN peak period jitter	—	—	—	±150	ps	—
CLKIN/MCLKIN jitter phase noise at –56 dBc	—	—	—	500	KHz	4
AC input swing limits	ΔV_{AC}	1.5	—	—	V	—
Input capacitance	C_{IN}	—	—	15	pf	5

Notes:
1. For clock frequencies, see the *Clock* chapter in the *MSC8157E Reference Manual.*
2. Measured at the rising edge and/or the falling edge at $V_{DDIO}/2$.
3. Slew rate as measured from ±20% to 80% of voltage swing at clock input.
4. Phase noise is calculated as FFT of TIE jitter.
5. The specified capacitance is not an external requirement. It represents the internal capacitance specification.

2.5 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8157E.

2.5.1 DDR SDRAM Electrical Characteristics

This section describes the DC electrical specifications for the DDR SDRAM interface of the MSC8157E. Table 7 provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Note: At recommended operating conditions (see Table 4) with GVDD = 1.5 V.

2.5.3.1 DC-Level Requirements for SerDes Reference Clocks

The DC-level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. Figure 6 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

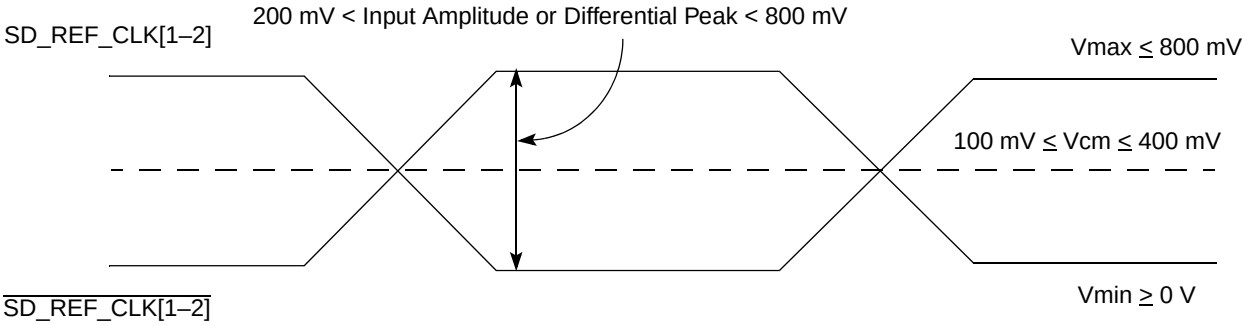


Figure 6. Differential Reference Clock Input DC Requirements (External DC-Coupled)

  - For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC-level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to GND_{SXC}. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage GND_{SXC}. Figure 7 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

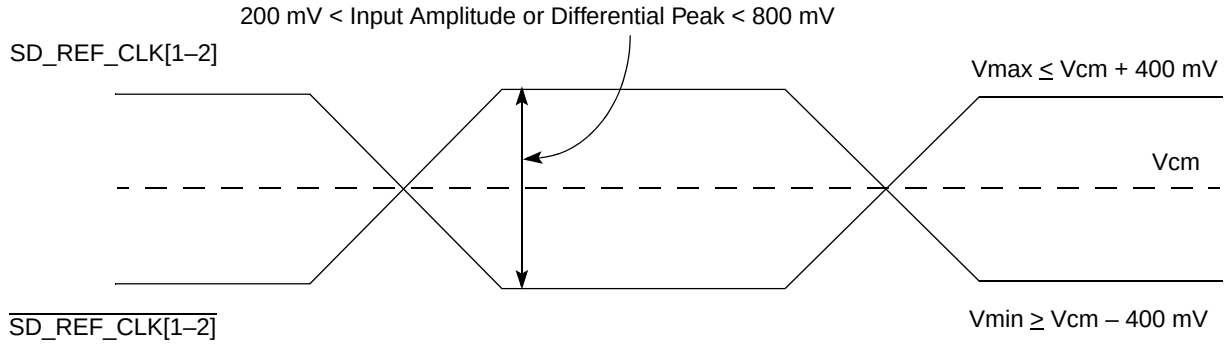


Figure 7. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- Single-Ended Mode
  - The reference clock can also be single-ended. The SD_REF_CLK[1–2] input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with $\overline{\text{SD\_REF\_CLK[1–2]}}$ either left unconnected or tied to ground.
  - The SD_REF_CLK[1–2] input average voltage must be between 200 and 400 mV. Figure 8 shows the SerDes reference clock input requirement for single-ended signaling mode.

Table 19. Serial RapidIO Transmitter DC Specifications for Long Run at 5 Gbaud (continued)

Parameter	Symbol	Min	Nom	Max	Units	Conditions
De-emphasized differential output voltage	$T\_V_{TX\text{-}DE\text{-}RATIO\text{-}3.5dB}$	3	3.5	4	dB	• p(n)_(y)_tx_eq_type[1:0] = 01 • p(n)_(y)_tx_ratio_post1q[3:0] = 1110
Tx De-emphasized level	$T\_V_{TX\text{-}DE\text{-}RATIO\text{-}6.0dB}$	5.5	6	6.5	dB	• p(n)_(y)_tx_eq_type[1:0] = 01 • p(n)_(y)_tx_ratio_post1q[3:0] = 1100
Differential resistance	T_Rd	80	100	120	Ω	

Table 20. Serial RapidIO Receiver DC Specifications for Long Run at 5 Gbaud

Parameter	Symbol	Min	Nom	Max	Units	Condition
Input differential voltage	R_Vdiff	N/A	—	1200	mV	It is assumed that for the R_Vdiff min specification, that the eye can be closed at the receiver after passing the signal through a CEI/SRIO Level II LR compliant channel.
Differential resistance	R_Rdin	80	—	120	Ω	

2.5.3.4 DC-Level Requirements for CPRI Configurations

This section provide various DC-level requirements for CPRI Configurations.

Note: Specifications are valid at the recommended operating conditions listed in Table 4.

Table 21. CPRI Transmitter DC Specifications (LV: 1.2288, 2.4576 and 3.072 Gbps)

Parameter	Symbol	Min	Nom	Max	Units	Condition
Output voltage	V_O	–0.40	—	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair.
Differential output voltage	V_{DIFFPP}	800	—	1600	mVp-p	L[A–J]TECR0[AMP_RED] = 0b000000.
Differential resistance	T_Rd	80	100	120	Ω	
Note: LV is XAUI-based.						

Table 22. CPRI Transmitter DC Specifications (LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps)

Parameter	Symbol	Min	Nom	Max	Units	Condition
Output differential voltage (into floating load Rload = 100 Ω)	T_Vdiff	800	—	1200	mV	L[A–J]TECR0[AMP_RED] = 0x000000
Differential resistance	T_Rd	80	100	120	Ω	
Note: LV-II is CEI-6G-LR-based.						

Table 23. CPRI Receiver DC Specifications (LV: 1.2288, 2.4576 and 3.072 Gbps)

Parameter	Symbol	Min	Nom	Max	Units	Condition
Differential input voltage	V_{IN}	200	—	1600	mVp-p	Measured at receiver.
Difference resistance	R_Rdin	80	—	120	Ω	
Note: LV is XAUI-based.						

Table 24. CPRI Receiver DC Specifications (LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps)

Parameter	Symbol	Min	Nom	Max	Units	Condition
Input differential voltage	R_Vdiff	N/A	—	1200	mV	It is assumed that for the R_Vdiff min specification, that the eye can be closed at the receiver after passing the signal through a CEI/CPRI Level II LR compliant channel.

Table 24. CPRI Receiver DC Specifications (continued)(LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps)

Parameter	Symbol	Min	Nom	Max	Units	Condition
Differential resistance	R_Rdin	80	—	120	Ω	
Note: LV-II is CEI-6G-LR-based.						

2.5.3.5 DC-Level Requirements for SGMII Configurations

Note: Specifications are valid at the recommended operating conditions listed in Table 4.

Table 25 describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics.

Table 25. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	500	1.45 × Nom	mV	1. The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$=1.0 V, no common mode offset variation (V_{OS} =500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and $\overline{\text{SD\_TXn}}$. 2. Amplitude setting: [A–J]TECR0[AMD_RED] = 0b000000
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	459	1.45 × Nom	mV	1. The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$=1.0V, no common mode offset variation (V_{OS} =500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and $\overline{\text{SD\_TXn}}$. 2. Amplitude setting: [A–J]TECR0[AMD_RED] = 0b000010
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	417	1.45 × Nom	mV	1. The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$=1.0V, no common mode offset variation (V_{OS} =500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and $\overline{\text{SD\_TXn}}$. 2. Amplitude setting: [A–J]TECR0[AMD_RED] = 0b000101
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	376	1.45 × Nom	mV	1. The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$=1.0V, no common mode offset variation (V_{OS} =500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and $\overline{\text{SD\_TXn}}$. 2. Amplitude setting: [A–J]TECR0[AMD_RED] = 0b001000
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	333	1.45 × Nom	mV	1. The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$=1.0V, no common mode offset variation (V_{OS} =500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and $\overline{\text{SD\_TXn}}$. 2. Amplitude setting: [A–J]TECR0[AMD_RED] = 0b001100

2.6 AC Timing Characteristics

This section describes the AC timing characteristics for the MSC8157E.

2.6.1 DDR SDRAM AC Timing Specifications

This section describes the AC electrical characteristics for the DDR SDRAM interface.

2.6.1.1 DDR SDRAM Input AC Timing Specifications

Table 28 provides the input AC timing specifications for the DDR SDRAM when V_{DDDDR} (typ) = 1.5 V.

Table 28. DDR3 SDRAM Input AC Timing Specifications for 1.5 V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage • > 1200 MHz data rate • ≤ 1200 MHz data rate	V_{ILAC}	—	 MV_{REF} – 0.150 MV_{REF} – 0.175	V
AC input high voltage • > 1200 MHz data rate • ≤ 1200 MHz data rate	V_{IHAC}	 MV_{REF} + 0.150 MV_{REF} + 0.175	—	V
Note: At recommended operating conditions with V_{DDDDR} of 1.5 ± 5%.				

Table 29 provides the input AC timing specifications for the DDR SDRAM interface.

Table 29. DDR SDRAM Input AC Timing Specifications

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}				1, 2, 4
• 1333 MHz data rate		–125	125	ps	
• 1200 MHz data rate		–142	142	ps	
• 1066 MHz data rate		–170	170	ps	
• 800 MHz data rate		–200	200	ps	
• 667 MHz data rate		–240	240	ps	
Tolerated Skew for MDQS—MDQ/MECC	t_{DISKEW}				2, 3
• 1333 MHz data rate		–250	250	ps	
• 1200 MHz data rate		–275	275	ps	
• 1066 MHz data rate		–300	300	ps	
• 800 MHz data rate		–425	425	ps	
• 667 MHz data rate		–510	510	ps	

Notes:
1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. Subtract this value from the total timing budget.
2. At recommended operating conditions with V_{DDDDR} (1.5 V) ± 5%
3. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.
4. The t_{CISKEW} test coverage is derived from the t_{DISKEW} parameters.

Figure 9 shows the DDR3 SDRAM interface input timing diagram.

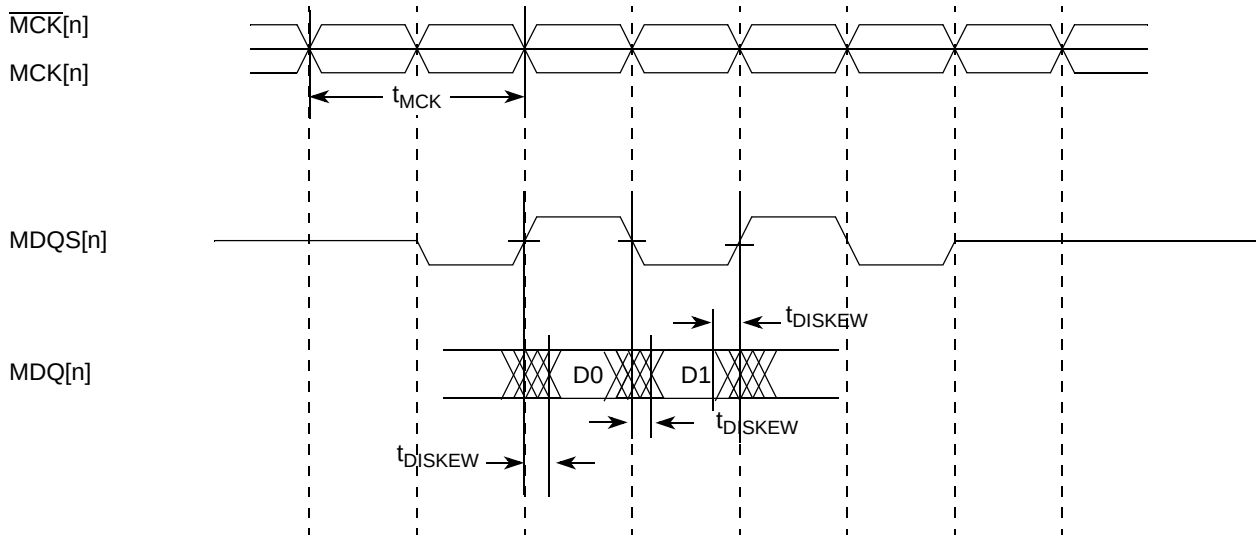


Figure 9. DDR3 SDRAM Interface Input Timing Diagram

2.6.1.2 DDR SDRAM Output AC Timing Specifications

Table 30 provides the output AC timing specifications for the DDR SDRAM interface.

Table 30. DDR SDRAM Output AC Timing Specifications

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	1.5	3	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}				3
• 1333 MHz data rate		0.606	—	ns	
• 1200 MHz data rate		0.675	—	ns	
• 1066 MHz data rate		0.744	—	ns	
• 800 MHz data rate		0.917	—	ns	
• 667 MHz data rate		1.10	—	ns	
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}				3
• 1333 MHz data rate		0.606	—	ns	
• 1200 MHz data rate		0.675	—	ns	
• 1066 MHz data rate		0.744	—	ns	
• 800 MHz data rate		0.917	—	ns	
• 667 MHz data rate		1.10	—	ns	
$\overline{\text{MCS}}$n output setup with respect to MCK	t_{DDKHCS}				3
• 1333 MHz data rate		0.606	—	ns	
• 1200 MHz data rate		0.675	—	ns	
• 1066 MHz data rate		0.744	—	ns	
• 800 MHz data rate		0.917	—	ns	
• 667 MHz data rate		1.10	—	ns	
$\overline{\text{MCS}}$n output hold with respect to MCK	t_{DDKHCX}				3
• 1333 MHz data rate		0.606	—	ns	
• 1200 MHz data rate		0.675	—	ns	
• 1066 MHz data rate		0.744	—	ns	
• 800 MHz data rate		0.917	—	ns	
• 667 MHz data rate		1.10	—	ns	
MCK to MDQS Skew	t_{DDKHMH}				4
• > 1066 MHz data rate		–0.245	0.245	ns	
• 800 MHz data rate		–0.375	0.375	ns	
• 667 MHz data rate		–0.6	0.6	ns	

Figure 11 shows the DDR SDRAM output timing diagram.

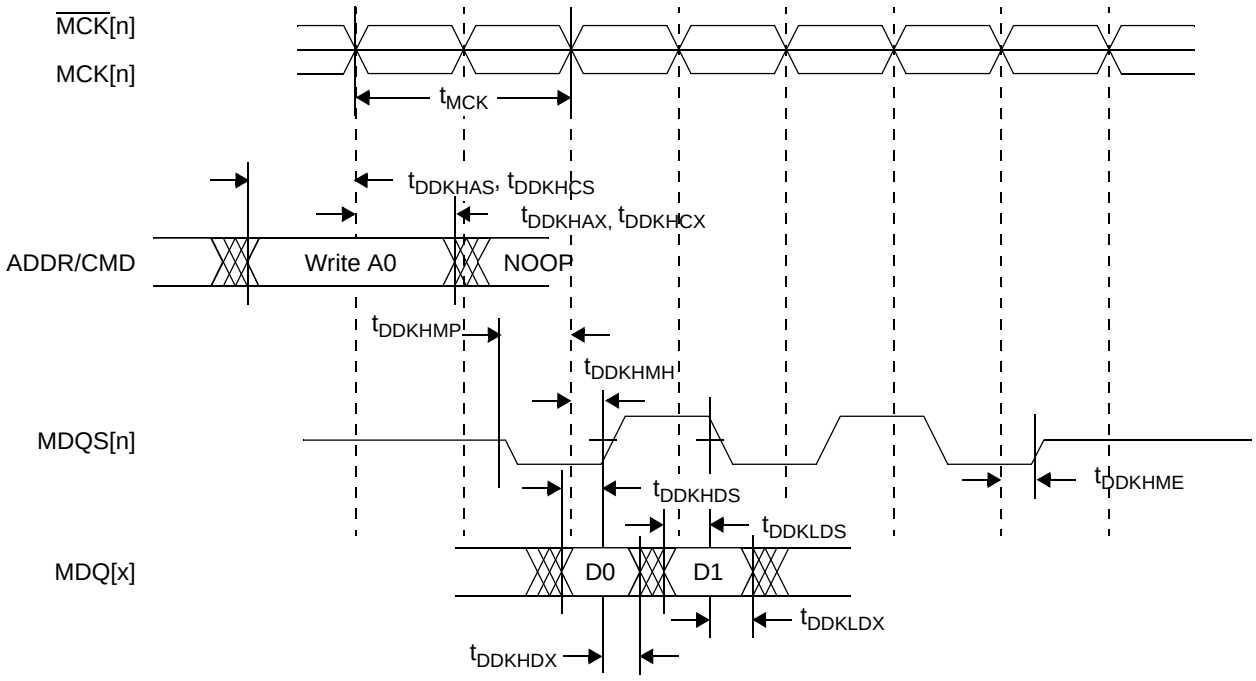


Figure 11. DDR SDRAM Output Timing

Figure 12 provides the AC test load for the DDR3 controller bus.

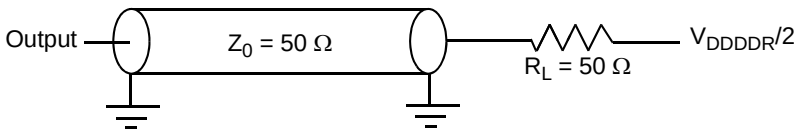


Figure 12. DDR3 Controller Bus AC Test Load

2.6.1.3 DDR3 SDRAM Differential Timing Specifications

This section describes the DC and AC differential timing specifications for the DDR3 SDRAM controller interface. Figure 13 shows the differential timing specification.

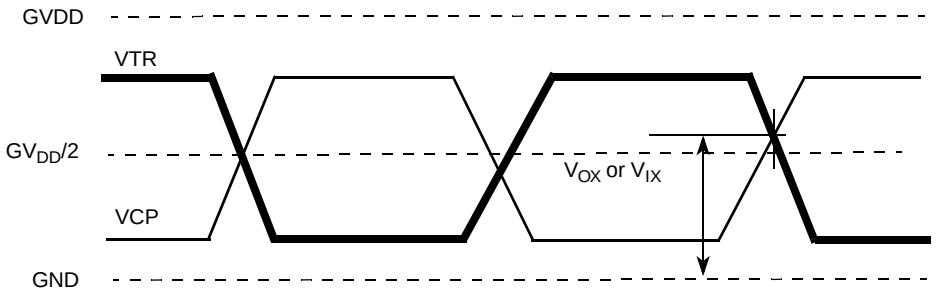


Figure 13. DDR3 SDRAM Differential Timing Specifications

Note: VTR specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as $\overline{\text{MCK}}$ or $\overline{\text{MDQS}}$).

Table 31 provides the DDR3 differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$.

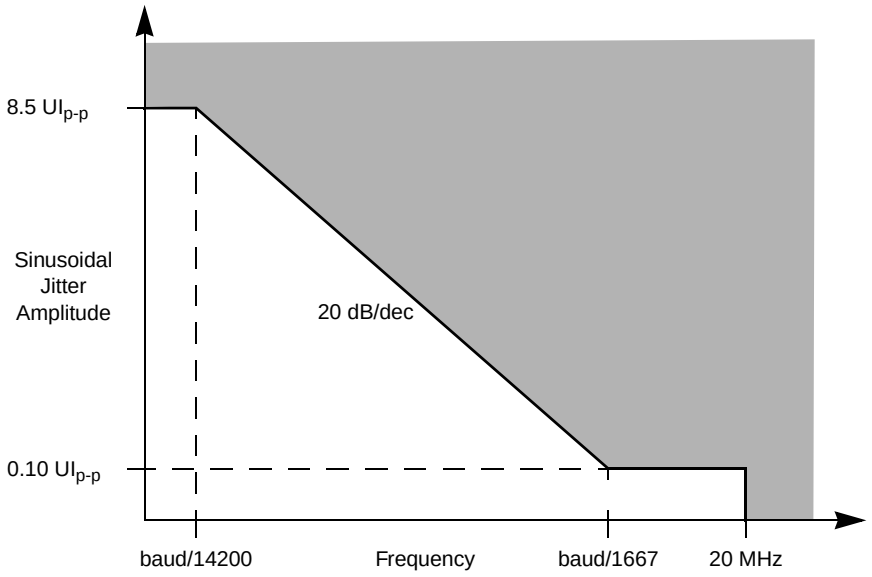


Figure 20. Single Frequency Sinusoidal Jitter Limits for Baud Rate <3.125 Gbps

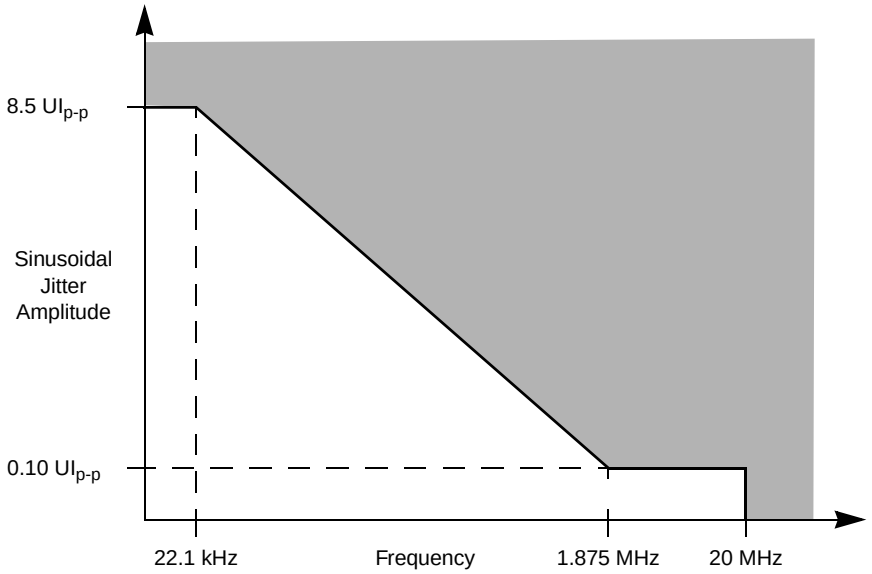


Figure 21. Single Frequency Sinusoidal Jitter Limits for Baud Rate 3.125 Gbps

2.6.3 Timers and Timers_32b AC Timing Specifications

Table 49 lists the timer input AC timing specifications.

Table 49. Timers Input AC Timing Specifications

Characteristics	Symbol	Minimum	Unit	Notes
Timers inputs—minimum pulse width	T_{TIWID}	8	ns	1, 2

Notes:
1. The maximum allowed frequency of timer outputs is 125 MHz. Configure the timer modules appropriately.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

Note: For recommended operating conditions, see Table 4.

2.6.4.2 RGMII AC Timing Specifications

Table 51 presents the RGMII AC timing specifications for applications requiring an on-board delayed clock.

Table 51. RGMII at 1 Gbps with On-Board Delay[2] AC Timing Specifications[1]

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)[3]	t_{SKEWT}	–0.5	—	0.5	ns
Data to clock input skew (at receiver)[3]	t_{SKEWR}	1	—	2.6	ns

Notes:
1. At recommended operating conditions with V_{DDIO} of 2.5 V ± 5%.
2. Program GCR4 as 0x00000000, UCC1_DELAY_HR as 0x00000000, and UCC3_DELAY_HR as 0x00000000.
3. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns is added to the associated clock signal.

Figure 24 shows the RGMII AC timing and multiplexing diagrams.

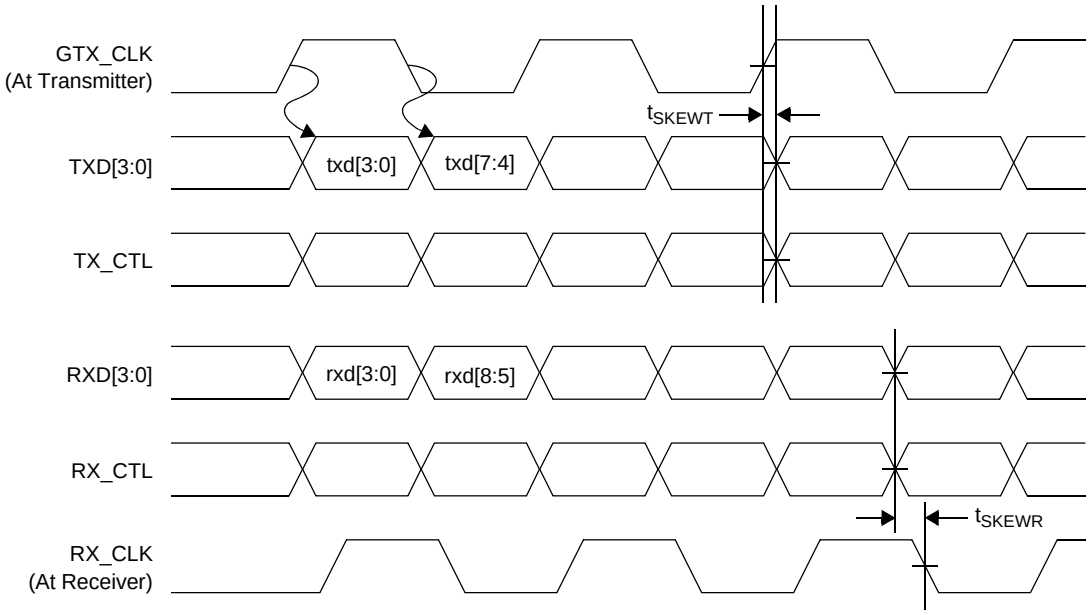
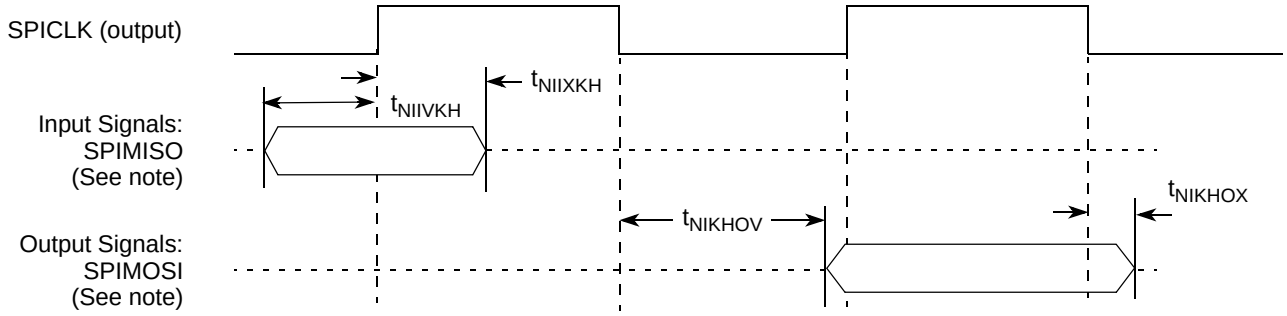


Figure 24. RGMII AC Timing and Multiplexing



Note: measured with SPMODE[CI] = 0, SPMODE[CP] = 0

Figure 27. SPI AC Timing in Master Mode (Internal Clock)

2.6.6 Asynchronous Signal Timing

Table 53 lists the asynchronous signal timing specifications.

Table 53. Signal Timing

Characteristics	Symbol	Type	Min
Input	t_{IN}	Asynchronous	One CLKIN/MCLKIN cycle
Output	t_{OUT}	Asynchronous	Application dependent
Note: Input value relevant for EE0, $\overline{\text{IRQ}}$[15–0], and $\overline{\text{NMI}}$ only.			

The following interfaces use the specified asynchronous signals:

- *GPIO*. Signals GPIO[31–0], when used as GPIO signals, that is, when the alternate multiplexed special functions are not selected.

Note: When used as a general purpose input (GPI), the input signal should be driven until it is acknowledged by the MSC8157E device, that is, when the expected input value is read from the GPIO data register.

- *EE port.* Signals EE0, EE1.
- *Boot function*. Signal STOP_BS.
- *I^2C interface*. Signals I2C_SCL and I2C_SDA.
- *Interrupt inputs*. Signals $\overline{\text{IRQ}}$[15–0] and $\overline{\text{NMI}}$.
- *Interrupt outputs*. Signals $\overline{\text{INT\_OUT}}$/$\overline{\text{CP\_TX\_INT}}$ and $\overline{\text{NMI\_OUT}}$/$\overline{\text{CP\_RX\_INT}}$ (minimum pulse width is 32 ns).

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