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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	SC3850 Six Core
Interface	Ethernet, I²C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	6.375MB
Voltage - I/O	1.00V, 1.50V, 2.50V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=msc8157esvt1000a

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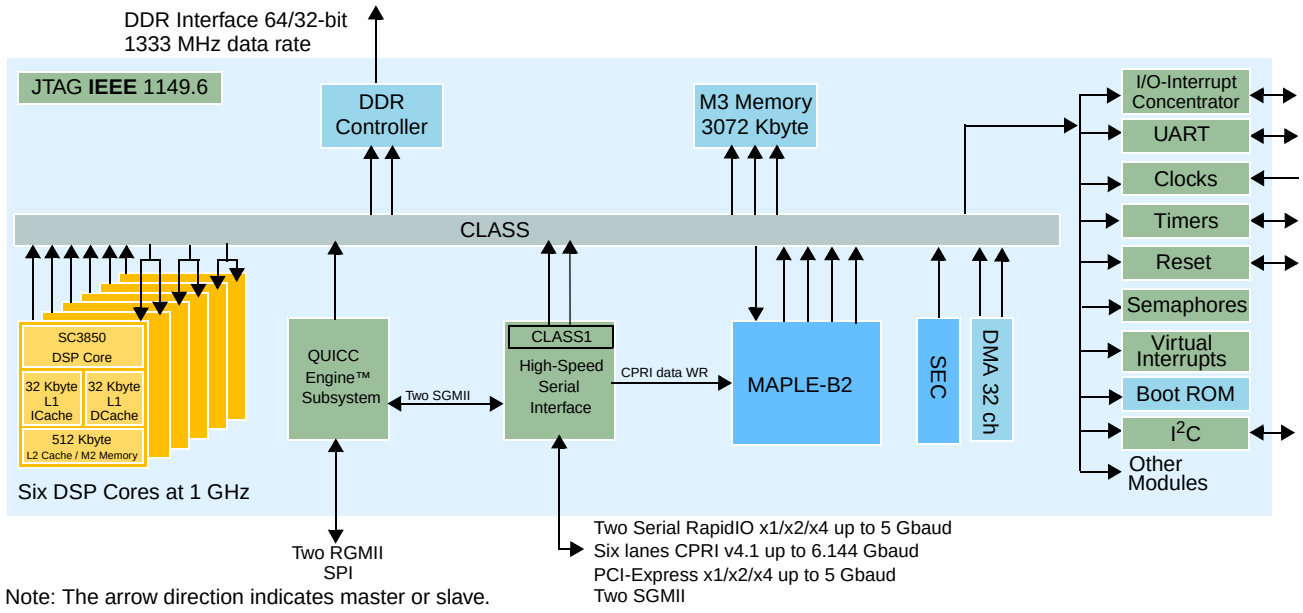


Figure 1. MSC8157E Block Diagram

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
M5	NC	Non-user	N/A
M6	NC	Non-user	N/A
M7	VSS	Ground	N/A
M8	VDD	Power	N/A
M9	VSS	Ground	N/A
M10	VDD	Power	N/A
M11	VSS	Ground	N/A
M12	VDD	Power	N/A
M13	VSS	Ground	N/A
M14	VDD	Power	N/A
M15	VSS	Ground	N/A
M16	VDD	Power	N/A
M17	VSS	Ground	N/A
M18	VDD	Power	N/A
M19	VSS	Ground	N/A
M20	VDD	Power	N/A
M21	NC	NC	N/A
M22	NC	NC	N/A
M23	SD_A_TX	O	SXPVDD
M24	$\overline{\text{SD\_A\_TX}}$	O	SXPVDD
M25	SXPVDD	Power	N/A
M26	SXPVSS	Ground	N/A
M27	$\overline{\text{SD\_A\_RX}}$	I	SXCVDD
M28	SD_A_RX	I	SXCVDD
N1	$\overline{\text{MRAS}}$	O	GVDD
N2	VSS	Ground	N/A
N3	NC	Non-user	N/A
N4	GVDD	Power	N/A
N5	VSS	Ground	N/A
N6	MODT1	O	GVDD
N7	CRPEVDD	Power	N/A
N8	VSS	Ground	N/A
N9	CRPEVDD	Power	N/A
N10	VSS	Ground	N/A
N11	CRPEVDD	Power	N/A
N12	VSS	Ground	N/A
N13	VDD	Power	N/A
N14	VSS	Ground	N/A
N15	VDD	Power	N/A
N16	VSS	Ground	N/A
N17	VDD	Power	N/A
N18	VSS	Ground	N/A
N19	VDD	Power	N/A
N20	VSS	Ground	N/A
N21	NC	NC	N/A
N22	NC	NC	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
AB1	$\overline{\text{MDQS8}}$	I/O	GVDD
AB2	MDM8	O	GVDD
AB3	MECC2	I/O	GVDD
AB4	MECC1	I/O	GVDD
AB5	NC	Non-user	N/A
AB6	MAPAR_IN	I	GVDD
AB7	MBA2	O	GVDD
AB8	MDQ2	I/O	GVDD
AB9	MDQ1	I/O	GVDD
AB10	MDQ0	I/O	GVDD
AB11	VSS	Ground	N/A
AB12	M3VDD	Power	N/A
AB13	VSS	Ground	N/A
AB14	M3VDD	Power	N/A
AB15	VSS	Ground	N/A
AB16	CPRIVDD	Power	N/A
AB17	VSS	Ground	N/A
AB18	CPRIVDD	Power	N/A
AB19	NC	NC	N/A
AB20	NC	Non-user	N/A
AB21	NC	NC	N/A
AB22	NC	NC	N/A
AB23	NC	NC	N/A
AB24	NC	NC	N/A
AB25	SXPVDD	Power	N/A
AB26	SXPVSS	Ground	N/A
AB27	$\overline{\text{SD\_E\_RX}}$	I	SXCVDD
AB28	SD_E_RX	I	SXCVDD
AC1	VSS	Ground	N/A
AC2	GVDD	Power	N/A
AC3	MECC4	I/O	GVDD
AC4	VSS	Ground	N/A
AC5	GVDD	Power	N/A
AC6	MDQ25	I/O	GVDD
AC7	VSS	Ground	N/A
AC8	GVDD	Power	N/A
AC9	MDQ3	I/O	GVDD
AC10	VSS	Ground	N/A
AC11	GVDD	Power	N/A
AC12	VSS	Ground	N/A
AC13	M3VDD	Power	N/A
AC14	VSS	Ground	N/A
AC15	CPRIVDD	Power	N/A
AC16	VSS	Ground	N/A
AC17	NC	NC	N/A
AC18	NC	NC	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
AC19	NC	NC	N/A
AC20	NC	Non-user	N/A
AC21	NC	NC	N/A
AC22	NC	NC	N/A
AC23	NC	NC	N/A
AC24	NC	NC	N/A
AC25	SD_F_TX	O	SXPVDD
AC26	$\overline{\text{SD\_F\_TX}}$	O	SXPVDD
AC27	SXCVSS	Ground	N/A
AC28	SXCVDD	Power	N/A
AD1	MECC7	I/O	GVDD
AD2	MECC6	I/O	GVDD
AD3	MECC0	I/O	GVDD
AD4	MECC5	I/O	GVDD
AD5	MECC3	I/O	GVDD
AD6	MDQ24	I/O	GVDD
AD7	MDM0	O	GVDD
AD8	$\overline{\text{MDQS0}}$	I/O	GVDD
AD9	MDQS0	I/O	GVDD
AD10	MDQ4	I/O	GVDD
AD11	MDQ6	I/O	GVDD
AD12	VSS	Non-user	N/A
AD13	VSS	Non-user	N/A
AD14	VSS	Non-user	N/A
AD15	VSS	Ground	N/A
AD16	VSS	Ground	N/A
AD17	NC	NC	N/A
AD18	SD_PLL2_AVDD	Power	N/A
AD19	NC	NC	N/A
AD20	NC	NC	N/A
AD21	NC	NC	N/A
AD22	NC	NC	N/A
AD23	NC	NC	N/A
AD24	NC	NC	N/A
AD25	SXPVDD	Power	N/A
AD26	SXPVSS	Ground	N/A
AD27	$\overline{\text{SD\_F\_RX}}$	I	SXCVDD
AD28	SD_F_RX	I	SXCVDD
AE1	MDQS2	I/O	GVDD
AE2	VSS	Ground	N/A
AE3	MDQ18	I/O	GVDD
AE4	GVDD	Power	N/A
AE5	VSS	Ground	N/A
AE6	MDQ29	I/O	GVDD
AE7	GVDD	Power	N/A
AE8	VSS	Ground	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
B24	GPIO25/TMR2/RCW_SRC1	I/O	NVDD
F24	GPIO26/TMR3	I/O	NVDD
E24	GPIO27/TMR4/RCW_SRC0	I/O	NVDD
G19	GPIO28/UART_RXD/CP_LOS1	I/O	NVDD
A20	GPIO29/UART_TXD/CP_LOS2	I/O	NVDD
J28	GPIO3/DRQ1/$\overline{\text{IRQ3}}$/RC3	I/O	NVDD
C25	GPIO30/I2C_SCL	I/O	NVDD
A21	GPIO31/I2C_SDA	I/O	NVDD
K22	GPIO4/DDN1/$\overline{\text{IRQ4}}$/RC4	I/O	NVDD
D24	GPIO5/$\overline{\text{IRQ5}}$/RC5/CP_SYNC4	I/O	NVDD
F25	GPIO6/$\overline{\text{IRQ6}}$/RC6/CP_SYNC5	I/O	NVDD
K26	GPIO7/IRQ7/RC7/CP_SYNC6	I/O	NVDD
F28	GPIO8/$\overline{\text{IRQ8}}$/RC8	I/O	NVDD
J23	GPIO9/$\overline{\text{IRQ9}}$/RC9	I/O	NVDD
A4	GVDD	Power	N/A
A7	GVDD	Power	N/A
AA4	GVDD	Power	N/A
AA9	GVDD	Power	N/A
AC11	GVDD	Power	N/A
AC2	GVDD	Power	N/A
AC5	GVDD	Power	N/A
AC8	GVDD	Power	N/A
AE10	GVDD	Power	N/A
AE4	GVDD	Power	N/A
AE7	GVDD	Power	N/A
AG11	GVDD	Power	N/A
AG2	GVDD	Power	N/A
AG5	GVDD	Power	N/A
AG8	GVDD	Power	N/A
C2	GVDD	Power	N/A
C5	GVDD	Power	N/A
E4	GVDD	Power	N/A
E7	GVDD	Power	N/A
G2	GVDD	Power	N/A
G5	GVDD	Power	N/A
J4	GVDD	Power	N/A
L2	GVDD	Power	N/A
L5	GVDD	Power	N/A
N4	GVDD	Power	N/A
R2	GVDD	Power	N/A
R5	GVDD	Power	N/A
R7	GVDD	Power	N/A
T8	GVDD	Power	N/A
U4	GVDD	Power	N/A
U7	GVDD	Power	N/A
V8	GVDD	Power	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
M6	NC	Non-user	N/A
N21	NC	NC	N/A
N22	NC	NC	N/A
N3	NC	Non-user	N/A
P21	NC	NC	N/A
P23	NC	NC	N/A
P24	NC	NC	N/A
P3	NC	Non-user	N/A
P5	NC	Non-user	N/A
R21	NC	NC	N/A
R22	NC	NC	N/A
R23	NC	NC	N/A
R24	NC	NC	N/A
T21	NC	NC	N/A
T22	NC	Non-user	N/A
T23	NC	Non-user	N/A
T24	NC	NC	N/A
U21	NC	NC	N/A
U22	NC	NC	N/A
U23	NC	NC	N/A
U24	NC	NC	N/A
V21	NC	NC	N/A
V22	NC	NC	N/A
V23	NC	NC	N/A
V24	NC	NC	N/A
V25	NC	NC	N/A
V26	NC	NC	N/A
W21	NC	NC	N/A
W22	NC	NC	N/A
W23	NC	NC	N/A
W26	NC	NC	N/A
Y21	NC	NC	N/A
Y22	NC	NC	N/A
Y23	NC	NC	N/A
Y24	NC	NC	N/A
Y25	NC	NC	N/A
Y26	NC	NC	N/A
Y5	NC	Non-user	N/A
D15	$\overline{\text{NMI}}$	I	QVDD
F15	$\overline{\text{NMI\_OUT}}$/$\overline{\text{CP\_RX\_INT}}$	O	QVDD
D21	NVDD	Power	N/A
D25	NVDD	Power	N/A
E19	NVDD	Power	N/A
E23	NVDD	Power	N/A
G25	NVDD	Power	N/A
H20	NVDD	Power	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
H23	NVDD	Power	N/A
H27	NVDD	Power	N/A
J21	NVDD	Power	N/A
K25	NVDD	Power	N/A
L21	NVDD	Power	N/A
AH14	PLL0_AVDD	Power	N/A
AH15	PLL1_AVDD	Power	N/A
AH16	PLL2_AVDD	Power	N/A
C17	$\overline{\text{PORESET}}$	I	QVDD
G15	QVDD	Power	N/A
H14	QVDD	Power	N/A
J27	RC21	I	NVDD
J24	$\overline{\text{RCW\_LSEL0}}$/RC17	I/O	NVDD
K24	$\overline{\text{RCW\_LSEL1}}$/RC18	I/O	NVDD
J26	$\overline{\text{RCW\_LSEL2}}$/RC19	I/O	NVDD
J25	$\overline{\text{RCW\_LSEL3}}$/RC20	I/O	NVDD
M27	$\overline{\text{SD\_A\_RX}}$	I	SXCVDD
M28	SD_A_RX	I	SXCVDD
M23	SD_A_TX	O	SXPVDD
M24	$\overline{\text{SD\_A\_TX}}$	O	SXPVDD
P27	$\overline{\text{SD\_B\_RX}}$	I	SXCVDD
P28	SD_B_RX	I	SXCVDD
N25	SD_B_TX	O	SXPVDD
N26	$\overline{\text{SD\_B\_TX}}$	O	SXPVDD
T27	$\overline{\text{SD\_C\_RX}}$	I	SXCVDD
T28	SD_C_RX	I	SXCVDD
R25	SD_C_TX	O	SXPVDD
R26	$\overline{\text{SD\_C\_TX}}$	O	SXPVDD
V27	$\overline{\text{SD\_D\_RX}}$	I	SXCVDD
V28	SD_D_RX	I	SXCVDD
U25	SD_D_TX	O	SXPVDD
U26	$\overline{\text{SD\_D\_TX}}$	O	SXPVDD
AB27	$\overline{\text{SD\_E\_RX}}$	I	SXCVDD
AB28	SD_E_RX	I	SXCVDD
AA25	SD_E_TX	O	SXPVDD
AA26	$\overline{\text{SD\_E\_TX}}$	O	SXPVDD
AD27	$\overline{\text{SD\_F\_RX}}$	I	SXCVDD
AD28	SD_F_RX	I	SXCVDD
AC25	SD_F_TX	O	SXPVDD
AC26	$\overline{\text{SD\_F\_TX}}$	O	SXPVDD
AF27	$\overline{\text{SD\_G\_RX}}$	I	SXCVDD
AF28	SD_G_RX	I	SXCVDD
AE25	SD_G_TX	O	SXPVDD
AE26	$\overline{\text{SD\_G\_TX}}$	O	SXPVDD
AH27	$\overline{\text{SD\_H\_RX}}$	I	SXCVDD
AH28	SD_H_RX	I	SXCVDD

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
W27	SXCVSS	Ground	N/A
AB25	SXPVDD	Power	N/A
AD25	SXPVDD	Power	N/A
AE21	SXPVDD	Power	N/A
AE23	SXPVDD	Power	N/A
AF25	SXPVDD	Power	N/A
AH25	SXPVDD	Power	N/A
M25	SXPVDD	Power	N/A
N23	SXPVDD	Power	N/A
P25	SXPVDD	Power	N/A
T25	SXPVDD	Power	N/A
AB26	SXPVSS	Ground	N/A
AD26	SXPVSS	Ground	N/A
AF21	SXPVSS	Ground	N/A
AF23	SXPVSS	Ground	N/A
AF26	SXPVSS	Ground	N/A
AH26	SXPVSS	Ground	N/A
M26	SXPVSS	Ground	N/A
N24	SXPVSS	Ground	N/A
P26	SXPVSS	Ground	N/A
T26	SXPVSS	Ground	N/A
E17	TCK	I	QVDD
F17	TDI	I	QVDD
B14	TDO	O	QVDD
B15	TMS	I	QVDD
G17	$\overline{\text{TRST}}$	I	QVDD
F10	VDD	Power	N/A
F8	VDD	Power	N/A
G7	VDD	Power	N/A
G9	VDD	Power	N/A
H10	VDD	Power	N/A
H16	VDD	Power	N/A
H18	VDD	Power	N/A
H8	VDD	Power	N/A
J11	VDD	Power	N/A
J13	VDD	Power	N/A
J15	VDD	Power	N/A
J17	VDD	Power	N/A
J19	VDD	Power	N/A
J7	VDD	Power	N/A
J9	VDD	Power	N/A
K10	VDD	Power	N/A
K12	VDD	Power	N/A
K14	VDD	Power	N/A
K16	VDD	Power	N/A
K18	VDD	Power	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
U8	VSS	Ground	N/A
V11	VSS	Ground	N/A
V13	VSS	Ground	N/A
V15	VSS	Ground	N/A
V17	VSS	Ground	N/A
V19	VSS	Ground	N/A
V2	VSS	Ground	N/A
V7	VSS	Ground	N/A
V9	VSS	Ground	N/A
W1	VSS	Ground	N/A
W10	VSS	Ground	N/A
W12	VSS	Ground	N/A
W14	VSS	Ground	N/A
W16	VSS	Ground	N/A
W18	VSS	Ground	N/A
W2	VSS	Ground	N/A
W20	VSS	Ground	N/A
W4	VSS	Ground	N/A
W8	VSS	Ground	N/A
Y11	VSS	Ground	N/A
Y13	VSS	Ground	N/A
Y15	VSS	Ground	N/A
Y17	VSS	Ground	N/A
Y19	VSS	Ground	N/A
Y7	VSS	Ground	N/A
Y9	VSS	Ground	N/A
D27	VSS‘	Ground	N/A

Notes:
1. Signal function during power-on reset is determined by the RCW source type. Selection of RapidIO, SGMII, CPRI, and PCI Express functionality during normal operation is configured by the RCW bit values. Selection of the GPIO function and other functions is done by GPIO register setup. For signals with GPIO functionality, the open-drain and internal 20 KΩ pull-up resistor can be configured by GPIO register programming. For configuration details, see the *GPIO* chapter in the *MSC8157E Reference Manual*.
2. NC signals should be disconnected for compatibility with future revisions of the device. Non-user signals are reserved for manufacturing and test purposes only. The assigned signal name is used to indicate whether the signal must be unconnected (Reserved), pulled down (VSS or SXCVSS), or pulled up (VDD).
3. Pin types are: Ground = all VSS connections; Power = all VDD connections; I = Input; O = Output; I/O = Input/Output; NC = not connected; non-user = connect as specified under Signal Name.
4. Connect power inputs to the power supplies via external filters. See the *MSC8157 Design Checklist* (AN4110) for details.

Table 10. Differential Signal Definitions (continued)

Term	Definition
Differential Waveform	The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD\_[A–J]\_TX}}$, for example) from the non-inverting signal (SD_[A–J]_TX, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 3 as an example for differential waveform.
Common Mode Voltage, V_{cm}	The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SD\_[A–J]\_TX} + V_{\overline{SD\_[A–J]\_TX}}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and $\overline{\text{TD}}$. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output differential swing (V_{OD}) has the same amplitude as each signal single-ended swing. The differential output signal ranges between 500 mV and –500 mV. In other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

2.5.2.2 SerDes Reference Clock Receiver Characteristics

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clock inputs are SD_REF_CLK1/$\overline{\text{SD\_REF\_CLK1}}$ or SD_REF_CLK2/$\overline{\text{SD\_REF\_CLK2}}$. Figure 4 shows a receiver reference diagram of the SerDes reference clocks.

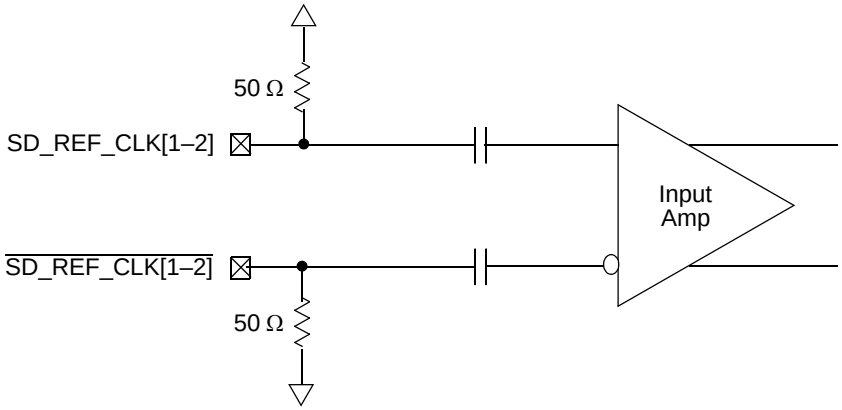


Figure 4. Receiver of SerDes Reference Clocks

The characteristics of the clock signals are as follows:

- The supply voltage requirements for V_{DDSXC} are as specified in **Table 4.**
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SD_REF_CLK[1–2] and $\overline{\text{SD\_REF\_CLK[1–2]}}$ are internally AC-coupled differential inputs as shown in Figure 4. Each differential clock input (SD_REF_CLK[1–2] or $\overline{\text{SD\_REF\_CLK[1–2]}}$ has on-chip 50-Ω termination to SXCVSS followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.

— To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK[1–2]}}$) through the same source impedance as the clock input (SD_REF_CLK[1–2]) in use.

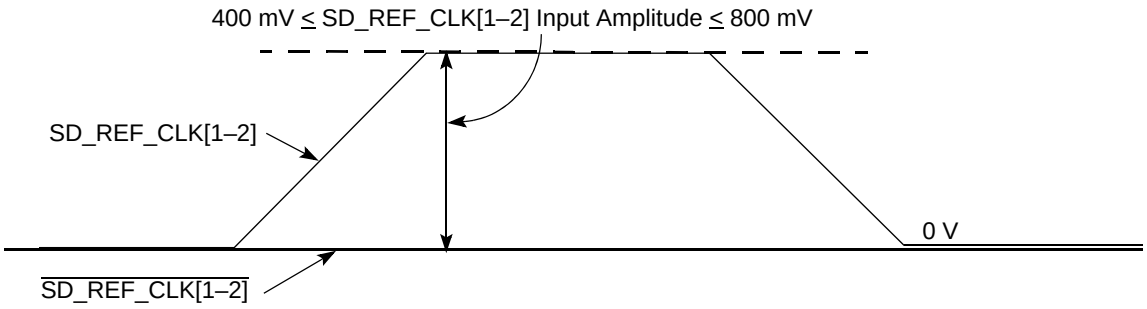


Figure 8. Single-Ended Reference Clock Input DC Requirements

2.5.3.2 DC-Level Requirements for PCI Express Configurations

The DC-level requirements for PCI Express implementations have separate requirements for the Tx and Rx lines. The MSC8157E supports a 2.5 Gbps and a 5 Gbps PCI Express interface defined by the *PCI Express Base Specification, Revision 2.0*. The transmitter specifications for 2.5 Gbps are defined in Table 11 and the receiver specifications are defined in Table 12. For 5 Gbps, the transmitter specifications are defined in Table 13 and the receiver specifications are defined in Table 14.

Note: Specifications are valid at the recommended operating conditions listed in Table 4.

Table 11. PCI Express (2.5 Gbps) Differential Transmitter (Tx) Output DC Specifications

Parameter	Symbol	Min	Nom	Max	Units	Condition
Differential peak-to-peak output voltage swing	$V_{TX\text{-}DIFFp\text{-}p}$	800	1000	1200	mV	$V_{TX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{TX\text{-}D+} - V_{TX\text{-}D-} \rvert$, Measured at the package pins with a test load of 50 Ω to GND on each pin.
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. Measured at the package pins with a test load of 50 Ω to GND on each pin.
DC differential Tx impedance	$Z_{TX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	Tx DC differential mode low Impedance
DC single-ended TX impedance	$Z_{TX\text{-}DC}$	40	50	60	Ω	Required Tx D+ as well as D– DC Impedance during all states

Table 12. PCI Express (2.5 Gbps) Differential Receiver (Rx) Input DC Specifications

Parameter	Symbol	Min	Nom	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX\text{-}DIFFp\text{-}p}$	120	1000	1200	mV	1
DC differential Input Impedance	$Z_{RX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	2
DC input impedance	$Z_{RX\text{-}DC}$	40	50	60	Ω	3
Powered down DC input impedance	$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	50	—	—	KΩ	4
Electrical idle detect threshold	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	65	—	175	mV	5

Table 14. PCI Express (5 Gbps) Differential Receiver (Rx) Input DC Specifications (continued)

Parameter	Symbol	Min	Nom	Max	Units	Notes

Notes:
1. $V_{RX\text{-}DIFFp\text{-}p} = 2 \times |V_{RX\text{-}D+} - V_{RX\text{-}D\text{-}}|$ Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Rx DC differential mode impedance. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
3. Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). Measured at the package pins with a test load of 50 Ω to GND on each pin. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
4. Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.
5. $V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2 \times |V_{RX\text{-}D+} - V_{RX\text{-}D\text{-}}|$. Measured at the package pins of the receiver

2.5.3.3 DC Level Requirements for Serial RapidIO Configurations

Note: Specifications are valid at the recommended operating conditions listed in Table 4.

Table 15. Serial RapidIO Transmitter DC Specifications for Transfer Rates ≤ 3.125 Gbaud

Parameter	Symbol	Min	Nom	Max	Units	Condition
Output voltage	V_O	–0.40	—	2.30	V	
Long run differential output voltage	V_{DIFFPP}	800	—	1600	mVp-p	L[A–J]TECR0[AMP_RED] = 0b000000
Short run differential output voltage	V_{DIFFPP}	500	—	1000	mVp-p	L[A–J]TECR0[AMP_RED] = 0b001000
DC differential TX impedance	ZTX-DIFF-DC	80	100	120	Ω	

Note: Voltage relative to COMMON of either signal comprising a differential pair.

Table 16. Serial RapidIO Receiver DC Specifications for Transfer Rates ≤ 3.125 Gbaud

Parameter	Symbol	Min	Nom	Max	Units
Differential input voltage	V_{IN}	200	—	1600	mVp-p
DC differential RX impedance	ZRX-DIFF-DC	80	100	120	Ω

Notes:
1. Voltage relative to COMMON of either signal comprising a differential pair.
2. Specifications are for Long and Short Run.

Table 17. Serial RapidIO Transmitter DC Specifications for Short Run at 5 Gbaud

Parameter	Symbol	Min	Nom	Max	Units	Condition
Output differential voltage (into floating load Rload = 100 Ω)	T_Vdiff	400	—	750	mV	Amplitude setting L[A–J]TECR0[AMP_RED] = 0b001101
Differential resistance	T_Rd	80	100	120	Ω	

Table 18. Serial RapidIO Receiver DC Specifications for Short Run at 5 Gbaud

Parameter	Symbol	Min	Nom	Max	Units
Input differential voltage	R_Vdiff	125	—	1200	mV
Differential resistance	R_Rdin	80		120	Ω

Table 19. Serial RapidIO Transmitter DC Specifications for Long Run at 5 Gbaud

Parameter	Symbol	Min	Nom	Max	Units	Conditions
Output differential voltage (into floating load Rload = 100 Ω)	T_Vdiff	800	—	1200	mV	Amplitude setting L[A–J]TECR0[AMP_RED] = 0b000000 (with de-emphasis disabled)

Table 30. DDR SDRAM Output AC Timing Specifications (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
MDQ/MECC/MDM output setup with respect to MDQS • 1333 MHz data rate • 1200 MHz data rate • 1066 MHz data rate • 800 MHz data rate • 667 MHz data rate	t_{DDKHDS}, t_{DDKLDS}	 250 275 300 375 450	 — — — — —	 ps ps ps ps ps	5, 6
MDQ/MECC/MDM output hold with respect to MDQS • 1333 MHz data rate • 1200 MHz data rate • 1066 MHz data rate • 800 MHz data rate • 667 MHz data rate	t_{DDKHDX}, t_{DDKLDX}	 250 275 300 375 450	 — — — — —	 ps ps ps ps ps	5
MDQS preamble	t_{DDKHMP}	$0.9 \times t_{MCK}$	—	ns	—
MDQS postamble	t_{DDKHME}	$0.4 \times t_{MCK}$	$0.6 \times t_{MCK}$	ns	—

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *MSC8157E Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MSC8157E.
6. At recommended operating conditions with V_{DDDDR} (1.5 V) ± 5%.

Note: For the ADDR/CMD setup and hold specifications in Table 30, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

Figure 10 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

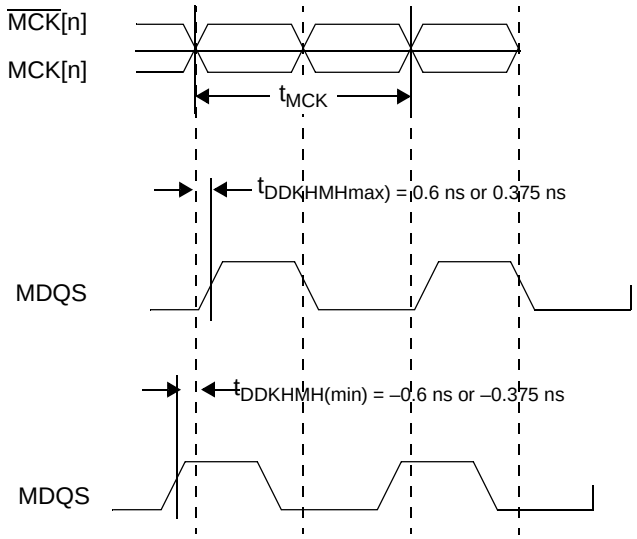


Figure 10. MCK to MDQS Timing

Figure 11 shows the DDR SDRAM output timing diagram.

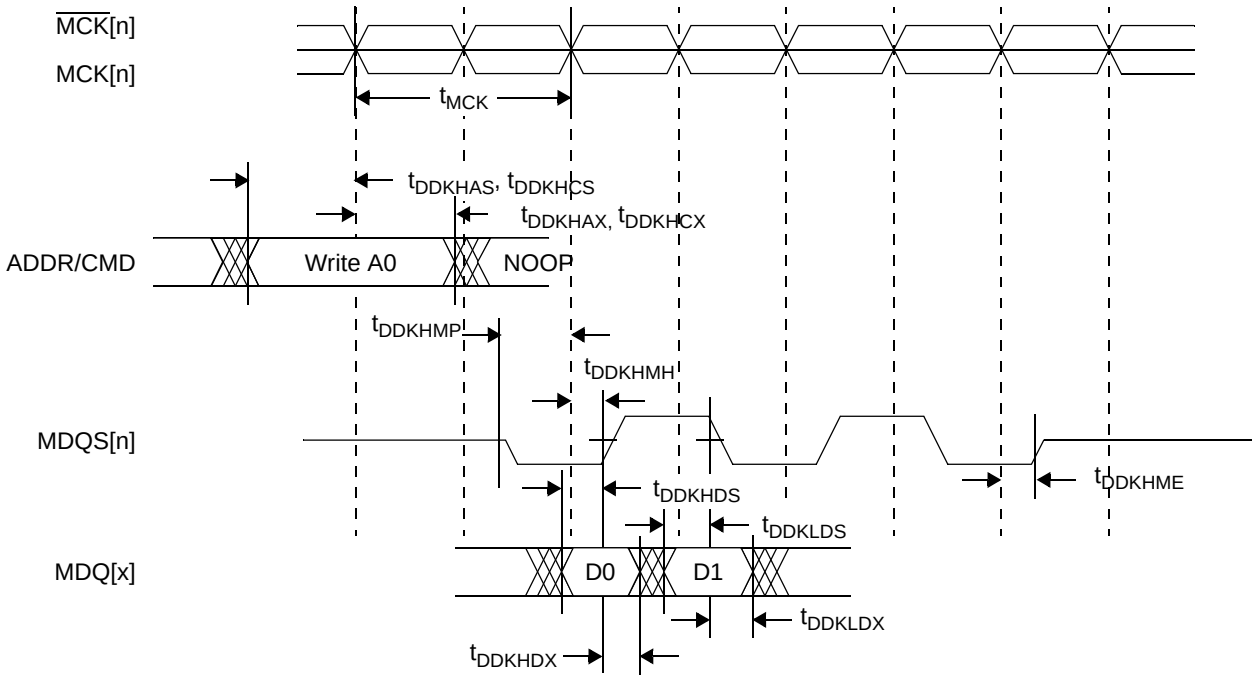


Figure 11. DDR SDRAM Output Timing

Figure 12 provides the AC test load for the DDR3 controller bus.

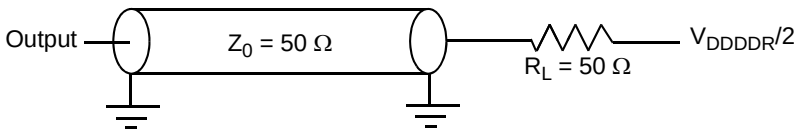


Figure 12. DDR3 Controller Bus AC Test Load

2.6.1.3 DDR3 SDRAM Differential Timing Specifications

This section describes the DC and AC differential timing specifications for the DDR3 SDRAM controller interface. Figure 13 shows the differential timing specification.

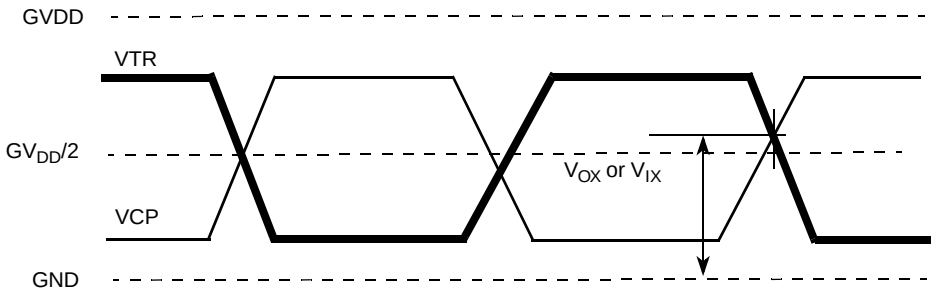


Figure 13. DDR3 SDRAM Differential Timing Specifications

Note: VTR specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as $\overline{\text{MCK}}$ or $\overline{\text{MDQS}}$).

Table 31 provides the DDR3 differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$.

Table 35. PCI Express 2.0 (5.0 Gbps) Differential Transmitter (Tx) Output AC Specifications

Parameter	Symbol	Min	Nom	Max	Units	Comments
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1.
Minimum Tx eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum Transmitter jitter can be derived as: $T_{TX-MAX-JITTER}$ = 1 – T_{TX-EYE} = 0.25 UI. See notes 2 and 3.
Tx RMS deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	—	—	0.15	ps	—
Tx RMS deterministic jitter < 1.5 MHz	$T_{TX-LF-RMS}$	—	3.0	—	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 4.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage test load as shown in Figure 16 and measured over any 250 consecutive Tx UIs.
3. A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-MAX-JITTER}$ = 0.25 UI for the Transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The DSP device SerDes transmitter does not have a built-in C_{TX}. An external AC coupling capacitor is required.

Table 36. PCI Express 2.0 (5.0 Gbps) Differential Receiver (Rx) Input AC Specifications

Parameter	Symbol	Min	Nom	Max	Units	Conditions
Unit Interval	UI	199.40	200.00	200.06	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Max Rx inherent timing error	$T_{RX-TJ-CC}$	—	—	0.4	UI	The maximum inherent total timing error for common REF_CLK Rx architecture
Maximum time between the jitter median and maximum deviation from the median	$T_{RX-TJ-DC}$	—	—	0.34	UI	Max Rx inherent total timing error
Max Rx inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	—	—	0.30	UI	The maximum inherent deterministic timing error for common REF_CLK Rx architecture
Max Rx inherent deterministic timing error	$T_{RX-DJ-DD-DC}$	—	—	0.24	UI	The maximum inherent deterministic timing error for common REF_CLK Rx architecture

Note: No test load is necessarily accosted with this value.

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in Figure 16.

Note: The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

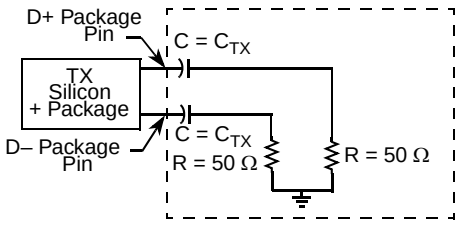


Figure 16. Test Measurement Load

2.6.2.4 Serial RapidIO AC Timing Specifications

Note: Specifications are valid at the recommended operating conditions listed in Table 4.

Table 37 defines the transmitter AC specifications for the Serial RapidIO interface at frequencies up to 3.125 Gbaud. The AC timing specifications do not include REF_CLK jitter.

Table 37. Serial RapidIO Transmitter AC Timing Specifications Up to 3.125 Gbaud

Characteristic	Symbol	Min	Nom	Max	Unit
Deterministic Jitter	J_D	—	—	0.17	UI p-p
Total Jitter	J_T	—	—	0.35	UI p-p
Unit Interval: 1.25 GBaud	UI	800 – 100ppm	800	800 + 100ppm	ps
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps

Table 38 defines the Receiver AC specifications for the Serial RapidIO interface at frequencies up to 3.125 Gbaud. The AC timing specifications do not include REF_CLK jitter.

Table 38. Serial RapidIO Receiver AC Timing Specifications Up to 3.125 Gbaud

Characteristic	Symbol	Min	Nom	Max	Unit	Notes
Deterministic Jitter Tolerance	J_D	—	—	0.37	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	J_{DR}	—	—	0.55	UI p-p	1
Total Jitter Tolerance	J_T	—	—	0.65	UI p-p	1, 2
Bit Error Rate	BER	—	—	10^{-12}	—	—
Unit Interval: 1.25 GBaud	UI	800 – 100ppm	800	800 + 100ppm	ps	—
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps	—

Notes:
1. Measured at receiver.
2. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 17. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 39 defines the short run transmitter AC specifications for the Serial RapidIO interface at 5 Gbaud. The AC timing specifications do not include REF_CLK jitter.

Table 39. Serial RapidIO Short Run Transmitter AC Timing Specifications at 5.0 Gbaud

Characteristic	Symbol	Min	Nom	Max	Unit
Uncorrelated High Probability Jitter	T_UHPJ	—	—	0.15	UI p-p
Total Jitter	T_TJ	—	—	0.30	UI p-p
Baud Rate	UI	5.000 – 100ppm	5.000	5.000 + 100ppm	Gbaud

Table 40 defines the short run Receiver AC specifications for the Serial RapidIO interface at 5 Gbaud. The AC timing specifications do not include REF_CLK jitter.

Table 40. Serial RapidIO Short Run Receiver AC Timing Specifications at 5 Gbaud

Characteristic	Symbol	Min	Nom	Max	Unit
Rx Baud Rate	R_Baud	5.000 – 100ppm	5.000	5.000 + 100ppm	Gbaud
Uncorrelated Bounded High Probability Jitter	R_UBHPJ	—	—	0.15	UIp-p
Correlated Bounded High Probability Jitter	R_CBHPJ	—	—	0.3	UIp-p
Bounded High Probability Jitter	R_BHPJ	—	—	0.45	UIp-p
Sinusoidal Jitter maximum	R_SJ-max	—	—	5	UIp-p
Sinusoidal Jitter, High Frequency	R_SJ-hf	—	—	0.05	UIp-p

Note: The intended application is a point-to-point interface up to two connectors. The maximum allowed total loss (channel + interconnects + other loss) is 20.4 dB @ 6.144 Gbps.

2.6.2.6 SGMII AC Timing Specifications

Note: Specifications are valid at the recommended operating conditions listed in Table 4.

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_[A–J]_TX and $\overline{\text{SD\_[A–J]\_TX}}$) or at the receiver inputs (SD_[A–J]_RX and $\overline{\text{SD\_[A–J]\_RX}}$) as depicted in Figure 19, respectively.

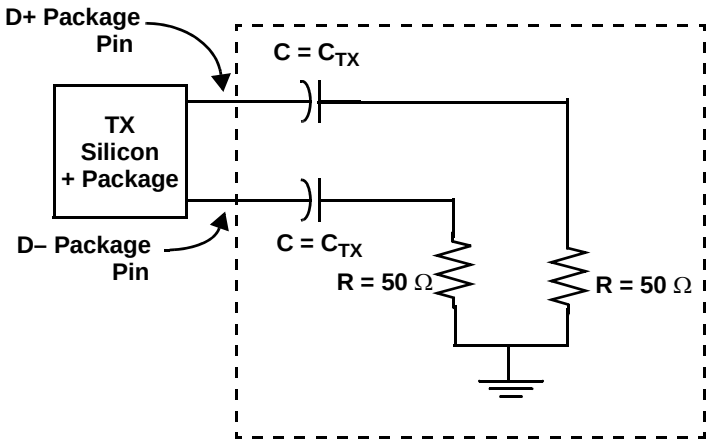


Figure 19. SGMII AC Test/Measurement Load

Table 47 provides the SGMII transmit AC timing specifications. The AC timing specifications do not include REF_CLK jitter.

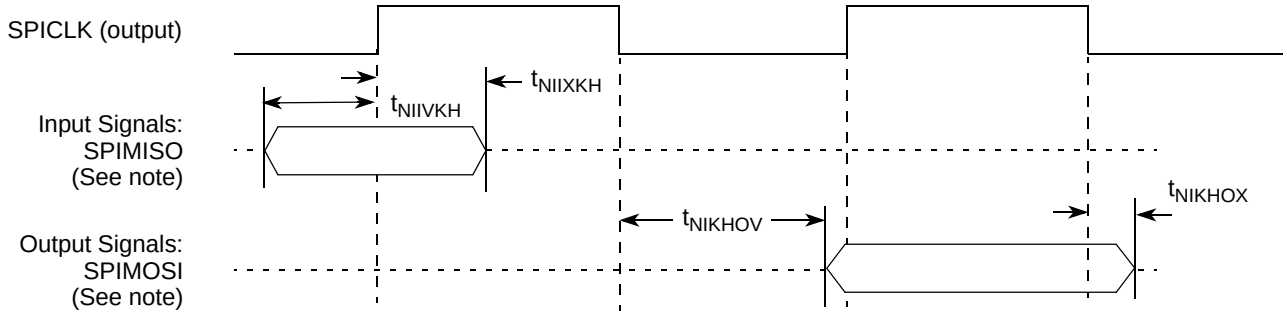
Table 47. SGMII Transmit AC Timing Specifications

Parameter	Symbol	Min	Nom	Max	Unit	Condition
Unit interval	UI	800 – 100ppm	800	800 + 100ppm	pS	± 100ppm
Deterministic jitter	JD	—	—	0.17	UI p-p	—
Total jitter	JT	—	—	0.35	UI p-p	—
AC coupling capacitor	CTX	75	—	200	nF	All transmitters must be AC-coupled
Note: The AC specifications do not include REF_CLK jitter.						

Table 48 provides the SGMII receiver AC timing specifications. The AC timing specifications do not include REF_CLK jitter.

Table 48. SGMII Receive AC Timing Specifications

Parameter	Symbol	Min	Nom	Max	Unit	Condition
Unit interval	UI	800 – 100ppm	800	800 + 100ppm	pS	± 100ppm
Deterministic jitter tolerance	JD	—	—	0.37	UI p-p	Measured at receiver.
Combined deterministic and random jitter tolerance	JDR	—	—	0.55	UI p-p	Measured at receiver
Total jitter tolerance	JT	—	—	0.65	UI p-p	Measured at receiver
Bit error ratio	BER	—	—	10^{-12}	—	—
Note: The AC specifications do not include REF_CLK jitter. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region shown in Figure 20 or Figure 21.						



Note: measured with SPMODE[CI] = 0, SPMODE[CP] = 0

Figure 27. SPI AC Timing in Master Mode (Internal Clock)

2.6.6 Asynchronous Signal Timing

Table 53 lists the asynchronous signal timing specifications.

Table 53. Signal Timing

Characteristics	Symbol	Type	Min
Input	t_{IN}	Asynchronous	One CLKIN/MCLKIN cycle
Output	t_{OUT}	Asynchronous	Application dependent
Note: Input value relevant for EE0, $\overline{\text{IRQ}}$[15–0], and $\overline{\text{NMI}}$ only.			

The following interfaces use the specified asynchronous signals:

- *GPIO*. Signals GPIO[31–0], when used as GPIO signals, that is, when the alternate multiplexed special functions are not selected.

Note: When used as a general purpose input (GPI), the input signal should be driven until it is acknowledged by the MSC8157E device, that is, when the expected input value is read from the GPIO data register.

- *EE port.* Signals EE0, EE1.
- *Boot function*. Signal STOP_BS.
- *I^2C interface*. Signals I2C_SCL and I2C_SDA.
- *Interrupt inputs*. Signals $\overline{\text{IRQ}}$[15–0] and $\overline{\text{NMI}}$.
- *Interrupt outputs*. Signals $\overline{\text{INT\_OUT}}$/$\overline{\text{CP\_TX\_INT}}$ and $\overline{\text{NMI\_OUT}}$/$\overline{\text{CP\_RX\_INT}}$ (minimum pulse width is 32 ns).

2.6.7 JTAG Signals

Table 54. JTAG Timing

Characteristics	Symbol	All frequencies		Unit
		Min	Max	
TCK cycle time	t_{TCKX}	36.0	—	ns
TCK clock high phase measured at $V_M = V_{DDIO}/2$	t_{TCKH}	15.0	—	ns
Boundary scan input data setup time	t_{BSVKH}	0.0	—	ns
Boundary scan input data hold time	t_{BSXKH}	15.0	—	ns
TCK fall to output data valid	t_{TCKHOV}	—	20.0	ns
TCK fall to output high impedance	t_{TCKHOZ}	—	24.0	ns
TMS, TDI data setup time	t_{TDIVKH}	5.0	—	ns
TMS, TDI data hold time	t_{TDIXKH}	5.0	—	ns
TCK fall to TDO data valid	t_{TDOHOV}	—	10.0	ns
TCK fall to TDO high impedance	t_{TDOHOZ}	—	12.0	ns
$\overline{TRST}$ assert time	t_{TRST}	100.0	—	ns
Note: All timings apply to OnCE module data transfers as well as any other transfers via the JTAG port.				

Figure 28 shows the Test Clock Input Timing Diagram

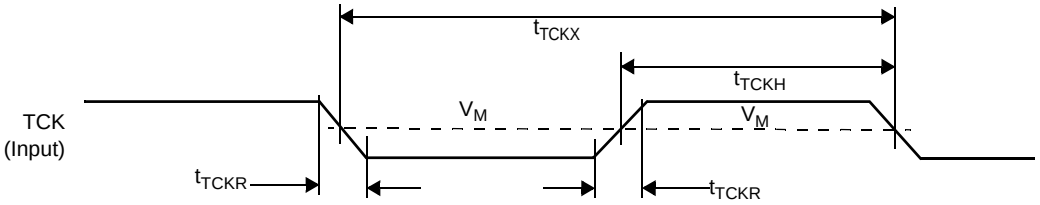


Figure 28. Test Clock Input Timing

Figure 29 shows the boundary scan (JTAG) timing diagram.

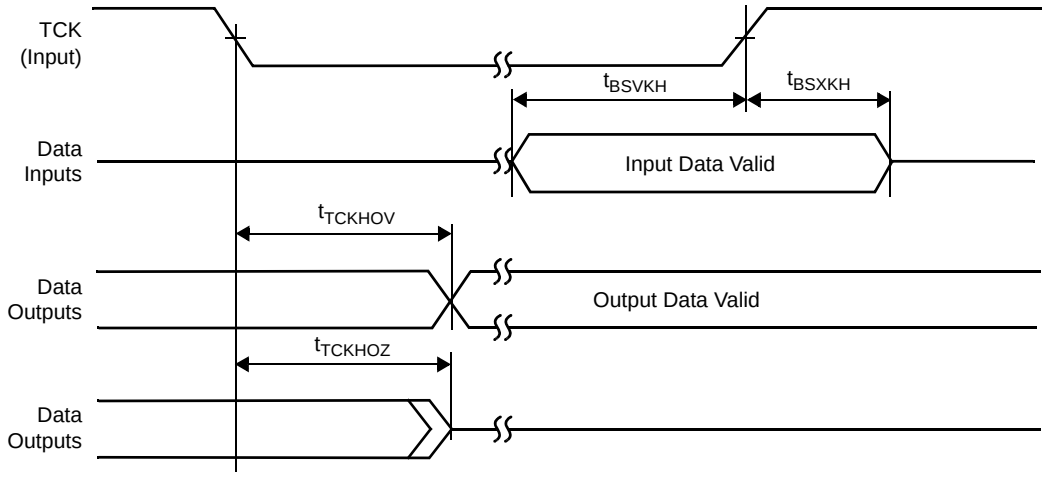


Figure 29. Boundary Scan (JTAG) Timing

6 Product Documentation

Following is a general list of supporting documentation:

- *MSC8157E Technical Data Sheet* (MSC8157E). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8157E device.
- *MSC8157E Reference Manual* (MSC8157ERM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes*. Cover various programming topics related to the StarCore DSP core and the MSC8157E device.
- *QUICC Engine Block Reference Manual with Protocol Interworking* (QEIWRM). Provides detailed information regarding the QUICC Engine technology including functional description, registers, and programming information.
- *SC3850 DSP Core Reference Manual*. Covers the SC3850 core architecture, control registers, clock registers, program control, and instruction set.
- *MSC8156SC3850 DSP Core Subsystem Reference Manual*. Covers core subsystem architecture, functionality, and registers.

7 Revision History

This table provides a revision history for this data sheet.

Table 55. Document Revision History

Revision	Date	Description
2	12/2013	Updated Section 4, “Ordering Information.”
1	10/2013	Updated Section 4, “Ordering Information.”
0	11/2011	Initial public release