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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	SC3850 Six Core
Interface	Ethernet, I²C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	6.375MB
Voltage - I/O	1.00V, 1.50V, 2.50V
Voltage - Core	1.00V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=msc8157etvt1000a

Table of Contents

List of Figures

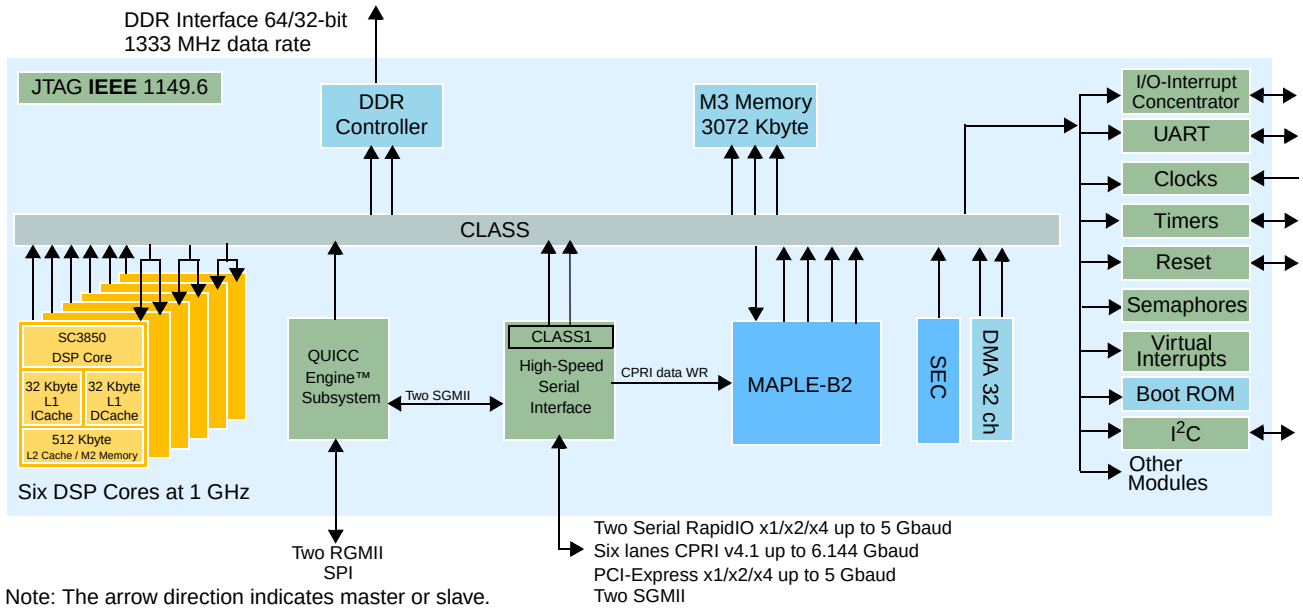


Figure 1. MSC8157E Block Diagram

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
U3	MCK1	O	GVDD
U4	GVDD	Power	N/A
U5	VSS	Ground	N/A
U6	MBA1	O	GVDD
U7	GVDD	Power	N/A
U8	VSS	Ground	N/A
U9	VDD	Power	N/A
U10	VSS	Ground	N/A
U11	VDD	Power	N/A
U12	VSS	Ground	N/A
U13	VDD	Power	N/A
U14	VSS	Ground	N/A
U15	VDD	Power	N/A
U16	VSS	Ground	N/A
U17	VDD	Power	N/A
U18	VSS	Ground	N/A
U19	VDD	Power	N/A
U20	VSS	Ground	N/A
U21	NC	NC	N/A
U22	NC	NC	N/A
U23	NC	NC	N/A
U24	NC	NC	N/A
U25	SD_D_TX	O	SXPVDD
U26	$\overline{\text{SD\_D\_TX}}$	O	SXPVDD
U27	SXCVSS	Ground	N/A
U28	SXCVDD	Power	N/A
V1	MVREF	Power	N/A
V2	VSS	Ground	N/A
V3	MA8	O	GVDD
V4	MA2	O	GVDD
V5	MA6	O	GVDD
V6	MCKE1	O	GVDD
V7	VSS	Ground	N/A
V8	GVDD	Power	N/A
V9	VSS	Ground	N/A
V10	VDD	Power	N/A
V11	VSS	Ground	N/A
V12	VDD	Power	N/A
V13	VSS	Ground	N/A
V14	VDD	Power	N/A
V15	VSS	Ground	N/A
V16	VDD	Power	N/A
V17	VSS	Ground	N/A
V18	VDD	Power	N/A
V19	VSS	Ground	N/A
V20	VDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
V21	NC	NC	N/A
V22	NC	NC	N/A
V23	NC	NC	N/A
V24	NC	NC	N/A
V25	NC	NC	N/A
V26	NC	NC	N/A
V27	$\overline{\text{SD\_D\_RX}}$	I	SXCVDD
V28	SD_D_RX	I	SXCVDD
W1	VSS	Ground	N/A
W2	VSS	Ground	N/A
W3	MA5	O	GVDD
W4	VSS	Ground	N/A
W5	GVDD	Power	N/A
W6	MMDIC1	I/O	GVDD
W7	GVDD	Power	N/A
W8	VSS	Ground	N/A
W9	VDD	Power	N/A
W10	VSS	Ground	N/A
W11	M3VDD	Power	N/A
W12	VSS	Ground	N/A
W13	M3VDD	Power	N/A
W14	VSS	Ground	N/A
W15	M3VDD	Power	N/A
W16	VSS	Ground	N/A
W17	CPRIVDD	Power	N/A
W18	VSS	Ground	N/A
W19	VDD	Power	N/A
W20	VSS	Ground	N/A
W21	NC	NC	N/A
W22	NC	NC	N/A
W23	NC	NC	N/A
W24	SD_PLL1_AVDD	Power	N/A
W25	SD_PLL1_AGND	Ground	N/A
W26	NC	NC	N/A
W27	SXCVSS	Ground	N/A
W28	SXCVDD	Power	N/A
Y1	MA11	O	GVDD
Y2	MA9	O	GVDD
Y3	MA12	O	GVDD
Y4	MA7	O	GVDD
Y5	NC	Non-user	N/A
Y6	MMDIC0	I/O	GVDD
Y7	VSS	Ground	N/A
Y8	GVDD	Power	N/A
Y9	VSS	Ground	N/A
Y10	VDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
AC19	NC	NC	N/A
AC20	NC	Non-user	N/A
AC21	NC	NC	N/A
AC22	NC	NC	N/A
AC23	NC	NC	N/A
AC24	NC	NC	N/A
AC25	SD_F_TX	O	SXPVDD
AC26	$\overline{\text{SD\_F\_TX}}$	O	SXPVDD
AC27	SXCVSS	Ground	N/A
AC28	SXCVDD	Power	N/A
AD1	MECC7	I/O	GVDD
AD2	MECC6	I/O	GVDD
AD3	MECC0	I/O	GVDD
AD4	MECC5	I/O	GVDD
AD5	MECC3	I/O	GVDD
AD6	MDQ24	I/O	GVDD
AD7	MDM0	O	GVDD
AD8	$\overline{\text{MDQS0}}$	I/O	GVDD
AD9	MDQS0	I/O	GVDD
AD10	MDQ4	I/O	GVDD
AD11	MDQ6	I/O	GVDD
AD12	VSS	Non-user	N/A
AD13	VSS	Non-user	N/A
AD14	VSS	Non-user	N/A
AD15	VSS	Ground	N/A
AD16	VSS	Ground	N/A
AD17	NC	NC	N/A
AD18	SD_PLL2_AVDD	Power	N/A
AD19	NC	NC	N/A
AD20	NC	NC	N/A
AD21	NC	NC	N/A
AD22	NC	NC	N/A
AD23	NC	NC	N/A
AD24	NC	NC	N/A
AD25	SXPVDD	Power	N/A
AD26	SXPVSS	Ground	N/A
AD27	$\overline{\text{SD\_F\_RX}}$	I	SXCVDD
AD28	SD_F_RX	I	SXCVDD
AE1	MDQS2	I/O	GVDD
AE2	VSS	Ground	N/A
AE3	MDQ18	I/O	GVDD
AE4	GVDD	Power	N/A
AE5	VSS	Ground	N/A
AE6	MDQ29	I/O	GVDD
AE7	GVDD	Power	N/A
AE8	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
AE9	MDQ5	I/O	GVDD
AE10	GVDD	Power	N/A
AE11	VSS	Ground	N/A
AE12	MDQ9	I/O	GVDD
AE13	VSS	Non-user	N/A
AE14	VSS	Ground	N/A
AE15	VSS	Ground	N/A
AE16	VSS	Ground	N/A
AE17	NC	NC	N/A
AE18	SD_PLL_AGND	Ground	N/A
AE19	NC	NC	N/A
AE20	SD_J_TX	O	SXPVDD
AE21	SXPVDD	Power	N/A
AE22	SD_I_TX	O	SXPVDD
AE23	SXPVDD	Power	N/A
AE24	NC	NC	N/A
AE25	SD_G_TX	O	SXPVDD
AE26	$\overline{\text{SD\_G\_TX}}$	O	SXPVDD
AE27	SXCVSS	Ground	N/A
AE28	SXCVDD	Power	N/A
AF1	$\overline{\text{MDQS2}}$	I/O	GVDD
AF2	MDQ17	I/O	GVDD
AF3	MDQ21	I/O	GVDD
AF4	MDQ16	I/O	GVDD
AF5	MDQ30	I/O	GVDD
AF6	MDQ27	I/O	GVDD
AF7	MDQ28	I/O	GVDD
AF8	MDQ7	I/O	GVDD
AF9	MDQ14	I/O	GVDD
AF10	MDQ11	I/O	GVDD
AF11	MDQ8	I/O	GVDD
AF12	MDQ10	I/O	GVDD
AF13	VSS	Non-user	N/A
AF14	VSS	Ground	N/A
AF15	VSS	Ground	N/A
AF16	VSS	Ground	N/A
AF17	NC	NC	N/A
AF18	NC	NC	N/A
AF19	NC	NC	N/A
AF20	$\overline{\text{SD\_J\_TX}}$	O	SXPVDD
AF21	SXPVSS	Ground	N/A
AF22	$\overline{\text{SD\_I\_TX}}$	O	SXPVDD
AF23	SXPVSS	Ground	N/A
AF24	NC	NC	N/A
AF25	SXPVDD	Power	N/A
AF26	SXPVSS	Ground	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
B4	MDQS7	I/O	GVDD
AA1	MDQS8	I/O	GVDD
AB1	$\overline{\text{MDQS8}}$	I/O	GVDD
AD3	MECC0	I/O	GVDD
AB4	MECC1	I/O	GVDD
AB3	MECC2	I/O	GVDD
AD5	MECC3	I/O	GVDD
AC3	MECC4	I/O	GVDD
AD4	MECC5	I/O	GVDD
AD2	MECC6	I/O	GVDD
AD1	MECC7	I/O	GVDD
Y6	MMDIC0	I/O	GVDD
W6	MMDIC1	I/O	GVDD
P6	MODT0	O	GVDD
N6	MODT1	O	GVDD
N1	$\overline{\text{MRAS}}$	O	GVDD
V1	MVREF	Power	N/A
M4	$\overline{\text{MWE}}$	O	GVDD
A10	NC	Non-user	N/A
A11	NC	Non-user	N/A
A12	NC	Non-user	N/A
A8	NC	Non-user	N/A
A9	NC	Non-user	N/A
AA20	NC	NC	N/A
AA22	NC	NC	N/A
AA23	NC	NC	N/A
AA24	NC	NC	N/A
AB19	NC	NC	N/A
AB20	NC	Non-user	N/A
AB21	NC	NC	N/A
AB22	NC	NC	N/A
AB23	NC	NC	N/A
AB24	NC	NC	N/A
AB5	NC	Non-user	N/A
AC17	NC	NC	N/A
AC18	NC	NC	N/A
AC19	NC	NC	N/A
AC20	NC	Non-user	N/A
AC21	NC	NC	N/A
AC22	NC	NC	N/A
AC23	NC	NC	N/A
AC24	NC	NC	N/A
AD17	NC	NC	N/A
AD19	NC	NC	N/A
AD20	NC	NC	N/A
AD21	NC	NC	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
AD22	NC	NC	N/A
AD23	NC	NC	N/A
AD24	NC	NC	N/A
AE17	NC	NC	N/A
AE19	NC	NC	N/A
AE24	NC	NC	N/A
AF17	NC	NC	N/A
AF18	NC	NC	N/A
AF19	NC	NC	N/A
AF24	NC	NC	N/A
AG17	NC	NC	N/A
AH17	NC	NC	N/A
B10	NC	Non-user	N/A
B12	NC	Non-user	N/A
B8	NC	Non-user	N/A
C10	NC	Non-user	N/A
C11	NC	Non-user	N/A
C12	NC	Non-user	N/A
C13	NC	Non-user	N/A
C15	NC	Non-user	N/A
C8	NC	Non-user	N/A
C9	NC	Non-user	N/A
D10	NC	Non-user	N/A
D12	NC	Non-user	N/A
D14	NC	Non-user	N/A
D8	NC	Non-user	N/A
E10	NC	Non-user	N/A
E11	NC	Non-user	N/A
E12	NC	Non-user	N/A
E13	NC	Non-user	N/A
E14	NC	Non-user	N/A
E9	NC	Non-user	N/A
F11	NC	Non-user	N/A
F12	NC	Non-user	N/A
F14	NC	Non-user	N/A
G11	NC	Non-user	N/A
G12	NC	Non-user	N/A
G13	NC	Non-user	N/A
G14	NC	Non-user	N/A
H13	NC	Non-user	N/A
L22	NC	NC	N/A
L23	NC	NC	N/A
L3	NC	Non-user	N/A
M21	NC	NC	N/A
M22	NC	NC	N/A
M5	NC	Non-user	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
V18	VDD	Power	N/A
V20	VDD	Power	N/A
W19	VDD	Power	N/A
W9	VDD	Power	N/A
Y10	VDD	Power	N/A
Y20	VDD	Power	N/A
A15	VSS	Ground	N/A
A17	VSS	Ground	N/A
A19	VSS	Ground	N/A
A2	VSS	Ground	N/A
A5	VSS	Ground	N/A
AA10	VSS	Ground	N/A
AA12	VSS	Ground	N/A
AA14	VSS	Ground	N/A
AA16	VSS	Ground	N/A
AA18	VSS	Ground	N/A
AA2	VSS	Ground	N/A
AA5	VSS	Ground	N/A
AA8	VSS	Ground	N/A
AB11	VSS	Ground	N/A
AB13	VSS	Ground	N/A
AB15	VSS	Ground	N/A
AB17	VSS	Ground	N/A
AC1	VSS	Ground	N/A
AC10	VSS	Ground	N/A
AC12	VSS	Ground	N/A
AC14	VSS	Ground	N/A
AC16	VSS	Ground	N/A
AC4	VSS	Ground	N/A
AC7	VSS	Ground	N/A
AD12	VSS	Non-user	N/A
AD13	VSS	Non-user	N/A
AD14	VSS	Non-user	N/A
AD15	VSS	Ground	N/A
AD16	VSS	Ground	N/A
AE11	VSS	Ground	N/A
AE13	VSS	Non-user	N/A
AE14	VSS	Ground	N/A
AE15	VSS	Ground	N/A
AE16	VSS	Ground	N/A
AE2	VSS	Ground	N/A
AE5	VSS	Ground	N/A
AE8	VSS	Ground	N/A
AF13	VSS	Non-user	N/A
AF14	VSS	Ground	N/A
AF15	VSS	Ground	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
M15	VSS	Ground	N/A
M17	VSS	Ground	N/A
M19	VSS	Ground	N/A
M7	VSS	Ground	N/A
M9	VSS	Ground	N/A
N10	VSS	Ground	N/A
N12	VSS	Ground	N/A
N14	VSS	Ground	N/A
N16	VSS	Ground	N/A
N18	VSS	Ground	N/A
N2	VSS	Ground	N/A
N20	VSS	Ground	N/A
N5	VSS	Ground	N/A
N8	VSS	Ground	N/A
P11	VSS	Ground	N/A
P13	VSS	Ground	N/A
P15	VSS	Ground	N/A
P17	VSS	Ground	N/A
P19	VSS	Ground	N/A
P7	VSS	Ground	N/A
P9	VSS	Ground	N/A
R10	VSS	Ground	N/A
R12	VSS	Ground	N/A
R14	VSS	Ground	N/A
R16	VSS	Ground	N/A
R18	VSS	Ground	N/A
R20	VSS	Ground	N/A
R4	VSS	Ground	N/A
R8	VSS	Ground	N/A
T1	VSS	Ground	N/A
T11	VSS	Ground	N/A
T13	VSS	Ground	N/A
T15	VSS	Ground	N/A
T17	VSS	Ground	N/A
T19	VSS	Ground	N/A
T2	VSS	Ground	N/A
T7	VSS	Ground	N/A
T9	VSS	Ground	N/A
U10	VSS	Ground	N/A
U12	VSS	Ground	N/A
U14	VSS	Ground	N/A
U16	VSS	Ground	N/A
U18	VSS	Ground	N/A
U2	VSS	Ground	N/A
U20	VSS	Ground	N/A
U5	VSS	Ground	N/A

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8157E Reference Manual*.

2.1 Maximum Ratings

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device with a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 3 describes the maximum electrical ratings for the MSC8157E.

Table 3. Absolute Maximum Ratings

Rating	Power Rail Name	Symbol	Value	Unit
Core supply voltage • Cores 0–5	VDD	V_{DD}	–0.3 to 1.1	V
PLL supply voltage[3]	PLL0_AVDD PLL1_AVDD PLL2_AVDD MAVDD SD_PLL1_AVDD SD_PLL2_AVDD	V_{DDPLL0} V_{DDPLL1} V_{DDPLL2} V_{DDPLLM} V_{DDPLL} V_{DDPLL}	–0.3 to 1.1 –0.3 to 1.1 –0.3 to 1.1 –0.3 to 1.1 –0.3 to 1.1 –0.3 to 1.1	V V V V V V
CRPE supply voltage CPRI supply voltage	CRPEVDD CPRIVDD	V_{DDCRPE} V_{DDCPRI}	–0.3 to 1.1 –0.3 to 1.1	V V
M3 memory supply voltage	M3VDD	V_{DDM3}	–0.3 to 1.1	V
DDR memory supply voltage	GVDD	V_{DDDDR}	–0.3 to 1.65	V
DDR reference voltage	MVREF	MV_{REF}	–0.3 to 0.51 × V_{DDDDR}	V
Input DDR voltage		V_{INDDR}	–0.3 to V_{DDDDR} + 0.3	V
I/O voltage excluding DDR and RapidIO lines	NVDD, QVDD	V_{DDIO}	–0.3 to 2.625	V
Input I/O voltage		V_{INIO}	–0.3 to V_{DDIO} + 0.3	V
SerDes pad voltage	SXPVDD	V_{DDSXP}	–0.3 to 1.65	V
SerDes core voltage	SXCVDD	V_{DDSXC}	–0.3 to 1.21	V
SerDes PLL voltage[3]		$V_{DDRIOPLL}$	–0.3 to 1.21	V
Input SerDes I/O voltage		V_{INRIO}	–0.4 to V_{DDSXC} + 0.3	V
Operating temperature		T_J	–40 to 105	°C
Storage temperature range		T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in Table 4.
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. PLL supply voltage is specified at input of the filter and not at pin of the MSC8157E (see the *MSC8157 Design Checklist* (AN4110)).

2.5.3.1 DC-Level Requirements for SerDes Reference Clocks

The DC-level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. Figure 6 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

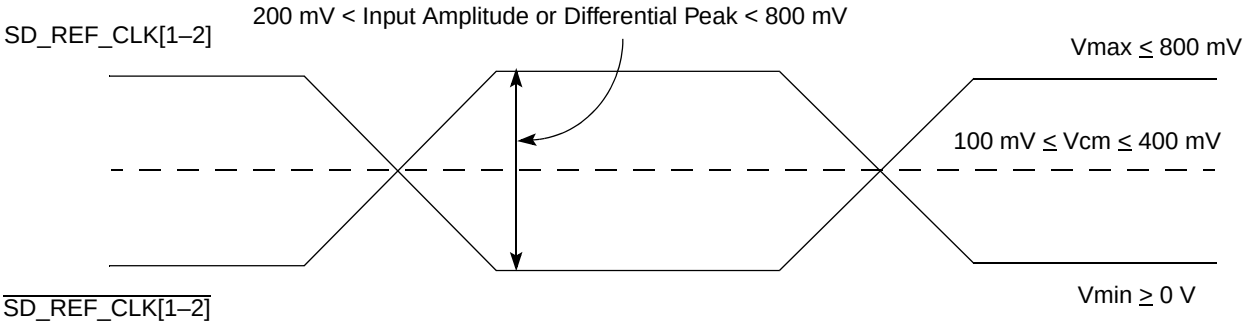


Figure 6. Differential Reference Clock Input DC Requirements (External DC-Coupled)

  - For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC-level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to GND_{SXC}. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage GND_{SXC}. Figure 7 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

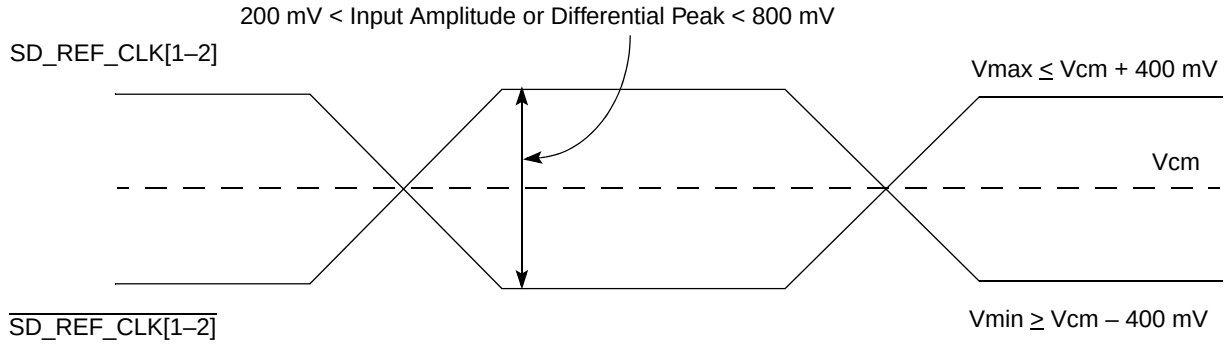


Figure 7. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- Single-Ended Mode
  - The reference clock can also be single-ended. The SD_REF_CLK[1–2] input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with $\overline{\text{SD\_REF\_CLK[1–2]}}$ either left unconnected or tied to ground.
  - The SD_REF_CLK[1–2] input average voltage must be between 200 and 400 mV. Figure 8 shows the SerDes reference clock input requirement for single-ended signaling mode.

Table 14. PCI Express (5 Gbps) Differential Receiver (Rx) Input DC Specifications (continued)

Parameter	Symbol	Min	Nom	Max	Units	Notes

Notes:
1. $V_{RX\text{-}DIFFp\text{-}p} = 2 \times |V_{RX\text{-}D+} - V_{RX\text{-}D\text{-}}|$ Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Rx DC differential mode impedance. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
3. Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). Measured at the package pins with a test load of 50 Ω to GND on each pin. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
4. Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.
5. $V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2 \times |V_{RX\text{-}D+} - V_{RX\text{-}D\text{-}}|$. Measured at the package pins of the receiver

2.5.3.3 DC Level Requirements for Serial RapidIO Configurations

Note: Specifications are valid at the recommended operating conditions listed in Table 4.

Table 15. Serial RapidIO Transmitter DC Specifications for Transfer Rates ≤ 3.125 Gbaud

Parameter	Symbol	Min	Nom	Max	Units	Condition
Output voltage	V_O	–0.40	—	2.30	V	
Long run differential output voltage	V_{DIFFPP}	800	—	1600	mVp-p	L[A–J]TECR0[AMP_RED] = 0b000000
Short run differential output voltage	V_{DIFFPP}	500	—	1000	mVp-p	L[A–J]TECR0[AMP_RED] = 0b001000
DC differential TX impedance	ZTX-DIFF-DC	80	100	120	Ω	

Note: Voltage relative to COMMON of either signal comprising a differential pair.

Table 16. Serial RapidIO Receiver DC Specifications for Transfer Rates ≤ 3.125 Gbaud

Parameter	Symbol	Min	Nom	Max	Units
Differential input voltage	V_{IN}	200	—	1600	mVp-p
DC differential RX impedance	ZRX-DIFF-DC	80	100	120	Ω

Notes:
1. Voltage relative to COMMON of either signal comprising a differential pair.
2. Specifications are for Long and Short Run.

Table 17. Serial RapidIO Transmitter DC Specifications for Short Run at 5 Gbaud

Parameter	Symbol	Min	Nom	Max	Units	Condition
Output differential voltage (into floating load Rload = 100 Ω)	T_Vdiff	400	—	750	mV	Amplitude setting L[A–J]TECR0[AMP_RED] = 0b001101
Differential resistance	T_Rd	80	100	120	Ω	

Table 18. Serial RapidIO Receiver DC Specifications for Short Run at 5 Gbaud

Parameter	Symbol	Min	Nom	Max	Units
Input differential voltage	R_Vdiff	125	—	1200	mV
Differential resistance	R_Rdin	80		120	Ω

Table 19. Serial RapidIO Transmitter DC Specifications for Long Run at 5 Gbaud

Parameter	Symbol	Min	Nom	Max	Units	Conditions
Output differential voltage (into floating load Rload = 100 Ω)	T_Vdiff	800	—	1200	mV	Amplitude setting L[A–J]TECR0[AMP_RED] = 0b000000 (with de-emphasis disabled)

Figure 9 shows the DDR3 SDRAM interface input timing diagram.

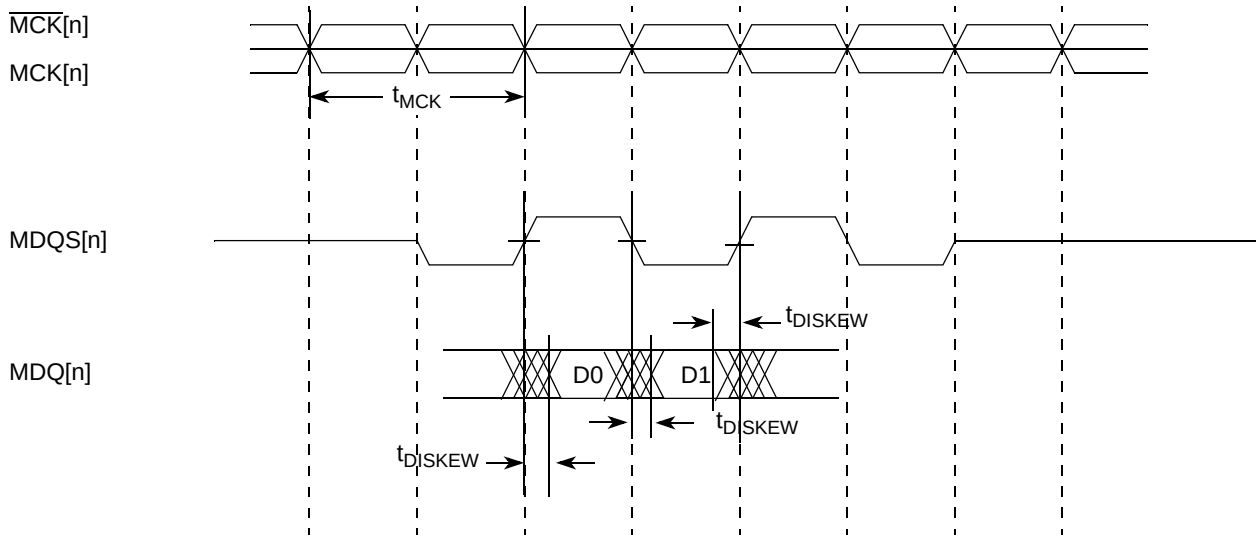


Figure 9. DDR3 SDRAM Interface Input Timing Diagram

2.6.1.2 DDR SDRAM Output AC Timing Specifications

Table 30 provides the output AC timing specifications for the DDR SDRAM interface.

Table 30. DDR SDRAM Output AC Timing Specifications

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	1.5	3	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}				3
• 1333 MHz data rate		0.606	—	ns	
• 1200 MHz data rate		0.675	—	ns	
• 1066 MHz data rate		0.744	—	ns	
• 800 MHz data rate		0.917	—	ns	
• 667 MHz data rate		1.10	—	ns	
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}				3
• 1333 MHz data rate		0.606	—	ns	
• 1200 MHz data rate		0.675	—	ns	
• 1066 MHz data rate		0.744	—	ns	
• 800 MHz data rate		0.917	—	ns	
• 667 MHz data rate		1.10	—	ns	
$\overline{\text{MCS}}$n output setup with respect to MCK	t_{DDKHCS}				3
• 1333 MHz data rate		0.606	—	ns	
• 1200 MHz data rate		0.675	—	ns	
• 1066 MHz data rate		0.744	—	ns	
• 800 MHz data rate		0.917	—	ns	
• 667 MHz data rate		1.10	—	ns	
$\overline{\text{MCS}}$n output hold with respect to MCK	t_{DDKHCX}				3
• 1333 MHz data rate		0.606	—	ns	
• 1200 MHz data rate		0.675	—	ns	
• 1066 MHz data rate		0.744	—	ns	
• 800 MHz data rate		0.917	—	ns	
• 667 MHz data rate		1.10	—	ns	
MCK to MDQS Skew	t_{DDKHMH}				4
• > 1066 MHz data rate		–0.245	0.245	ns	
• 800 MHz data rate		–0.375	0.375	ns	
• 667 MHz data rate		–0.6	0.6	ns	

Table 33. PCI Express 2.0 (2.5 Gbps) Differential Transmitter (Tx) Output AC Specifications (continued)

Parameter	Symbol	Min	Nom	Max	Units	Comments
Time between the jitter median and maximum deviation from the median.	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See notes 2 and 3.
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 4.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage test load as shown in Figure 16 and measured over any 250 consecutive Tx UIs.
3. A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-NAX-JITTER}$ = 0.25 UI for the transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The DSP device SerDes transmitter does not have a built-in C_{TX}. An external AC coupling capacitor is required.

Table 34. PCI Express 2.0 (2.5 Gbps) Differential Receiver (Rx) Input AC Specifications

Parameter	Symbol	Min	Nom	Max	Units	Comments
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1.
Minimum receiver eye width	T_{RX-EYE}	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER}$ = 1 – T_{RX-EYE}= 0.6 UI. See notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See notes 2, 3, and 4.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 16 should be used as the Rx device when taking measurements. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

Table 35. PCI Express 2.0 (5.0 Gbps) Differential Transmitter (Tx) Output AC Specifications

Parameter	Symbol	Min	Nom	Max	Units	Comments
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1.
Minimum Tx eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum Transmitter jitter can be derived as: $T_{TX-MAX-JITTER}$ = 1 – T_{TX-EYE} = 0.25 UI. See notes 2 and 3.
Tx RMS deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	—	—	0.15	ps	—
Tx RMS deterministic jitter < 1.5 MHz	$T_{TX-LF-RMS}$	—	3.0	—	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 4.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage test load as shown in Figure 16 and measured over any 250 consecutive Tx UIs.
3. A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-MAX-JITTER}$ = 0.25 UI for the Transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The DSP device SerDes transmitter does not have a built-in C_{TX}. An external AC coupling capacitor is required.

Table 36. PCI Express 2.0 (5.0 Gbps) Differential Receiver (Rx) Input AC Specifications

Parameter	Symbol	Min	Nom	Max	Units	Conditions
Unit Interval	UI	199.40	200.00	200.06	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Max Rx inherent timing error	$T_{RX-TJ-CC}$	—	—	0.4	UI	The maximum inherent total timing error for common REF_CLK Rx architecture
Maximum time between the jitter median and maximum deviation from the median	$T_{RX-TJ-DC}$	—	—	0.34	UI	Max Rx inherent total timing error
Max Rx inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	—	—	0.30	UI	The maximum inherent deterministic timing error for common REF_CLK Rx architecture
Max Rx inherent deterministic timing error	$T_{RX-DJ-DD-DC}$	—	—	0.24	UI	The maximum inherent deterministic timing error for common REF_CLK Rx architecture

Note: No test load is necessarily accosted with this value.

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in Figure 16.

Note: The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

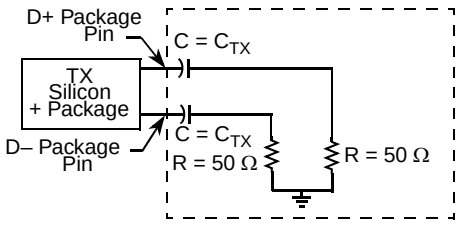


Figure 16. Test Measurement Load

Table 40. Serial RapidIO Short Run Receiver AC Timing Specifications at 5 Gbaud (continued)

Characteristic	Symbol	Min	Nom	Max	Unit
Total jitter (without sinusoidal jitter)	R_Tj	—	—	0.6	UIp-p
Note: The AC specifications do not include REF_CLK jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region in Figure 18. The ISI jitter (R_CBHPJ) and amplitude have to be correlated, for example, by a PCB trace.					

Table 41 defines the Transmitter AC specifications for long run Serial RapidIO interfaces using a transfer rate of 5 Gbps. The AC timing specifications do not include REF_CLK jitter.

Table 41. Serial RapidIO Transmitter Long Run AC Timing for Transfer Rate of 5 Gbps

Characteristic	Symbol	Min	Nom	Max	Unit	Conditions
Tx Baud Rate	T_Baud	5.000 – 100 ppm	5.000	5.000 + 100 ppm	Gbps	± 100 ppm
Uncorrelated high probability jitter	T_UHPJ			0.15	UI p-p	With de-emphasis disabled.
Total Jitter	T_TJ	—	—	0.30	UI p-p	With de-emphasis disabled.

Table 42 defines the Receiver AC specifications for long run Serial RapidIO interfaces using a transfer rate of 5 Gbps. The AC timing specifications do not include REF_CLK jitter.

Table 42. Serial RapidIO Receiver Long Run AC Timing for Transfer Rate of 5 Gbps

Characteristic	Symbol	Min	Nom	Max	Unit	Condition
Rx Baud Rate	R_Baud	5.000 – 100 ppm	5.000	5.000 + 100 ppm	Gbps	
Gaussian	R_GJ			0.275	UI p-p	Informative jitter budget @Rx input
Uncorrelated bounded high probability jitter (D_J)	R_UBHPJ			0.15	UI p-p	Informative jitter budget @Rx input
Correlated bounded high probability jitter (ISI)	R_CBHPJ			0.525	UI p-p	Informative jitter budget @Rx input
Bounded high probability jitter (D_J + ISI)	R_BHPJ			0.675	UI p-p	Informative jitter budget @Rx input
Sinusoidal jitter, maximum	R_SJ-max			5	UI p-p	Informative jitter budget @Rx input
Sinusoidal jitter, high frequency	R_SJ-hf			0.05	UI p-p	Informative jitter budget @Rx input
Total Jitter (does not include sinusoidal jitter).	R_TJ			0.95	UI p-p	Informative jitter budget @Rx input
Note: The AC specifications do not include REF_CLK jitter. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 18. The ISI jitter (R_CBHPJ) and amplitude have to be correlated, for example, by a PC trace.						

Figure 22 shows the AC test load for the timers.

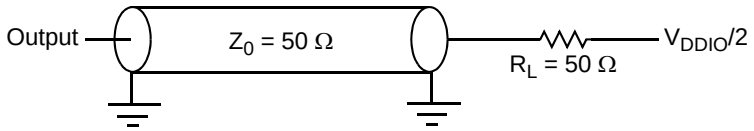


Figure 22. Timer AC Test Load

2.6.4 Ethernet Timing

This section describes the AC electrical characteristics for the Ethernet interface.

There are three general configuration registers used to configure the timing: GCR4, UCC1_DELAY_HR, and UCC3_DELAY_HR. These registers configure the programmable delay units (PDU) that should be programmed differently for each Interface to meet timing requirements. For additional information, see the *MSC8157E Reference Manual*.

2.6.4.1 Management Interface Timing

Table 50. Ethernet Controller Management Interface Timing

Characteristics	Symbol	Min	Max	Unit
GE_MDC frequency	f_{MDC}	—	2.5	MHz
GE_MDC period	t_{MDC}	400	—	ns
GE_MDC clock pulse width high	t_{MDC_H}	160	—	ns
GE_MDC clock pulse width low	t_{MDC_L}	160	—	ns
GE_MDC to GE_MDIO delay	t_{MDKHDX}	10	70	ns
GE_MDIO to GE_MDC rising edge setup time	t_{MDDVKH}	20	—	ns
GE_MDC rising edge to GE_MDIO hold time	t_{MDDXKH}	0	—	ns

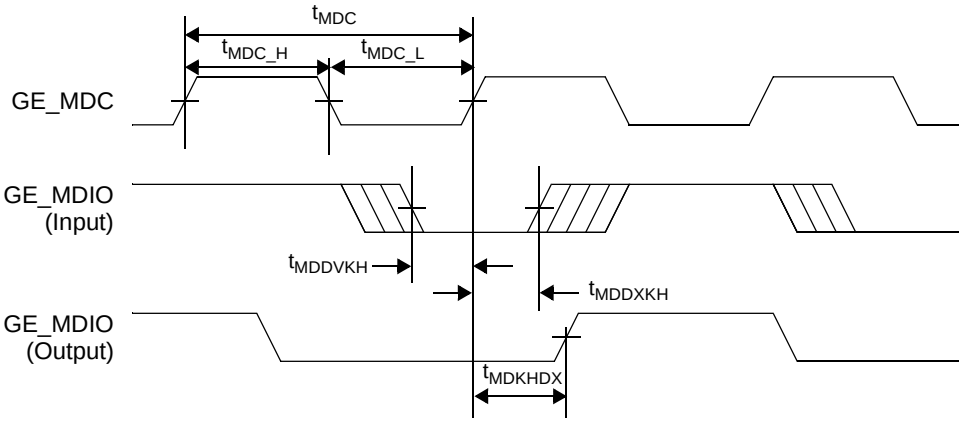


Figure 23. MII Management Interface Timing

2.6.4.2 RGMII AC Timing Specifications

Table 51 presents the RGMII AC timing specifications for applications requiring an on-board delayed clock.

Table 51. RGMII at 1 Gbps with On-Board Delay[2] AC Timing Specifications[1]

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)[3]	t_{SKEWT}	–0.5	—	0.5	ns
Data to clock input skew (at receiver)[3]	t_{SKEWR}	1	—	2.6	ns

Notes:
1. At recommended operating conditions with V_{DDIO} of 2.5 V ± 5%.
2. Program GCR4 as 0x00000000, UCC1_DELAY_HR as 0x00000000, and UCC3_DELAY_HR as 0x00000000.
3. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns is added to the associated clock signal.

Figure 24 shows the RGMII AC timing and multiplexing diagrams.

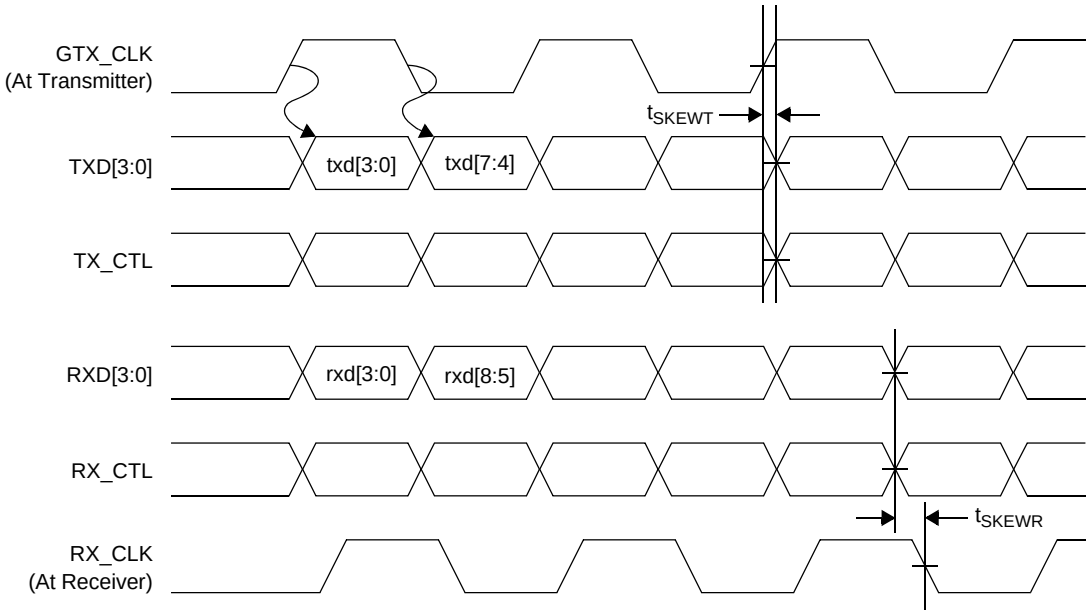


Figure 24. RGMII AC Timing and Multiplexing

2.6.5 SPI Timing

Table 52 lists the SPI input and output AC timing specifications.

Table 52. SPI AC Timing Specifications

Parameter	Symbol [1]	Min	Max	Unit	Note
SPI outputs valid—Master mode (internal clock) delay	t_{NIKHOV}	—	6	ns	2
SPI outputs hold—Master mode (internal clock) delay	t_{NIKHOX}	0.5	—	ns	2
SPI outputs valid—Slave mode (external clock) delay	t_{NEKHOV}	—	12	ns	2
SPI outputs hold—Slave mode (external clock) delay	t_{NEKHOX}	2	—	ns	2
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	12	—	ns	—
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns	—
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns	—
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns	—

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).
2. Output specifications are measured from the 50% level of the rising edge of SPICLK to the 50% level of the signal. Timings are measured at the pin.

Figure 25 provides the AC test load for the SPI.

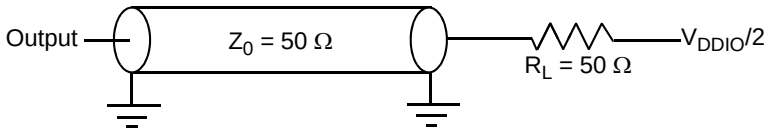
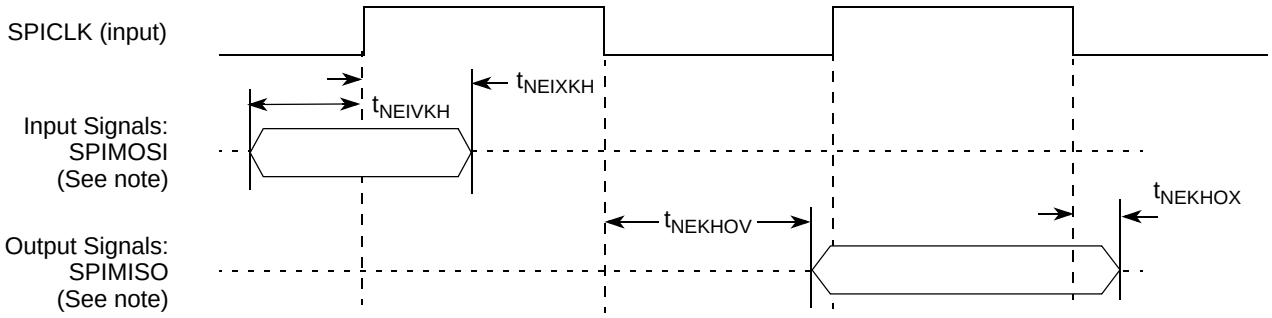


Figure 25. SPI AC Test Load

Figure 26 and Figure 27 represent the AC timings from Table 52. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 26 shows the SPI timings in slave mode (external clock).

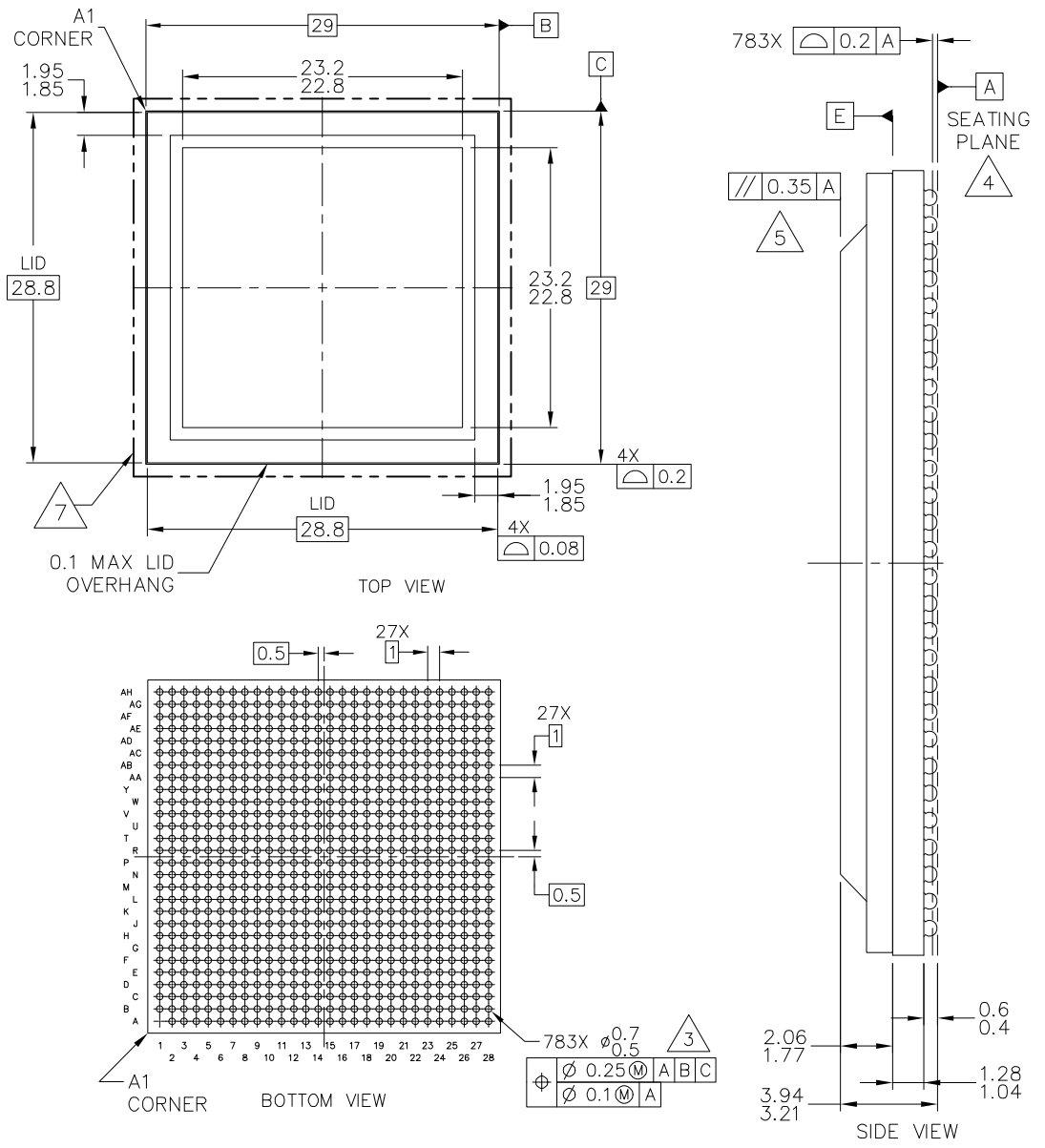


Note: measured with SPMODE[CI] = 0, SPMODE[CP] = 0

Figure 26. SPI AC Timing in Slave Mode (External Clock)

Figure 27 shows the SPI timings in master mode (internal clock).

5 Package Information



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURE PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. ALL DIMENSIONS ARE SYMMETRIC ACROSS THE PACKAGE CENTER LINES, UNLESS DIMENSIONED OTHERWISE.
7. 29.2MM MAXIMUM PACKAGE ASSEMBLY (LID + LAMINATE) X AND Y.

Figure 32. MSC8157E Mechanical Information, 783-ball FC-PBGA Package