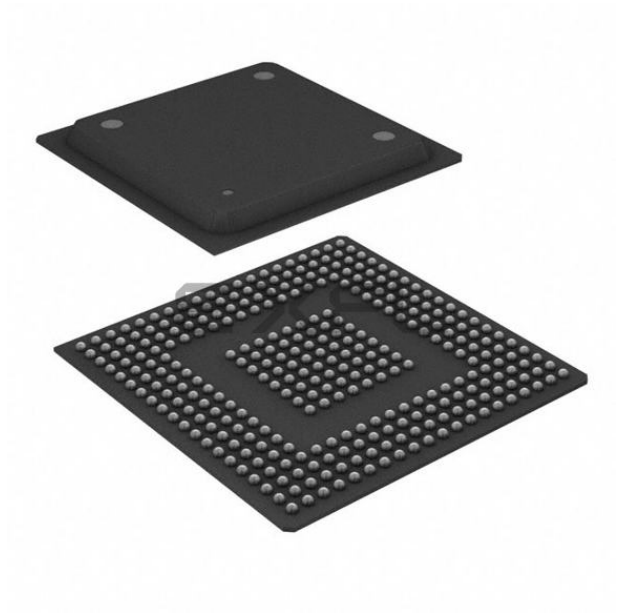

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

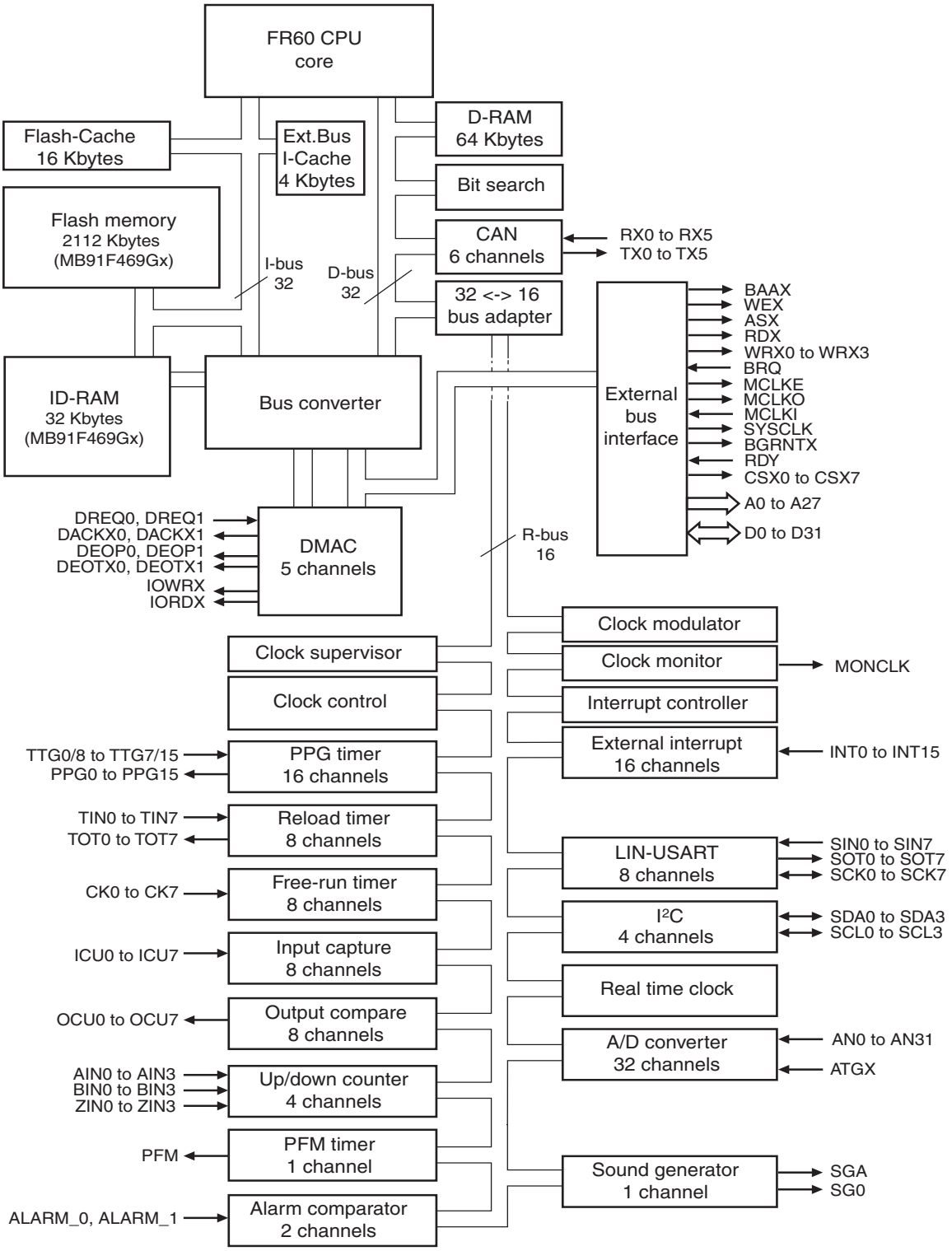
Details	
Product Status	Obsolete
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, WDT
Number of I/O	205
Program Memory Size	2.112MB (2.112M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	112K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	320-BBGA
Supplier Device Package	320-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f469gapb-gs-k6e1

Contents

JEDEC	Pin no.	Pin name	I/O	I/O circuit type[1]	Description
W11	103	P00_4	I/O	A	General-purpose input/output port
		D28			Signal pin of external data bus (bit28)
W12	104	P10_1	I/O	A	General-purpose input/output port
		ASX			Address strobe output pin
W13	105	P10_0	I/O	A	General-purpose input/output port
		SYSCLK			Clock output pin for external bus
W14	106	P10_5	I/O	A	General-purpose input/output port
		MCLKI			Clock input pin for memory
W15	107	TDO	O	O	Boundary Scan Test Data Out pin
W16	108	TDI	I	H	Boundary Scan Test Data In pin
W17	109	TRST	I	I	Boundary Scan Test Reset pin
W18	110	P21_2	I/O	A	General-purpose input/output port
		SCK0			Clock input/output pin of USART0
		CK0			External clock input pin of free-run timer 0
W19	111	P21_1	I/O	A	General-purpose input/output port
		SOT0			Data output pin of USART0
V19	112	P21_5	I/O	A	General-purpose input/output port
		SOT1			Data output pin of USART1
U19	113	P20_1	I/O	A	General-purpose input/output port
		SOT2			Data output pin of USART2
		BIN0			Up/down counter input pin
T19	114	X0A	---	J2	Sub clock (oscillation) input
R19	115	P19_1	I/O	A	General-purpose input/output port
		SOT4			Data output pin of USART4
P19	116	P19_4	I/O	A	General-purpose input/output port
		SIN5			Data input pin of USART5
N19	117	P18_0	I/O	A	General-purpose input/output port
		SIN6			Data input pin of USART6
		AIN2			Up/down counter input pin
M19	118	X0	---	J1	Clock (oscillation) input
L19	119	P17_0	I/O	A	General-purpose input/output port
		PPG0			Output pin of PPG timer
K19	120	P17_3	I/O	A	General-purpose input/output port
		PPG3			Output pin of PPG timer

7. Block Diagram

7.1 MB91F469Gx



9.6 Flash Security

9.6.1 Vector addresses

Two Flash Security Vectors (FSV1, FSV2) are located parallel to the Boot Security Vectors (BSV1, BSV2) controlling the protection functions of the Flash Security Module:

FSV1: 0x24:8000 BSV1: 0x24:8004
FSV2: 0x24:8008 BSV2: 0x24:800C

9.6.2 Security Vector FSV1

The setting of the Flash Security Vector FSV1 is responsible for the read and write protection modes and the individual write protection of the 8 Kbytes sectors.

9.6.2.1 FSV1 (bit31 to bit16)

The setting of the Flash Security Vector FSV1 bits [31:16] is responsible for the read and write protection modes.

Table 2. Explanation of the bits in the Flash Security Vector FSV1 [31:16]

FSV1[31:19]	FSV1[18] Write Protection Level	FSV1[17] Write Protection	FSV1[16] Read Protection	Flash Security Mode
set all to “0”	set to “0”	set to “0”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”)
set all to “0”	set to “0”	set to “1”	set to “0”	Write Protection (all device modes, without exception)
set all to “0”	set to “0”	set to “1”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”) and Write Protection (all device modes)
set all to “0”	set to “1”	set to “0”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”)
set all to “0”	set to “1”	set to “1”	set to “0”	Write Protection (all device modes, except INTVEC mode MD[2:0] = “000”)
set all to “0”	set to “1”	set to “1”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”) and Write Protection (all device modes except INTVEC mode MD[2:0] = “000”)

	Register				
Address	**+1**	**+2**	**+3**	**+4**	**Block**
000060_H	SCR04 [R/W,W] 00000000	SMR04 [R/W,W] 00000000	SSR04 [R/W,R] 00001000	RDR04/TDR04 [R/W] 00000000	LIN-USART 4 with FIFO
000064_H	ESCR04 [R/W] 00000X00	ECCR04 [R/W,R,W] -00000XX	FSR04 [R] - - - 00000	FCR04 [R/W] 0001 - 000	
000068_H	SCR05 [R/W,W] 00000000	SMR05 [R/W,W] 00000000	SSR05 [R/W,R] 00001000	RDR05/TDR05 [R/W] 00000000	LIN-USART 5 with FIFO
$00006C_H$	ESCR05 [R/W] 00000X00	ECCR05 [R/W,R,W] -00000XX	FSR05 [R] - - - 00000	FCR05 [R/W] 0001 - 000	
000070_H	SCR06 [R/W,W] 00000000	SMR06 [R/W,W] 00000000	SSR06 [R/W,R] 00001000	RDR06/TDR06 [R/W] 00000000	LIN-USART 6 with FIFO
000074_H	ESCR06 [R/W] 00000X00	ECCR06 [R/W,R,W] -00000XX	FSR06 [R] - - - 00000	FCR06 [R/W] 0001 - 000	
000078_H	SCR07 [R/W,W] 00000000	SMR07 [R/W,W] 00000000	SSR07 [R/W,R] 00001000	RDR07/TDR07 [R/W] 00000000	LIN-USART 7 with FIFO
$00007C_H$	ESCR07 [R/W] 00000X00	ECCR07 [R/W,R,W] -00000XX	FSR07 [R] - - - 00000	FCR07 [R/W] 0001 - 000	
000080_H	BGR100 [R/W] 00000000	BGR000 [R/W] 00000000	BGR101 [R/W] 00000000	BGR001 [R/W] 00000000	Baudrate Generator LIN-USART 0-7
000084_H	BGR102 [R/W] 00000000	BGR002 [R/W] 00000000	BGR103 [R/W] 00000000	BGR003 [R/W] 00000000	
000088_H	BGR104 [R/W] 00000000	BGR004 [R/W] 00000000	BGR105 [R/W] 00000000	BGR005 [R/W] 00000000	
$00008C_H$	BGR106 [R/W] 00000000	BGR006 [R/W] 00000000	BGR107 [R/W] 00000000	BGR007 [R/W] 00000000	
000090_H - $0000CC_H$	Reserved				Reserved
$0000D0_H$	IBCR0 [R/W] 00000000	IBSR0 [R] 00000000	ITBAH0 [R/W] - - - - - - 00	ITBAL0 [R/W] 00000000	I^2C 0
$0000D4_H$	ITMKH0 [R/W] 00 - - - - 11	ITMKL0 [R/W] 11111111	ISMK0 [R/W] 01111111	ISBA0 [R/W] - 0000000	
$0000D8_H$	Reserved	IDAR0 [R/W] 00000000	ICCR0 [R/W] 00011111	Reserved	
$0000DC_H$	IBCR1 [R/W] 00000000	IBSR1 [R] 00000000	ITBAH1 [R/W] - - - - - - 00	ITBAL1 [R/W] 00000000	I^2C 1
$0000E0_H$	ITMKH1 [R/W] 00 - - - - 11	ITMKL1 [R/W] 11111111	ISMK1 [R/W] 01111111	ISBA1 [R/W] - 0000000	
$0000E4_H$	Reserved	IDAR1 [R/W] 00000000	ICCR1 [R/W] 00011111	Reserved	
$0000E8_H$ - $0000FC_H$	Reserved				Reserved
000100_H	GCN10 [R/W] 00110010 00010000		Reserved	GCN20 [R/W] - - - - 0000	PPG Control 0-3

	Register				
Address	**+1**	**+2**	**+3**	**+4**	**Block**
000160_H	PTMR10 [R] 11111111 11111111		PCSR10 [W] XXXXXXXX XXXXXXXX		PPG 10
000164_H	PDUT10 [W] XXXXXXXX XXXXXXXX		PCNH10 [R/W] 0000000 -	PCNL10 [R/W] 000000 - 0	
000168_H	PTMR11 [R] 11111111 11111111		PCSR11 [W] XXXXXXXX XXXXXXXX		PPG 11
$00016C_H$	PDUT11 [W] XXXXXXXX XXXXXXXX		PCNH11 [R/W] 0000000 -	PCNL11 [R/W] 000000 - 0	
000170_H	P0TMCSRH [R/W] - 0 - 000 - 0	P0TMCSRL [R/W] - - - 00000	P1TMCSRH [R/W] - 0 - 000 - 0	P1TMCSRL [R/W] - - - 00000	Pulse Frequency Modulator
000174_H	P0TMRLR [W] XXXXXXXX XXXXXXXX		P0TMR [R] XXXXXXXX XXXXXXXX		
000178_H	P1TMRLR [W] XXXXXXXX XXXXXXXX		P1TMR [R] XXXXXXXX XXXXXXXX		
$00017C_H$	Reserved				Reserved
000180_H	Reserved	ICS01 [R/W] 00000000	Reserved	ICS23 [R/W] 00000000	Input Capture 0-3
000184_H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188_H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		
$00018C_H$	OCS01 [R/W] - - - 0 - - 00 0000 - - 00		OCS23 [R/W] - - - 0 - - 00 0000 - - 00		Output Compare 0-3
000190_H	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194_H	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
000198_H	SGCRH [R/W] 0000 - - 00	SGCRL [R/W] - - 0 - - 000	SGFR [R/W, R] XXXXXXXX XXXXXXXX		Sound Generator
$00019C_H$	SGAR [R/W] 00000000	Reserved	SGTR [R/W] XXXXXXXX	SGDR [R/W] XXXXXXXX	
$0001A0_H$	ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000		A/D Converter
$0001A4_H$	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
$0001A8_H$	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] - - - 00000	ADECH [R/W] - - - 00000	
$0001AC_H$	Reserved	ACSR0 [R/W] 011XXX00	Reserved	ACSR1 [R/W] 011XXX00	Alarm Comparator 0-1
$0001B0_H$	TMRLRC0 [W] XXXXXXXX XXXXXXXX		TMRC0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0 (PPG 0-1)
$0001B4_H$	Reserved		TMCSRCH0 [R/W] - - - 00000	TMCSRCL0 [R/W] 0 - 000000	

	Register				
Address	**+1**	**+2**	**+3**	**+4**	**Block**
000440_H	ICR00 [R/W] - - - 11111	ICR01 [R/W] - - - 11111	ICR02 [R/W] - - - 11111	ICR03 [R/W] - - - 11111	Interrupt Control register
000444_H	ICR04 [R/W] - - - 11111	ICR05 [R/W] - - - 11111	ICR06 [R/W] - - - 11111	ICR07 [R/W] - - - 11111	
000448_H	ICR08 [R/W] - - - 11111	ICR09 [R/W] - - - 11111	ICR10 [R/W] - - - 11111	ICR11 [R/W] - - - 11111	
$00044C_H$	ICR12 [R/W] - - - 11111	ICR13 [R/W] - - - 11111	ICR14 [R/W] - - - 11111	ICR15 [R/W] - - - 11111	
000450_H	ICR16 [R/W] - - - 11111	ICR17 [R/W] - - - 11111	ICR18 [R/W] - - - 11111	ICR19 [R/W] - - - 11111	
000454_H	ICR20 [R/W] - - - 11111	ICR21 [R/W] - - - 11111	ICR22 [R/W] - - - 11111	ICR23 [R/W] - - - 11111	
000458_H	ICR24 [R/W] - - - 11111	ICR25 [R/W] - - - 11111	ICR26 [R/W] - - - 11111	ICR27 [R/W] - - - 11111	
$00045C_H$	ICR28 [R/W] - - - 11111	ICR29 [R/W] - - - 11111	ICR30 [R/W] - - - 11111	ICR31 [R/W] - - - 11111	
000460_H	ICR32 [R/W] - - - 11111	ICR33 [R/W] - - - 11111	ICR34 [R/W] - - - 11111	ICR35 [R/W] - - - 11111	
000464_H	ICR36 [R/W] - - - 11111	ICR37 [R/W] - - - 11111	ICR38 [R/W] - - - 11111	ICR39 [R/W] - - - 11111	
000468_H	ICR40 [R/W] - - - 11111	ICR41 [R/W] - - - 11111	ICR42 [R/W] - - - 11111	ICR43 [R/W] - - - 11111	
$00046C_H$	ICR44 [R/W] - - - 11111	ICR45 [R/W] - - - 11111	ICR46 [R/W] - - - 11111	ICR47 [R/W] - - - 11111	
000470_H	ICR48 [R/W] - - - 11111	ICR49 [R/W] - - - 11111	ICR50 [R/W] - - - 11111	ICR51 [R/W] - - - 11111	
000474_H	ICR52 [R/W] - - - 11111	ICR53 [R/W] - - - 11111	ICR54 [R/W] - - - 11111	ICR55 [R/W] - - - 11111	
000478_H	ICR56 [R/W] - - - 11111	ICR57 [R/W] - - - 11111	ICR58 [R/W] - - - 11111	ICR59 [R/W] - - - 11111	
$00047C_H$	ICR60 [R/W] - - - 11111	ICR61 [R/W] - - - 11111	ICR62 [R/W] - - - 11111	ICR63 [R/W] - - - 11111	
000480_H	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] 00XXX – 00	CTBR [W] XXXXXXXX	Clock Control Unit
000484_H	CLKR [R/W] ---- 0000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488_H	Reserved				Reserved
$00048C_H$	PLLDIVM [R/W] - - - - 0000	PLLDIVN [R/W] - - 000000	PLLDIVG [R/W] - - - - 0000	PLLMULG [W] 00000000	PLL Clock Gear Unit
000490_H	PLLCTRL [R/W] - - - - 0000	Reserved			
000494_H	OSCC1 [R/W] - - - - - 010	OSCS1 [R/W] 00001111	OSCC2 [R/W] - - - - - 010	OSCS2 [R/W] 00001111	Main/Sub Oscillator Control
000498_H	PORTEN [R/W] - - - - - - 00	Reserved			Port Input Enable Control
$00049C_H$	Reserved				Reserved

	Register				
Address	**+1**	**+2**	**+3**	**+4**	**Block**
$0004A0_H$	Reserved	WTCER [R/W] - - - - - - 00	WTCR [R/W] 00000000 000 – 00 – 0		Watchdog Timer
$0004A4_H$	Reserved	WTBR [R/W] - - - XXXXX XXXXXXXX XXXXXXXX			
$0004A8_H$	WTHR [R/W] - - - 00000	WTMR [R/W] - - 000000	WTSR [R/W] - - 000000	Reserved	
$0004AC_H$	CSVTR [R/W] - - - 00010	CSVCR [R/W] 00011100	CSCFG [R/W] 0X000000	CMCFG [R/W] 00000000	Clock- Supervisor / Selector / Monitor
$0004B0_H$	CUCR [R/W] - - - - - - - - - - - - 0 - - 00		CUTD [R/W] 10000000 00000000		Calibration Unit of Sub Oscillation
$0004B4_H$	CUTR1 [R] - - - - - - - - 00000000		CUTR2 [R] 00000000 00000000		
$0004B8_H$	CMPR [R/W] - - 000010 11111101		Reserved	CMCR [R/W] - 001 - - 00	Clock Modulation
$0004BC_H$	CMT1 [R/W] 00000000 1 - - - 0000		CMT2 [R/W] - - 000000 - - 000000		
$0004C0_H$	CANPRE [R/W] 0 - - - 0000	CANCKD [R/W] - - 000000[1]	Reserved		CAN Clock Control
$0004C4_H$	LVSEL [R/W] 00000101	LVDET [R/W] -000 0 - 00	HWWDE [R/W] - - - - - - 00	HWWD [R/W,W] 00011000	LV Detection / Hardware-Watchdog
$0004C8_H$	OSCRH [R/W] 000 - - 001	OSCRL [R/W] - - - - - 000	WPCRH [R/W] 000 - - 000	WPCRL [R/W] - - - - - - 00	Main-/Sub-Oscillation Stabilization Timer
$0004CC_H$	OSCCR [R/W] - - - - - - 00	Reserved	REGSEL [R/W] - - 000100	REGCTR [R/W] - - - X - - 00	Main- Oscillation Standby Control Main/ Sub Regulator Control
$0004D0_H$ - $00063C_H$	Reserved				Reserved

	Register				
Address	**+1**	**+2**	**+3**	**+4**	**Block**
$000EC0_H$	PPER00 [R/W] 00000000	PPER01 [R/W] 00000000	PPER02 [R/W] 00000000	PPER03 [R/W] 00000000	Port Pull-Up/Down Enable register
$000EC4_H$	PPER04 [R/W] - - - - 0000	PPER05 [R/W] 00000000	PPER06 [R/W] 00000000	PPER07 [R/W] 00000000	
$000EC8_H$	PPER08 [R/W] 00000000	PPER09 [R/W] 00000000	PPER10 [R/W] - 0000000	PPER11 [R/W] - - - - - - 00	
$000ECC_H$	Reserved	PPER13 [R/W] 00000000	PPER14 [R/W] 00000000	PPER15 [R/W] 00000000	
$000ED0_H$	PPER16 [R/W] 00000000	PPER17 [R/W] 00000000	PPER18 [R/W] - 000 - 000	PPER19 [R/W] - 000 - 000	
$000ED4_H$	PPER20 [R/W] - 000 - 000	PPER21 [R/W] - 000 - 000	PPER22 [R/W] 00000000	PPER23 [R/W] 00000000	
$000ED8_H$	PPER24 [R/W] 00000000	Reserved	PPER26 [R/W] 00000000	PPER27 [R/W] 00000000	
$000EDC_H$	PPER28 [R/W] 00000000	PPER29 [R/W] 00000000	Reserved		
$000EE0_H$ - $000EFC_H$	Reserved				Reserved
$000F00_H$	PPCR00 [R/W] 11111111	PPCR01 [R/W] 11111111	PPCR02 [R/W] 11111111	PPCR03 [R/W] 11111111	Port Pull-Up/Down Control register
$000F04_H$	PPCR04 [R/W] - - - - 1111	PPCR05 [R/W] 11111111	PPCR06 [R/W] 11111111	PPCR07 [R/W] 11111111	
$000F08_H$	PPCR08 [R/W] 11111111	PPCR09 [R/W] 11111111	PPCR10 [R/W] - 1111111	PPCR11 [R/W] - - - - - - 11	
$000F0C_H$	Reserved	PPCR13 [R/W] 11111111	PPCR14 [R/W] 11111111	PPCR15 [R/W] 11111111	
$000F10_H$	PPCR16 [R/W] 11111111	PPCR17 [R/W] 11111111	PPCR18 [R/W] - 111 - 111	PPCR19 [R/W] - 111 - 111	
$000F14_H$	PPCR20 [R/W] - 111 - 111	PPCR21 [R/W] - 111 - 111	PPCR22 [R/W] 11111111	PPCR23 [R/W] 11111111	
$000F18_H$	PPCR24 [R/W] 11111111	Reserved	PPCR26 [R/W] 11111111	PPCR27 [R/W] 11111111	
$000F1C_H$	PPCR28 [R/W] 11111111	PPCR29 [R/W] 11111111	Reserved		
$000F20_H$ - $000FFC_H$	Reserved				Reserved

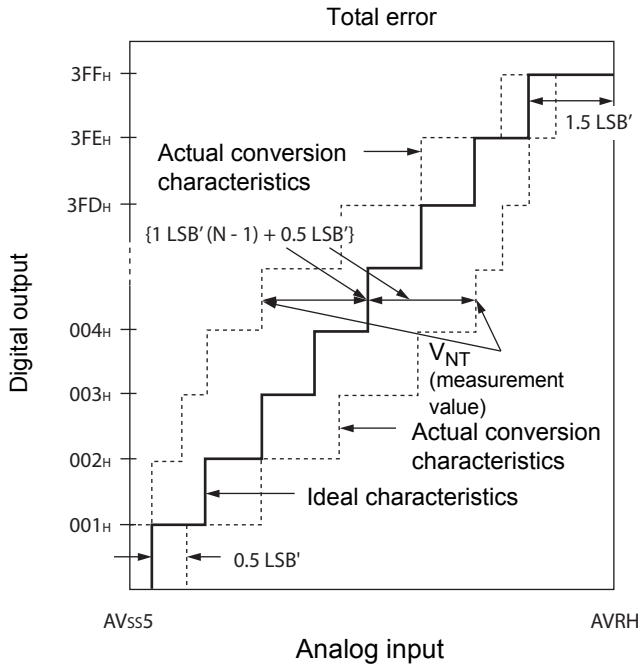
	Register				
Address	+1	+2	+3	+4	Block
$00C000_H$	CTRLR0 [R/W] 00000000 00000001		STATR0 [R/W] 00000000 00000000		CAN 0 Control register
$00C004_H$	ERRCNT0 [R] 00000000 00000000		BTR0 [R/W] 00100011 00000001		
$00C008_H$	INTR0 [R] 00000000 00000000		TESTR0 [R/W] 00000000 X0000000		
$00C00C_H$	BRPE0 [R/W] 00000000 00000000		Reserved		
$00C010_H$	IF1CREQ0 [R/W] 00000000 00000001		IF1CMSK0 [R/W] 00000000 00000000		CAN 0 IF 1 Register
$00C014_H$	IF1MSK20 [R/W] 11111111 11111111		IF1MSK10 [R/W] 11111111 11111111		
$00C018_H$	IF1ARB20 [R/W] 00000000 00000000		IF1ARB10 [R/W] 00000000 00000000		
$00C01C_H$	IF1MCTR0 [R/W] 00000000 00000000		Reserved		
$00C020_H$	IF1DTA10 [R/W] 00000000 00000000		IF1DTA20 [R/W] 00000000 00000000		
$00C024_H$	IF1DTB10 [R/W] 00000000 00000000		IF1DTB20 [R/W] 00000000 00000000		
$00C028_H$ - $00C02C_H$	Reserved				Reserved
$00C030_H$	IF1DTA20 [R/W] 00000000 00000000		IF1DTA10 [R/W] 00000000 00000000		CAN 0 IF 1 Register mirror
$00C034_H$	IF1DTB20 [R/W] 00000000 00000000		IF1DTB10 [R/W] 00000000 00000000		
$00C038_H$ - $00C03C_H$	Reserved				Reserved
$00C040_H$	IF2CREQ0 [R/W] 00000000 00000001		IF2CMSK0 [R/W] 00000000 00000000		CAN 0 IF 2 Register
$00C044_H$	IF2MSK20 [R/W] 11111111 11111111		IF2MSK10 [R/W] 11111111 11111111		
$00C048_H$	IF2ARB20 [R/W] 00000000 00000000		IF2ARB10 [R/W] 00000000 00000000		
$00C04C_H$	IF2MCTR0 [R/W] 00000000 00000000		Reserved		
$00C050_H$	IF2DTA10 [R/W] 00000000 00000000		IF2DTA20 [R/W] 00000000 00000000		
$00C054_H$	IF2DTB10 [R/W] 00000000 00000000		IF2DTB20 [R/W] 00000000 00000000		
$00C058_H$ - $00C05C_H$	Reserved				Reserved

	Register				
Address	**+1**	**+2**	**+3**	**+4**	**Block**
$00C260_H$	IF2DTA22 [R/W] 00000000 00000000		IF2DTA12 [R/W] 00000000 00000000		CAN 2 IF 2 Register mirror
$00C264_H$	IF2DTB22 [R/W] 00000000 00000000		IF2DTB12 [R/W] 00000000 00000000		
$00C268_H$ - $00C27C_H$	Reserved				Reserved
$00C280_H$	TREQR22 [R] 00000000 00000000		TREQR12 [R] 00000000 00000000		CAN 2 Status Flags
$00C284_H$	TREQR42 [R] 00000000 00000000		TREQR32 [R] 00000000 00000000		
$00C288_H$	TREQR62 [R] 00000000 00000000		TREQR52 [R] 00000000 00000000		
$00C28C_H$	TREQR82 [R] 00000000 00000000		TREQR72 [R] 00000000 00000000		
$00C290_H$	NEWDT22 [R] 00000000 00000000		NEWDT12 [R] 00000000 00000000		
$00C294_H$	NEWDT42 [R] 00000000 00000000		NEWDT32 [R] 00000000 00000000		
$00C298_H$	NEWDT62 [R] 00000000 00000000		NEWDT52 [R] 00000000 00000000		
$00C29C_H$	NEWDT82 [R] 00000000 00000000		NEWDT72 [R] 00000000 00000000		
$00C2A0_H$	INTPND22 [R] 00000000 00000000		INTPND12 [R] 00000000 00000000		
$00C2A4_H$	INTPND42 [R] 00000000 00000000		INTPND32 [R] 00000000 00000000		
$00C2A8_H$	INTPND62 [R] 00000000 00000000		INTPND52 [R] 00000000 00000000		
$00C2AC_H$	INTPND82 [R] 00000000 00000000		INTPND72 [R] 00000000 00000000		
$00C2B0_H$	MSGVAL22 [R] 00000000 00000000		MSGVAL12 [R] 00000000 00000000		
$00C2B4_H$	MSGVAL42 [R] 00000000 00000000		MSGVAL32 [R] 00000000 00000000		
$00C2B8_H$	MSGVAL62 [R] 00000000 00000000		MSGVAL52 [R] 00000000 00000000		
$00C2BC_H$	MSGVAL82 [R] 00000000 00000000		MSGVAL72 [R] 00000000 00000000		
$00C2C0_H$ - $00C2FC_H$	Reserved				Reserved

13. Interrupt Vector Table

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Reset	0	00	–	–	$3FC_H$	$000FFFFC_H$	–
Mode vector	1	01	–	–	$3F8_H$	$000FFFF8_H$	–
System Reserved	2	02	–	–	$3F4_H$	$000FFFF4_H$	–
System Reserved	3	03	–	–	$3F0_H$	$000FFFF0_H$	–
System Reserved	4	04	–	–	$3EC_H$	$000FFFEC_H$	–
CPU supervisor mode (INT #5 instruction) [5]	5	05	–	–	$3E8_H$	$000FFFE8_H$	–
Memory Protection exception [5]	6	06	–	–	$3E4_H$	$000FFFE4_H$	–
System Reserved	7	07	–	–	$3E0_H$	$000FFFE0_H$	–
System Reserved	8	08	–	–	$3DC_H$	$000FFFDC_H$	–
System Reserved	9	09	–	–	$3D8_H$	$000FFFD8_H$	–
System Reserved	10	0A	–	–	$3D4_H$	$000FFFD4_H$	–
System Reserved	11	0B	–	–	$3D0_H$	$000FFFD0_H$	–
System Reserved	12	0C	–	–	$3CC_H$	$000FFFCC_H$	–
System Reserved	13	0D	–	–	$3C8_H$	$000FFFC8_H$	–
Undefined instruction exception	14	0E	–	–	$3C4_H$	$000FFFC4_H$	–
NMI request	15	0F	F_H fixed		$3C0_H$	$000FFFC0_H$	–
External Interrupt 0	16	10	ICR00	440_H	$3BC_H$	$000FFFBC_H$	0, 16
External Interrupt 1	17	11			$3B8_H$	$000FFFB8_H$	1, 17
External Interrupt 2	18	12	ICR01	441_H	$3B4_H$	$000FFFB4_H$	2, 18
External Interrupt 3	19	13			$3B0_H$	$000FFFB0_H$	3, 19
External Interrupt 4	20	14	ICR02	442_H	$3AC_H$	$000FFFAC_H$	20
External Interrupt 5	21	15			$3A8_H$	$000FFFA8_H$	21
External Interrupt 6	22	16	ICR03	443_H	$3A4_H$	$000FFFA4_H$	22
External Interrupt 7	23	17			$3A0_H$	$000FFFA0_H$	23
External Interrupt 8	24	18	ICR04	444_H	$39C_H$	$000FFF9C_H$	–
External Interrupt 9	25	19			398_H	$000FFF98_H$	–
External Interrupt 10	26	1A	ICR05	445_H	394_H	$000FFF94_H$	–
External Interrupt 11	27	1B			390_H	$000FFF90_H$	–
External Interrupt 12	28	1C	ICR06	446_H	$38C_H$	$000FFF8C_H$	–
External Interrupt 13	29	1D			388_H	$000FFF88_H$	–
External Interrupt 14	30	1E	ICR07	447_H	384_H	$000FFF84_H$	–
External Interrupt 15	31	1F			380_H	$000FFF80_H$	–

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
2	3	046E	64	55.3	75.9	
2	5	04AC	64	49.9	89.1	
3	3	066D	64	52.5	82	
4	3	086C	64	49.9	89.1	
5	3	0A6B	64	47.6	97.6	
1	3	026F	60	54.9	66.1	
1	5	02AE	60	51.9	71	
1	7	02ED	60	49.3	76.7	
1	9	032C	60	46.9	83.3	
1	11	036B	60	44.7	91.3	
2	3	046E	60	51.9	71	
2	5	04AC	60	46.9	83.3	
3	3	066D	60	49.3	76.7	
4	3	086C	60	46.9	83.3	
5	3	0A6B	60	44.7	91.3	
1	3	026F	56	51.4	61.6	
1	5	02AE	56	48.6	66.1	
1	7	02ED	56	46.1	71.4	
1	9	032C	56	43.8	77.6	
1	11	036B	56	41.8	84.9	
1	13	03AA	56	39.9	93.8	
2	3	046E	56	48.6	66.1	
2	5	04AC	56	43.8	77.6	
2	7	04EA	56	39.9	93.8	
3	3	066D	56	46.1	71.4	
3	5	06AA	56	39.9	93.8	
4	3	086C	56	43.8	77.6	
5	3	0A6B	56	41.8	84.9	
6	3	0C6A	56	39.9	93.8	
1	3	026F	52	47.8	57	
1	5	02AE	52	45.2	61.2	
1	7	02ED	52	42.9	66.1	
1	9	032C	52	40.8	71.8	
1	11	036B	52	38.8	78.6	
1	13	03AA	52	37.1	86.8	



$$1LSB' \text{ (ideal value)} = \frac{AVRH - AV_{SS}5}{1024} \text{ [V]}$$

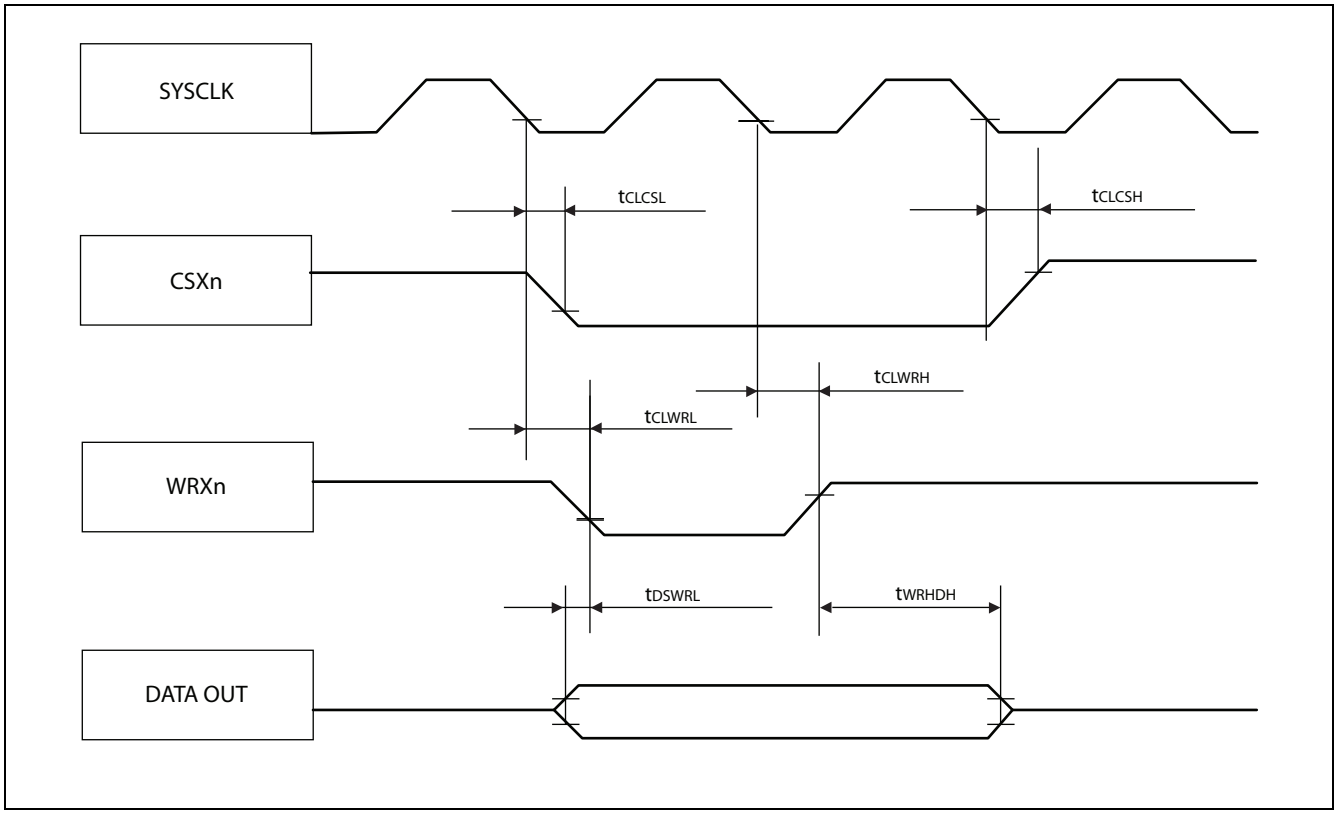
$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ LSB' \cdot (N - 1) + 0.5\ LSB'\}}{1\ LSB'}$$

N: A/D converter digital output value
V_{OT}' (ideal value) = $AV_{SS}5 + 0.5$ LSB' [V]
V_{FST}' (ideal value) = AVRH − 1.5 LSB' [V]
V_{NT}: Voltage at which the digital output changes from $(N + 1)_H$ to N_H

15.7.7.5 Synchronous Write Access - No Byte Control Type

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = − 40 °C to + 125 °C)

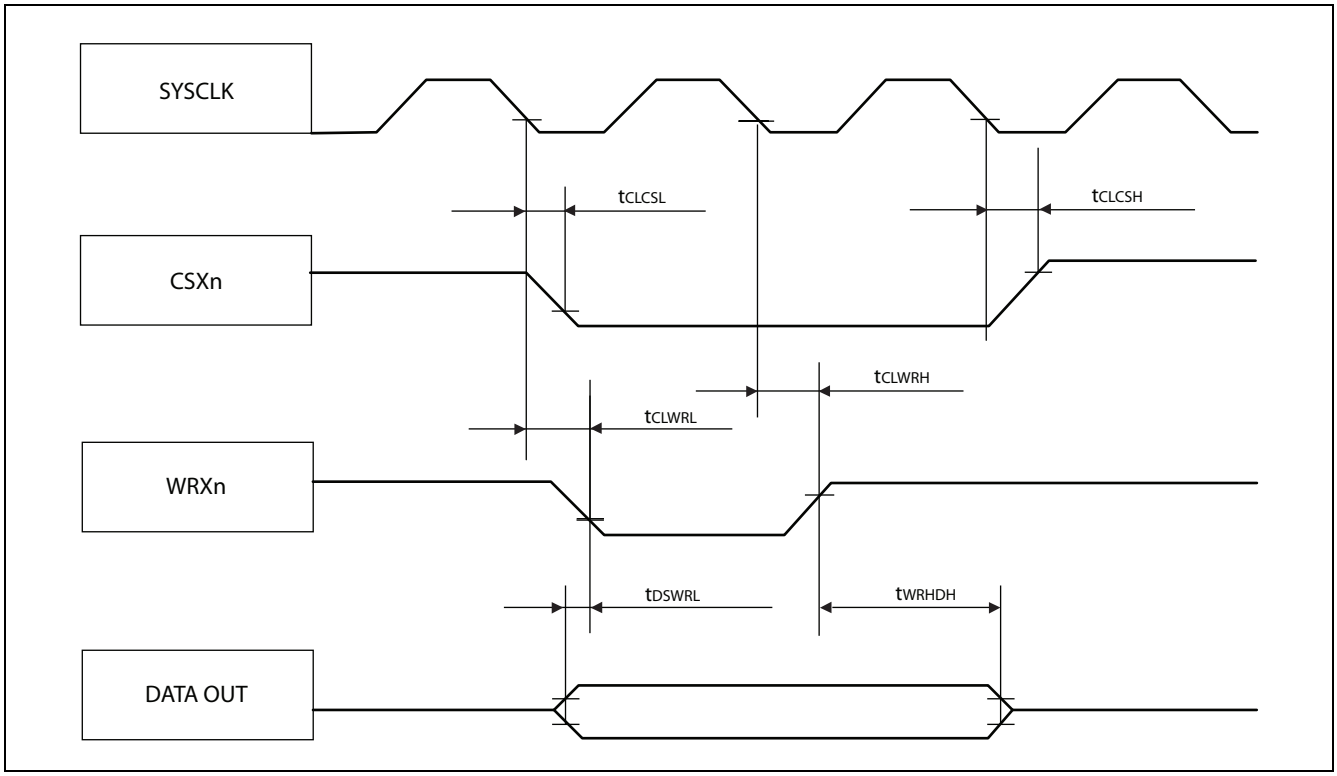
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↓ to WRXn delay time	t_{CLWRL}	SYSCLK WRXn	−	9	ns
	t_{CLWRH}		− 1	−	ns
Data valid to WRXn ↓ setup time	t_{DSWRL}	WRXn D31 to D0	− 6	−	ns
WRXn ↑ to Data valid hold time	t_{WRHDH}	WRXn D31 to D0	t_{CLKT} − 10	−	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	−	9	ns
	t_{CLCSH}		−	8	ns



15.7.8.5 Synchronous Write Access - No Byte Control Type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = − 40 °C to + 125 °C)

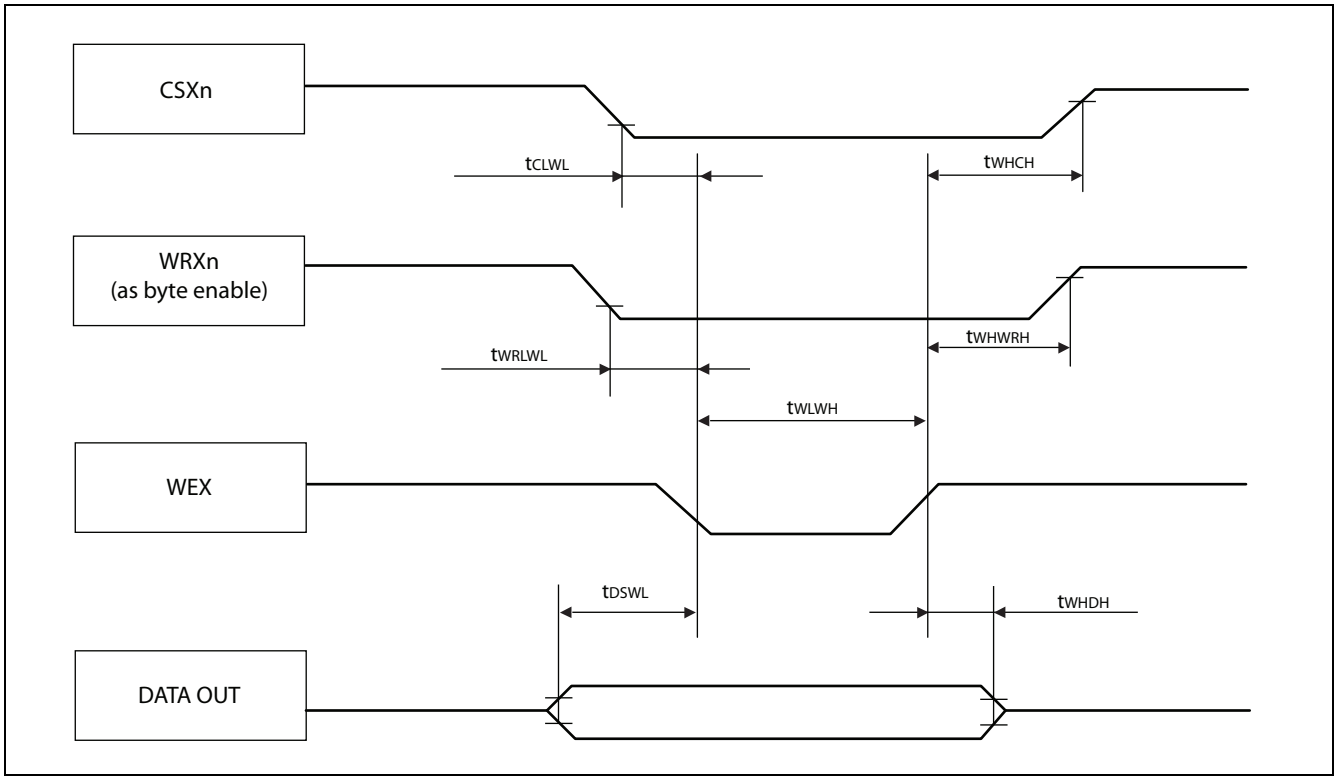
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↓ to WRXn delay time	t_{CLWRL}	SYSCLK WRXn	–	5	ns
	t_{CLWRH}		– 1	–	ns
Data valid to WRXn ↓ setup time	t_{DSWRL}	WRXn D31 to D0	– 11	–	ns
WRXn ↑ to Data valid hold time	t_{WRHDH}	WRXn D31 to D0	t_{CLKT} – 13	–	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	–	5	ns
	t_{CLCSH}		–	6	ns



15.7.8.6 Asynchronous Write Access - Byte Control Type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = − 40 °C to + 125 °C)

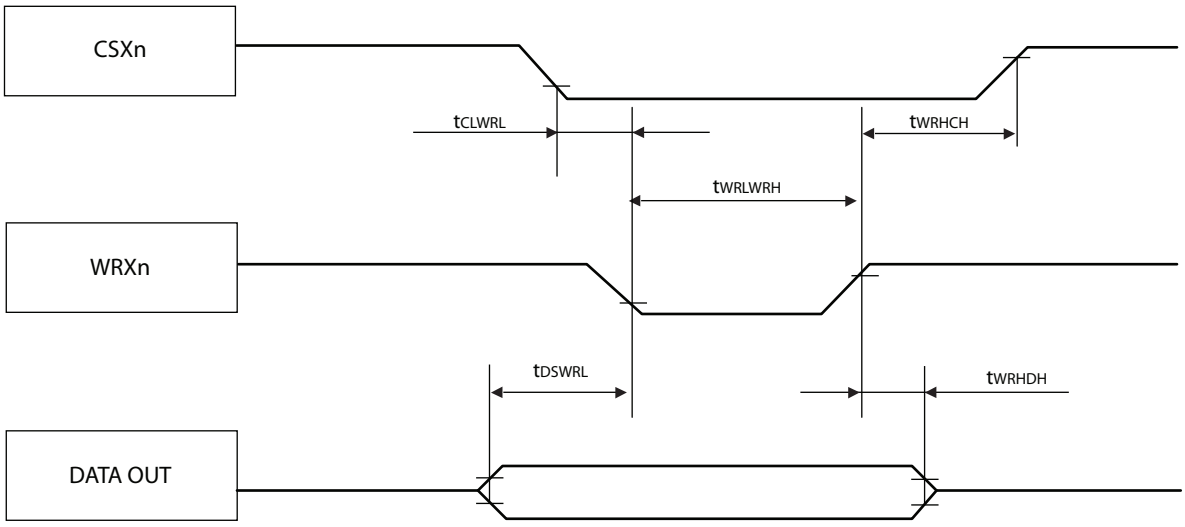
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WEX ↓ to WEX ↑ pulse width	t_{WLWH}	WEX	t_{CLKT} − 4	−	ns
Data valid to WEX ↓ setup time	t_{DSWL}	WEX D31 to D0	1/2 · t_{CLKT} − 12	−	ns
WEX ↑ to Data valid hold time	t_{WHDH}	WEX D31 to D0	1/2 · t_{CLKT} − 11	−	ns
WEX to WRXn delay time	t_{WRLWL}	WEX WRXn	−	1/2 · t_{CLKT} + 1	ns
	t_{WHWRH}		1/2 · t_{CLKT} − 1	−	ns
WEX to CSXn delay time	t_{CLWL}	WEX CSXn	−	1/2 · t_{CLKT} − 1	ns
	t_{WHCH}		1/2 · t_{CLKT} + 1	−	ns



15.7.8.7 Asynchronous Write Access - No Byte Control Type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = − 40 °C to + 125 °C)

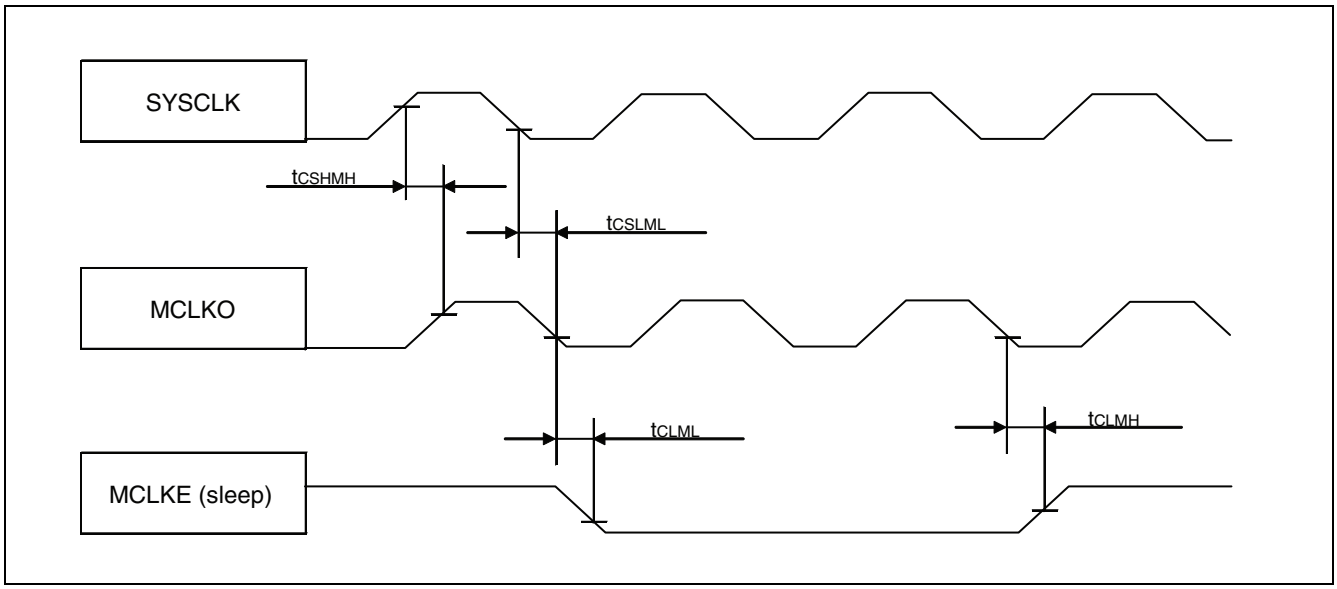
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WRXn ↓ to WRXn ↑ pulse width	t_{WRLWRH}	WRXn	t_{CLKT} − 3	−	ns
Data valid to WRXn ↓ setup time	t_{DSWRL}	WRXn D31 to D0	1/2 · t_{CLKT} − 12	−	ns
WRXn ↑ to Data valid hold time	t_{WRHDH}	WRXn D31 to D0	1/2 · t_{CLKT} − 11	−	ns
WRXn to CSXn delay time	t_{CLWRL}	WRXn CSXn	−	1/2 · t_{CLKT} − 1	ns
	t_{WRHCH}		1/2 · t_{CLKT} + 1	−	ns



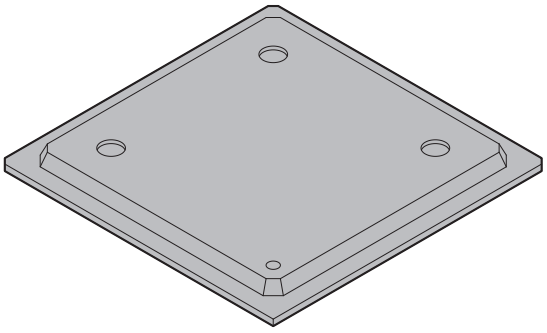
15.7.8.10 Clock Relationships

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = − 40 °C to + 125 °C)

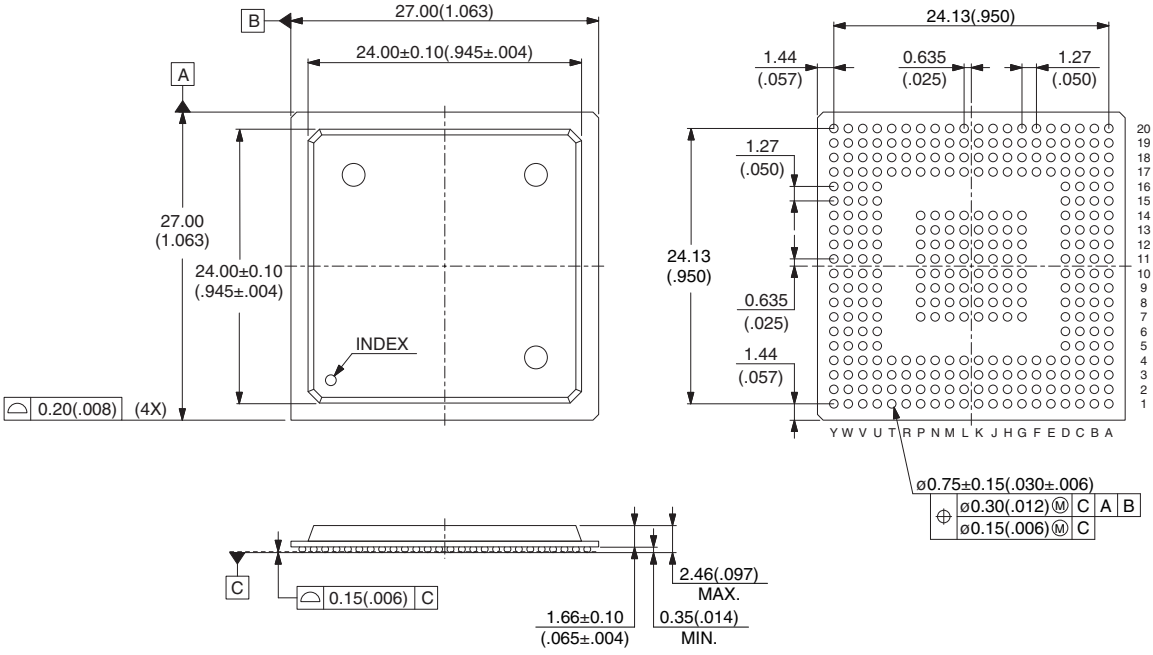
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK to MCLKO	t_{CSHMH}	SYSCLK MCLKO	1	5	ns
	t_{CSLML}		0	2	ns
MCLKO ↓ to MCLKE (in sleep mode)	t_{CLML}	MCLKO MCLKE	−	4	ns
	t_{CLMH}		− 3	−	ns



17. Package Dimension

320-pin plastic PBGA		
	Lead pitch	1.27 mm
	Package width × package length	27.00 mm × 27.00 mm
	Lead shape	Ball
	Sealing method	Plastic mold
	Mounting height	2.46 mm Max
	Weight	2.90 g
(BGA-320P-M06)		

320-pin plastic PBGA
(BGA-320P-M06)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.