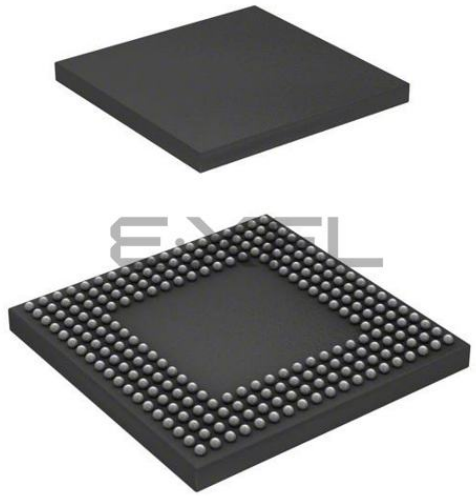

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-3 DSP
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	FIFO, SCI, SIO, SmartCard, USB
Peripherals	DMA, LCD, POR, WDT
Number of I/O	104
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 2.05V
Data Converters	A/D 6x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	240-LFBGA
Supplier Device Package	240-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd6417727bp100cv

Item	Features
Bus state controller (BSC)	• Physical address space divided into six areas (area 0, areas 2 to 6), each of up to 64 Mbytes, with the following features settable for each area: — Bus size (8, 16, or 32 bits) — Number of wait cycles (hardware wait function also waited) — Direct connection of SRAM, synchronous DRAM, and burst ROM possible by designating memory to be connected to each area — Supports PCMCIA interface (2 channels) — Chip select signals (CS0, CS2–CS6) for relevant area • Synchronous DRAM refresh function — Programmable refresh interval — Supports CAS-before-RAS refresh and self-refresh modes — Supports power-down DRAM • Synchronous DRAM burst access function • Big endian or little endian can be specified
Li bus state controller (LBSC)	• Bus State Controller for LCDC or USB Host • Supports synchronous DRAM • Synchronous DRAM access function (area 3)
User debug Interface (H-UDI)	• E10A emulator support • Pin arrangement conforming to JTAG specification • Realtime branch trace
Timer (TMU)	• 3-channel auto-reload-type 32-bit timer • Choice of six counter input clocks • Maximum resolution: 2 MHz
Realtime clock (RTC)	• Built-in clock, calendar functions, and alarm functions • On-chip 32-kHz crystal oscillator circuit with a maximum resolution (cycle interrupt) of 1/256 second
Serial communi-cation interface (SCI)	• Asynchronous mode or clock synchronous mode can be selected • Full-duplex communication • Supports smart card interface

Item	Features
LCD controller (LCDC)	• From 16 x 1 to 1024 x 1024 pixels can be supported • 4/8/15/16 bpp (bit per pixel) color modes • 1/2/4/6 bpp (bit per pixel) gray scale • 8-bit Frame rate controller • TFT/DSTN/STN • Signal polarity setting function • Hardware panel rotation • Power control function • Selectable clock source (LCLK, bus clock (Bϕ), or peripheral clock (Pϕ))
AFE I/F	• ST7550 direct interface • Telephone line control • 128-word FIFO for transfer • 128-word FIFO for receive
I/O port	• Thirteen 8-bit I/O ports
A/D converter (ADC)	• 10 bits ± 4 LSB, 6 channels • Conversion time: 15 µs • Input range: 0–Vcc (max. 3.6 V)
D/A converter (DAC)	• 8 bits ± 4 LSB, 2 channels • Conversion time: 10 µs • Output range: 0–Vcc (max. 3.6 V)

Product lineup

	Power Supply Voltage				
SH7727	**I/O**	**Internal**	**Operating Frequency**	**Model Name**	**Package**
160 MHz products	3.0 V to 3.6 V	1.70 V to 2.05 V	160 MHz	HD6417727F160C	240-pin plastic HQFP (PRQP0240KC-B)
				HD6417727BP160C	240-pin CSP (PLBG0240JA-A)
100 MHz products	2.6 V to 3.6 V	1.60 V to 2.05 V	100 MHz	HD6417727F100C	240-pin plastic HQFP (PRQP0240KC-B)
				HD6417727BP100C	240-pin CSP (PLBG0240JA-A)

MMU Exception in the Data Access Mode

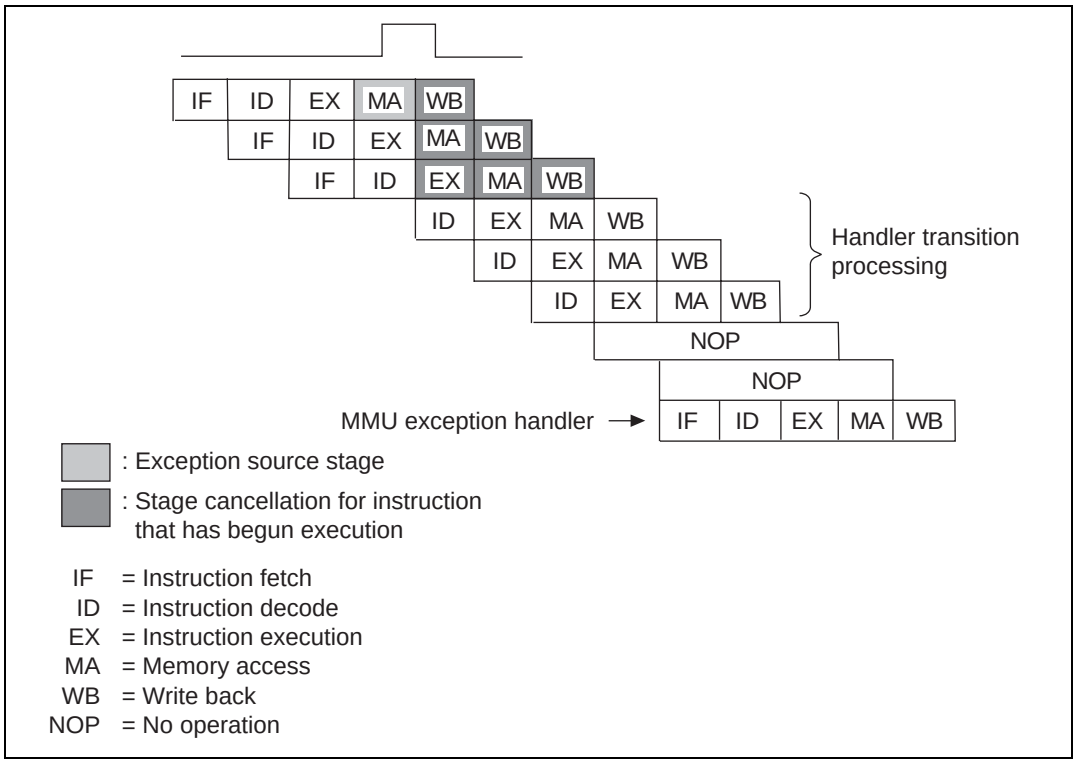


Figure 3.13 MMU Exception Signals in Data Access

- Manual Reset
  - Conditions: $\overline{\text{RESETM}}$ low
  - Operations: EXPEVT set to H'020, VBR and SR initialized, branch to PC = H'A0000000. Initialization sets the VBR register to H'00000000. In SR, the MD, RB, and BL bits are set to 1 and the interrupt mask bits (I3 to I0) is set to 1111. The CPU and on-chip supporting modules are initialized. See the register descriptions in the relevant sections for details. A high level is output from the STATUS0 and STATUS1 pins.

- H-UDI Reset
  - Conditions: H-UDI reset command input (see section 31.4.3, H-UDI Reset)
  - Operations: EXPEVT set to H'000, VBR and SR initialized, branch to PC = H'A0000000. Initialization sets the VBR register to H'0000000. In SR, the MD, RB and BL bits are set to 1 and the interrupt mask bits (I3 to I0) is set to 1111. The CPU and on-chip supporting modules are initialized. See the register descriptions in the relevant sections for details.

Table 4.4 Types of Reset

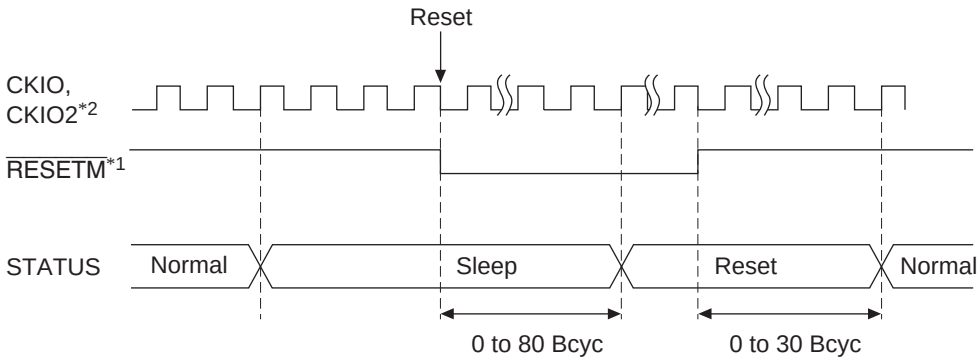
Type	Conditions for Transition to Reset State	Internal State	
		CPU	On-Chip Supporting Modules
Power-on reset	$\overline{\text{RESETP}}$ = Low	Initialized	(See register configuration in relevant sections)
Manual reset	$\overline{\text{RESETM}}$ = Low	Initialized	
H-UDI reset	H-UDI reset command input	Initialized	

4.5.2 General Exceptions

- TLB miss exception
  - Conditions: Comparison of TLB addresses shows no address match
  - Operations: The logical address (32 bits) that caused the exception is set in TEA and the corresponding virtual page number (22 bits) is set in PTEH (31 to 10). The ASID of PTEH indicates the ASID at the time the exception occurred. The RC bit in MMUCR is incremented by 1 when all ways are enabled, and if there is a disabled way, setting is prioritized starting from way 0.

  The PC and SR of the instruction that generated the exception are saved to the SPC and SSR, respectively. If the exception occurred during a read, H'040 is set in EXPEVT; if the exception occurred during a write, H'060 is set in EXPEVT. The BL, MD and RB bits in SR are set to 1 and a branch occurs to PC = VBR + H'0400.

Sleep to Manual Reset



Notes: 1. Keep $\overline{\text{RESETM}}$ low until the STATUS becomes reset.
2. CKIO2 can be used at only clock modes 0, 1 and 2.

Figure 9.9 Sleep to Manual Reset STATUS Output

fill operation in the event of a cache miss, the missed data is read first, then 16-byte boundary data including the missed data is read in wraparound mode.

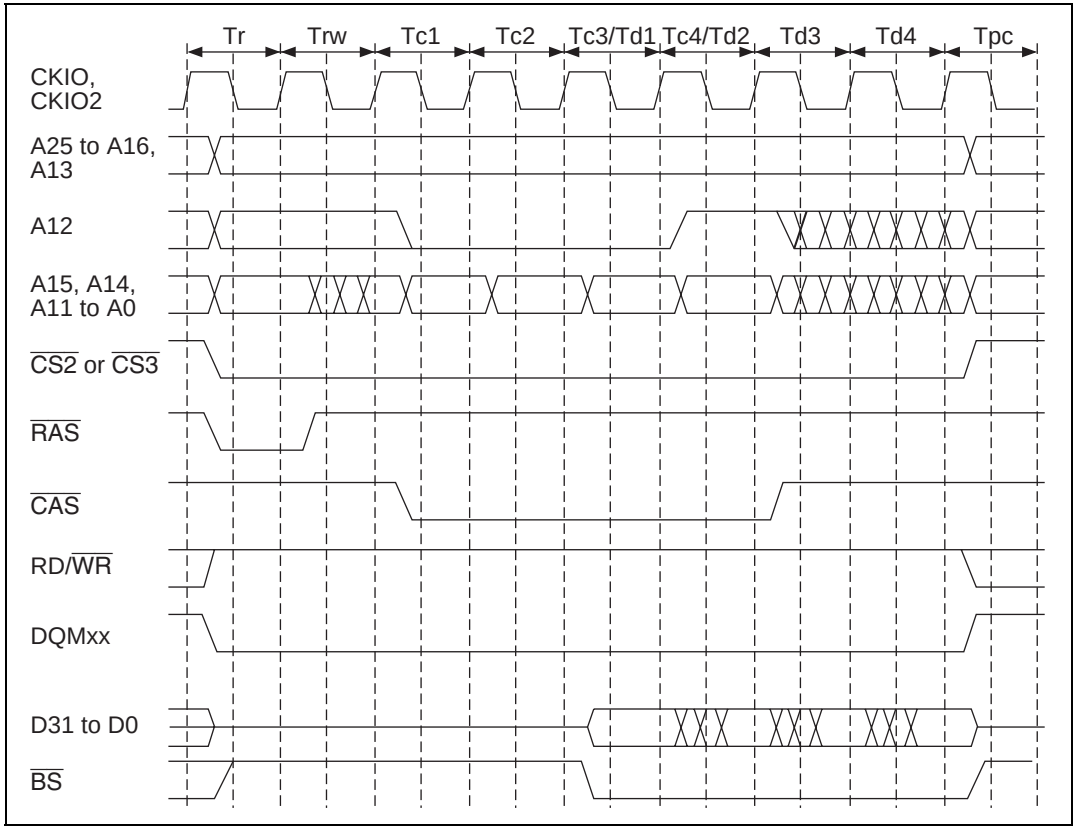


Figure 12.14 Synchronous DRAM Burst Read Wait Specification Timing

Single Read: Figure 12.15 shows the timing when a single address read is performed. As the burst length is set to 1 in synchronous DRAM burst read/single write mode, only the required data is output. Consequently, no unnecessary bus cycles are generated even when a cache-through area is accessed.

Channel	Name	Abbrevi-ation	R/W	Initial Value	Address	Register Size	Access Size
2	DMA source address register 2	SAR2	R/W	Undefined	H'04000040 (H'A4000040)*4	32 bits	16, 32*2
	DMA destination address register 2	DAR2	R/W	Undefined	H'04000044 (H'A4000044)*4	32 bits	16, 32*2
	DMA transfer count register 2	DMATCR2	R/W	Undefined	H'04000048 (H'A4000048)*4	24 bits	16, 32*3
	DMA channel control register 2	CHCR2	R/W*1	H'00000000	H'0400004C (H'A400004C)*4	32 bits	8, 16, 32*2
3	DMA source address register 3	SAR3	R/W	Undefined	H'04000050 (H'A4000050)*4	32 bits	16, 32*2
	DMA destination address register 3	DAR3	R/W	Undefined	H'04000054 (H'A4000054)*4	32 bits	16, 32*2
	DMA transfer count register 3	DMATCR3	R/W	Undefined	H'04000058 (H'A4000058)*4	24 bits	16, 32*3
	DMA channel control register 3	CHCR3	R/W*1	H'00000000	H'0400005C (H'A400005C)*4	32 bits	8, 16, 32*2
Shared	DMA operation register	DMAOR	R/W*1	H'0000	H'04000060 (H'A4000060)*4	16 bits	8, 16*2
	DMA channel assign register	CHRAR	R/W	H'0000	H'0400022A (H'A400022A)*4	16 bits	16

Notes: These registers are located in area 1 of physical space. Therefore, when the cache is on, either access these registers from the P2 area of logical space or else make an appropriate setting using the MMU so that these registers are not cached.

1. Only a write of 0 after a read of 1 to clear a flag is enabled for bit 1 in CHCR0 to CHCR3 and bits 1 and 2 in DMAOR.
2. If SAR0 to SAR3, DAR0 to DAR3, and CHCR0 to CHCR3 are accessed in 16 bits, the 16 bit values that were not accessed are held.
3. DMATCR comprises the 24 bits from bit 0 to bit 23. The upper 8 bits, bits 24 to 31, cannot be written with 1 and are always read as 0.
4. When address translation by the MMU does not apply, the address in parentheses should be used.

Table 14.6 Relationship of Request Modes and Bus Modes

Address Mode	Transfer Areas	Request Mode	Bus Mode	Transfer Size (bits)	Usable Channels
Dual	External device with DACK and external memory	External	B/C	8/16/32/128	0
	External device with DACK and memory-mapped external device	External	B/C	8/16/32/128	0
	External memory and external memory	All*1	B/C	8/16/32/128	0–3*5
	External memory and memory-mapped external device	All*1	B/C	8/16/32/128	0–3*5
	Memory-mapped external device and memory-mapped external device	All*1	B/C	8/16/32/128	0–3*5
	External memory and on-chip supporting module	All*2	B/C*3	8/16/32*4	0–3*5
	Memory-mapped external device and on-chip supporting module	All*2	B/C*3	8/16/32*4	0–3*5
	On-chip supporting module and on-chip supporting module	All*2	B/C*3	8/16/32*4	0–3*5
	X/Y memory and X/Y memory	All	B/C	8/16/32/128	0–3
	X/Y memory and memory-mapped external device	All*1	B/C	8/16/32/128	0–3
	X/Y memory and on-chip supporting module	All*2	B/C*3	8/16/32	0–3
	X/Y memory and external memory	All	B/C	8/16/32/128	0–3
Single	External device with DACK and external memory	External	B/C	8/16/32/128	0
	External device with DACK and memory-mapped external device	External	B/C	8/16/32/128	0

B: Burst

C: Cycle steal

Notes: 1. External requests, auto requests and on-chip supporting module (CMT) requests are all available.

2. External requests, auto requests and on-chip supporting module requests are all available. When the SIOF, USBF, SCIF, or A/D converter is the transfer request source, the transfer destination or transfer source must be also the SIOF, USBF, SCIF, or A/D converter, respectively.

3. The SIOF, USBF, SCIF, or A/D converter can be specified for the transfer request source in the cycle-steal mode only.

4. The access size permitted when the transfer destination or source is an on-chip supporting module register.

5. If the transfer request is an external request, only channel 0 is available.

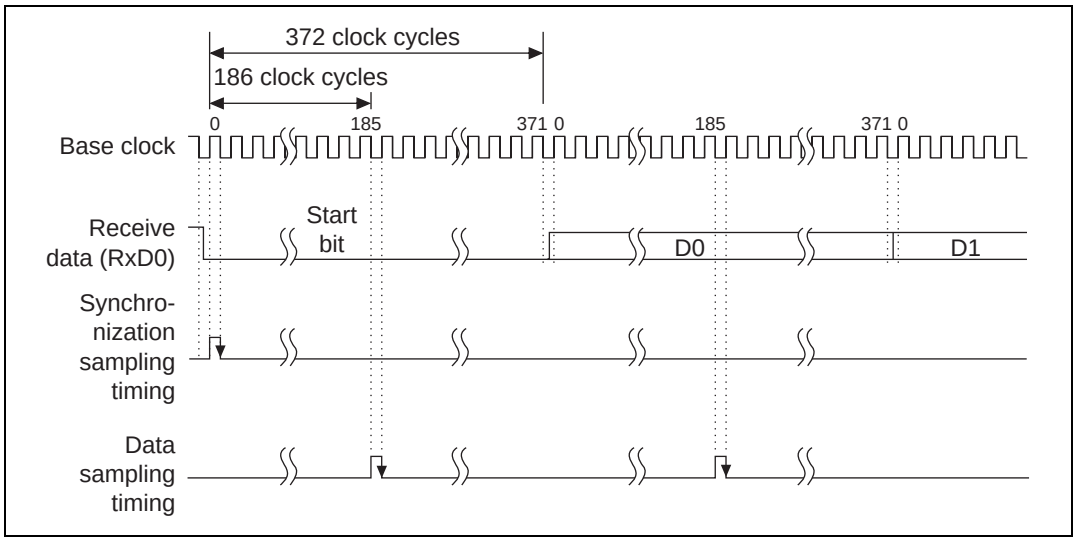


Figure 18.8 Receive Data Sampling Timing in Smart Card Mode

The receive margin is found from the following equation:

For smart card mode:

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F) \right| \times 100\%$$

Where: M = Receive margin (%)
N = Ratio of bit rate to clock (N = 372)
D = Clock duty (D = 0 to 1.0)
L = Frame length (L = 10)
F = Absolute value of clock frequency deviation

Using this equation, the receive margin when F = 0 and D = 0.5 is as follows:

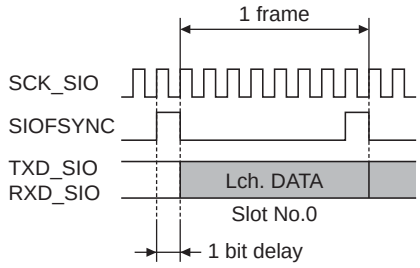
$$M = (0.5 - 1/2 \times 372) \times 100\% = 49.866\%$$

20.3.9 Transmit or Receive Timing

Figures 20.13 to 20.19 show examples of serial transmit or receive of SIOF.

(1) A Case of 8 bits Monaural (No.1)

Sync pulse method, falling edge sampling, transmit data and receive data are assigned to slot No. 0, frame length is 8 bits.

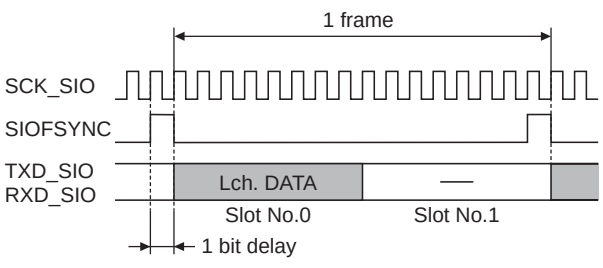


Setting: TRMD = 00 or 10, REDG = 0, FL = 0000 (frame length 16 bits),
TDLE = 1, TDLA3 to TDLA0 = 0000, TDRE = 0, TDRA3 to TDRA0 = 0000,
RDLE = 1, RDLA3 to RDLA0 = 0000, RDRE = 0, RDRA3 to RDRA0 = 0000,
CD0E = 1, CD0A3 to CD0A0 = 0000, CD1E = 0, CD1A3 to CD1A0 = 0000

Figure 20.13 Transmit or Receive Timing (8 bits monaural—1)

(2) A Case of 8 bits Monaural (No.2)

Sync pulse method, falling edge sampling, transmit data and receive data are assigned to slot No.0, frame length is 16 bits.



Setting: TRMD = 00 or 10, REDG = 0, FL = 0100 (frame length 16 bits),
TDLE = 1, TDLA3 to TDLA0 = 0000, TDRE = 0, TDRA3 to TDRA0 = 0000,
RDLE = 1, RDLA3 to RDLA0 = 0000, RDRE = 0, RDRA3 to RDRA0 = 0000,
CD0E = 0, CD0A3 to CD0A0 = 0000, CD1E = 0, CD1A3 to CD1A0 = 0000

Figure 20.14 Transmit or Receive Timing (8 bits monaural—2)

Section 24 USB HOST Module

24.1 General Description

The USB Host Controller module incorporated in SH7727 supports Open Host Controller (Open HCI) Specification for the Universal Serial Bus (USB) as well as the Universal Serial Bus specification ver.1.1.

The Open HCI Specification for the USB is a register-level description of Host Controller for the USB which in turn is described by the USB specification.

It is necessary to refer Open HCI specification to develop drivers for this USB Host Controller and hardware. Also refer to the restrictions on the use of the module listed at the end of this section.

24.1.1 Features

- Support open HCI standard ver.1.0 register set
- Support Universal Serial Bus standard ver.1.1
- Root Hub function
- Support Full speed (12Mbps) mode and Low speed (1.5Mbps) mode
- Support Overcurrent detection
- Support 127 endpoints control in maximum
- The whole area of the synchronous DRAM in area 3 connected to the CPU can be used for transfer data and descriptor.

24.2.2 HcControl

HcControl Register (H'04000404)

The HcControl register defines the operation mode for the host controller. Most of bits of this register are amended only by the host controller driver other than HostController Function State and Remote Wakeup Command.

Register: *HcControl* **Offset: 04–07**

Bits	Reset	R/W	Description
31–11	0h	—	Reserved. Read/Write 0's
10	0b	R/W	**RemoteWakeupEnable (RWE)** This bit is used by HCD to enable/disable the remote wakeup function at the same time as the detection of an upstream resume signal. This function is not supported. Be sure to write 0.
9	0b	R/W	**RemoteWakeupConnected (RWC)** This bit indicates whether the host controller supports a remote wakeup signal or not. When the remote wakeup is supported and used in the system, the host controller must set this bit between POST in the system firmware. The host controller clears the bit at the same time of the hardware reset, however, does not change at the same time as the software reset. The remote wakeup signal to the system of the host is specific for the host bus, so it is not described in this specification. 0: Remote wakeup signal is not supported. (initial value) 1: Remote wakeup signal is supported.
8	0b	R/W	**InterruptRouting (IR)** This bit determines the routing of interrupts generated by the event registered in HcInterruptStatus. HCD clears this bit at the same time as the hardware reset, however, does not clear at the same time as the software reset. HCD uses this bit as a tag to indicate the ownership of the host controller. 0: All interrupts are routed to normal bus interrupt mechanism. (initial value) 1: Interrupts are routed to SMI.

27.5 Ports F, M

Each pin has an input pullup MOS, which is controlled by Ports F, M Control Register (PFDR, PMDR) in PFC.

27.5.1 Ports F, M Data Register (PFDR, PMDR)

Bit:	7	6	5	4	3	2	1	0
	Px7DT	Px6DT	Px5DT	Px4DT	Px3DT	Px2DT	Px1DT	Px0DT
Initial value:	*	*	*	*	*	*	*	*
R/W:	R	R	R	R	R	R	R	R

Note: * Undefined

Ports F, M Data Register (PFDR, PMDR) is an 8-bit read register that stores data for pins PTx7 to PTx0. Px7DT to Px0DT bit corresponds to PTx7 to PTx0 pin. When the pin function is general input port, if the port is read, the corresponding pin level is read. Table 27.4 shows the function of PFDR and PMDR.

PFDR and PMDR are initialized by a power-on reset. After initialization, the general input port function (pullup MOS: on) is set as the initial pin function, and the corresponding pin levels are read.

Table 27.4 Read/Write Operation of the Ports F, M Data Register (PFDR, PMDR)

PxnMD1	PxnMD0	Pin State	Read	Write
0	0	Other function	H'00	Ignored (no affect on pin state)
	1	Reserved*	—	—
1	0	Input (Pullup MOS on)	Pin state	Ignored (no affect on pin state)
	1	Input (Pullup MOS off)	Pin state	Ignored (no affect on pin state)

Note: * Operation cannot be guaranteed when this bit it set to "reserved." (n = 0 to 7)
(x = F, M)

28.4.3 Scan Mode (MULTI = 1, SCN = 1)

Scan mode is useful for monitoring analog inputs in a group of one or more channels including channel 1. When the ADST bit in the A/D control/status register (ADCSR) is set to 1 by software or external trigger input, A/D conversion starts on the first channel in the group (AN2 when CH2 = 0, AN4 when CH2 = 1). When two or more channels are selected, after conversion of the first channel ends, conversion of the second channel (AN3 or AN5) starts immediately. A/D conversion is repeated continuously on the selected channels until the ADST bit is cleared to 0.

The conversion results are transferred for storage into the A/D data registers corresponding to the channels.

When the mode or analog input channel must be changed during analog conversion, to prevent incorrect operation, first clear the ADST bit to 0 to halt A/D conversion. After making the necessary changes, set the ADST bit to 1. A/D conversion will start again from the first channel in the group. The ADST bit can be set at the same time as the mode or channel selection is changed.

Typical operations when three channels (AN4 to AN6) are selected in scan mode are described next. Figure 28.5 shows a timing diagram for this example.

1. Scan mode is selected (MULTI = 1, SCN = 1), channel group 1 is selected (CH2 = 1), analog input channels AN4 to AN6 are selected (CH1 = 1, CH0 = 0), and A/D conversion is started (ADST = 1).
2. When A/D conversion of the first channel (AN4) is completed, the result is transferred into ADDRA. Next, conversion of the second channel (AN5) starts automatically.
3. Conversion proceeds in the same way through the third channel (AN6).
4. When conversion of all the selected channels (AN4 to AN6) is completed, the ADF flag is set to 1 and conversion of the first channel (AN4) starts again. If the ADIE bit is set to 1, an ADI interrupt is requested at this time.
5. Steps 2 to 4 are repeated as long as the ADST bit remains set to 1. When the ADST bit is cleared to 0, A/D conversion stops. After that, if the ADST bit is set to 1, A/D conversion starts again from the first channel (AN4).

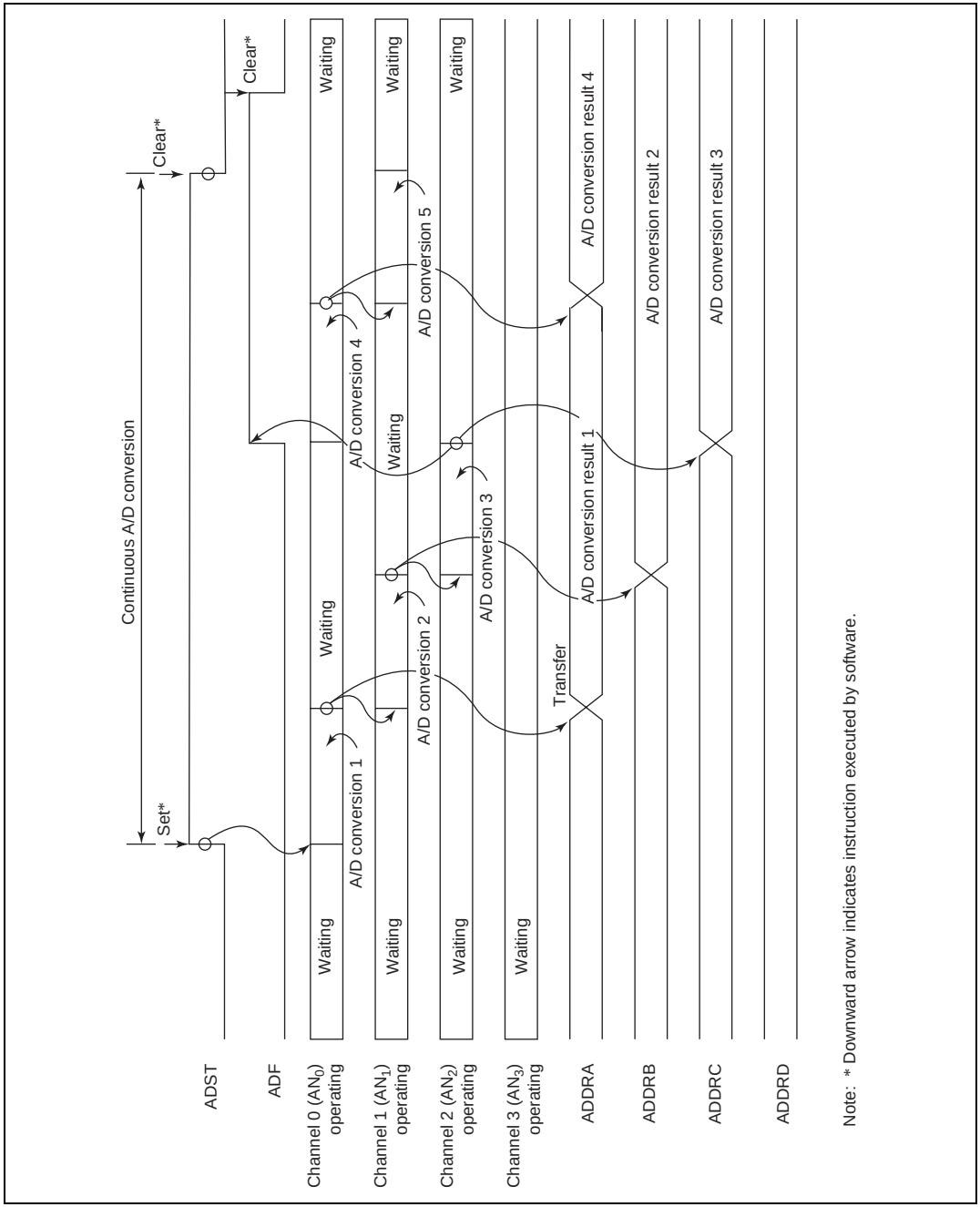


Figure 28.5 Example of A/D Converter Operation (Scan Mode, Channels AN4 to AN6 Selected)

31.4 H-UDI Operations

31.4.1 TAP Controller

Figure 31.2 shows the internal states of TAP controller. State transitions basically conform with the JTAG standard.

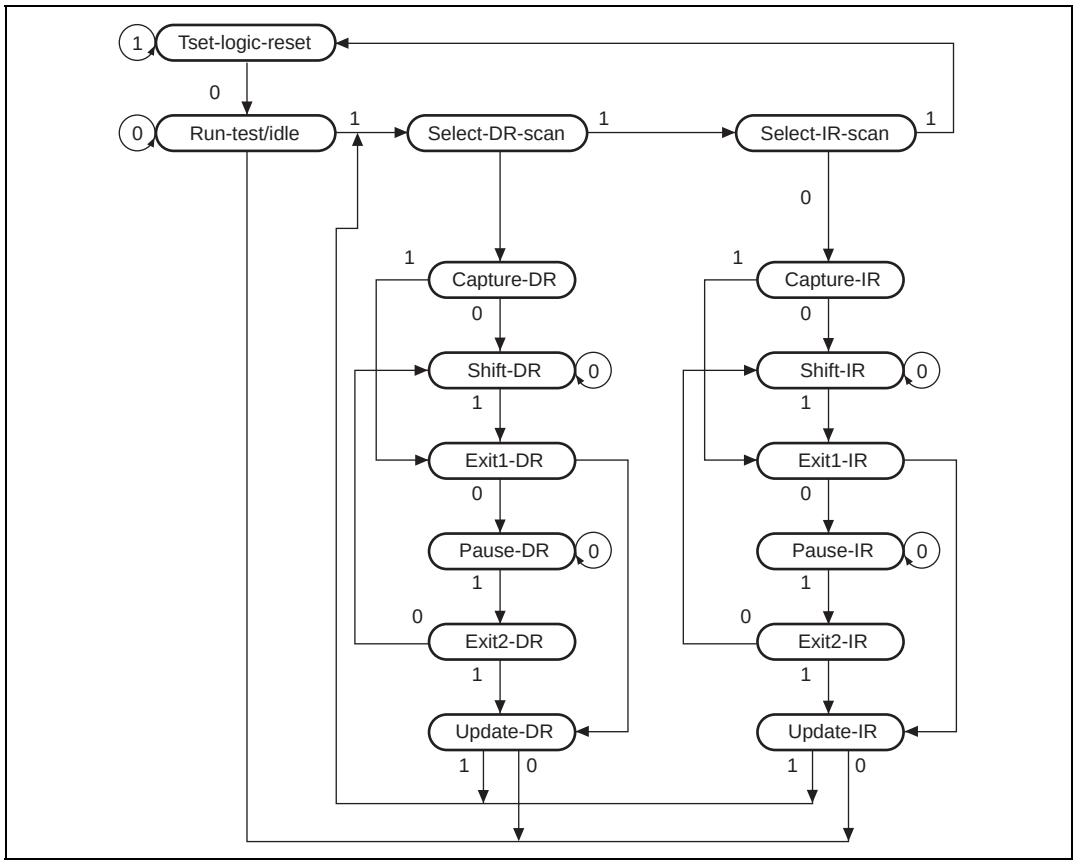


Figure 31.2 TAP Controller State Transitions

Note: The transition condition is the TMS value on the rising edge of TCK. The TDI value is sampled on the rising edge of TCK; shifting occurs on the falling edge of TCK. The TDO value changes on the TCK falling edge. The TDO is at high impedance, except with shift-DR (shift-SR) and shift-IR states. During the change to $\overline{\text{TRST}}$ = 0, there is a transition to test-logic-reset asynchronously with TCK.

Table 32.6 Clock Timing (2)

Conditions: VccQ = 3.0 to 3.6 V, Vcc = 1.70 to 2.05 V, AVcc = 3.3 ± 0.3 V, Ta = –20 to 75°C, 100 MHz products

Item	Symbol	Min	Max	Unit	Figure
EXTAL clock input frequency	f_{EX}	6	50	MHz	32.3
EXTAL clock input cycle time	t_{EXcyc}	20	166.7	ns	
EXTAL clock input low pulse width	t_{EXL}	4	—	ns	
EXTAL clock input high pulse width	t_{EXH}	4	—	ns	
EXTAL clock input rise time	t_{EXR}	—	6	ns	
EXTAL clock input fall time	t_{EXF}	—	6	ns	
CKIO clock input frequency	f_{CKI}	24	50	MHz	32.4
CKIO clock input cycle time	t_{CKIcyc}	20	41.7	ns	
CKIO clock input low pulse width	t_{CKIL}	4	—	ns	
CKIO clock input high pulse width	t_{CKIH}	4	—	ns	
CKIO clock input rise time	t_{CKIR}	—	6	ns	
CKIO clock input fall time	t_{CKIF}	—	6	ns	
CKIO clock output frequency	f_{OP}	24	50	MHz	32.5
CKIO clock output cycle time	t_{cyc}	20	41.7	ns	
CKIO clock output low pulse width	t_{CKOL}	3	—	ns	
CKIO clock output high pulse width	t_{CKOH}	3	—	ns	
CKIO clock output rise time	t_{CKOR}	—	5	ns	
CKIO clock output fall time	t_{CKOF}	—	5	ns	
CKIO2 clock output delay time	t_{CK2D}	—	2.5	ns	
CKIO2 clock output rise time	t_{CK2OR}	—	7	ns	
CKIO2 clock output fall time	t_{CK2OF}	—	7	ns	
Power-on oscillation settling time	t_{OSC1}	10	—	ms	32.6
$\overline{\text{RESETP}}$ setup time (At power on and cancellation of standby mode)	t_{RESPS}	20	—	ns	32.6, 32.7
$\overline{\text{RESETM}}$ setup time (At cancellation of standby mode)	t_{RESMS}	0	—	ns	
$\overline{\text{RESETP}}$ assert time (At power on and cancellation of standby mode)	t_{RESPW}	20	—	t_{cyc}	
$\overline{\text{RESETM}}$ assert time (At cancellation of standby mode)	t_{RESMW}	20	—	t_{cyc}	
Standby return oscillation settling time 1	t_{OSC2}	10	—	ms	32.7
Standby return oscillation settling time 2	t_{OSC3}	10	—	ms	32.8
Standby return oscillation settling time 3	t_{OSC4}	11	—	ms	32.9
PLL synchronization settling time 1 (At cancellation of standby mode)	t_{PLL1}	100	—	µs	32.10, 32.11
PLL synchronization settling time 2 (At multiplier change)	t_{PLL2}	100	—	µs	32.12
IRQ/IRL interrupt determination time (RTC used and standby mode)	t_{IRQSTB}	100	—	µs	32.11

Type	Signal Name (Initial Status: Bold)	Pin No. (HQFP)	I/O	Power-On Reset	Manual Reset	Standby	Release/ Open Bus Privileges
Bus functions	**A0 to A25**	61 to 63, 65, 67 to 74, 76, 78 to 85, 87, 89, 90, 92, 94	O	Z	O	Z(L)	Z
	$\overline{BS}$/PTK[4]	95	O/IO	H	O/P	Z(H)/K	Z/P
	$\overline{RD}$	96	O	H	O	Z(H)	Z
	$\overline{WE0}$/DQMLL	97	O/O	H	O/O	Z(H)/Z(H)	Z/Z
	$\overline{WE1}$/DQMLU/$\overline{WE}$	98	O/O/O	H	O/O/O	Z(H)/Z(H)/ Z(H)	Z/Z/Z
	$\overline{WE2}$/DQMUL/$\overline{ICIORD}$/ PTK[6], **$\overline{WE3}$**/DQMUU/$\overline{ICIOWR}$/ PTK[7]	99, 101	O/O/O/ IO	H	O/O/O/P	Z(H)/Z(H)/ O/K	Z/Z/Z/P
	RDWR	103	O	H	O	Z(H)	Z
	$\overline{CS0}$, $\overline{CS2}$, $\overline{CS3}$	105, 106, 107	O	H	O	Z(H)	Z
	$\overline{CS4}$/PTK[2]	108	O/IO	H	O/P	Z(H)/K	Z/P
	$\overline{CS5}$/$\overline{CE1A}$/PTK[3]	109	O/O/IO	H	O/O/P	Z(H)/Z(H)/ K	Z/Z/P
	$\overline{CS6}$/$\overline{CE1B}$	110	O/O	H	O/O	Z(H)/Z(H)	Z/Z
	$\overline{CE2A}$/**PTE[4],** $\overline{CE2B}$/**PTE[5]**	111, 112	O/IO	V	O/P	Z(H)/K	Z/P
	CKE/PTK[5]	128	O/IO	H	O/P	O/K	O/P
	Reserved/$\overline{CAS}$/PTJ[2]	131	O/O/IO	H	O/O/P	O/Z(H)/K	O/Z(H)/P
	$\overline{WAIT}$	146	I	Z	Z	Z	Z
	$\overline{IOIS16}$/**PTG[7]**	149	I/I	V	I/I	Z/Z(V)	I/I
	$\overline{RAS}$/PTJ[0], **Reserved**/PTJ[1], **Reserved**/PTJ[3]*3, **Reserved**/PTJ[4]*3, **Reserved**/PTJ[5]*3	129, 130, 133, 135, 136	O/IO	H	O/P	Z(H)/K	Z(H)/P
AFE/USB digital/port related	**AFE_HC1**/ USB1d_DPLS/PTK[0]	113	O/I/IO	L	O/I/P	Z/Z/K	O/I/P
	$\overline{AFE\_RLYCNT}$/ USB1d_DMNS/PTK[1]	114	O/I/IO	L	O/I/P	O/Z/K	O/I/P
	AFE_SCLK/ USB1d_TXDPLS	116	I/O	I	I/O	Z/O	I/O

Appendix C Product Lineup

Table C.1 SH7727 Group Product Lineup

Abbreviation	Power Supply Voltages I/O	Power Supply Voltages Internal	Operation Frequency	Model Name	Package
SH7727	3.3±0.3 V	1.7 to 2.05 V	160 MHz	HD6417727F160C	240-pin plastic HQFP (PRQP0240KC-B)
	3.3±0.3 V	1.7 to 2.05 V	160 MHz	HD6417727BP160C	240-pin CSP (PLBG0240JA-A)
	3.1±0.5 V	1.6 to 2.05 V	100 MHz	HD6417727F100C	240-pin plastic HQFP (PRQP0240KC-B)
	3.1±0.5 V	1.6 to 2.05 V	100 MHz	HD6417727BP100C	240-pin CSP (PLBG0240JA-A)