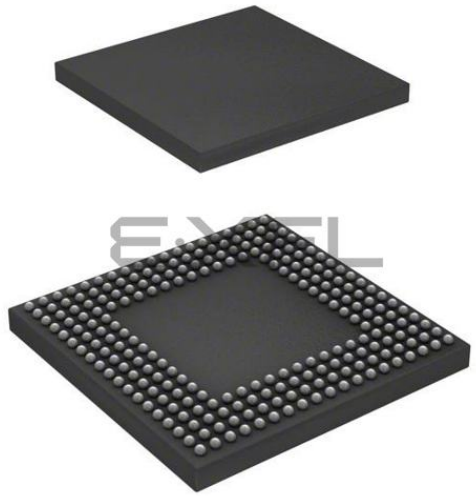

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Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 2.05V
Data Converters	A/D 6x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
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Supplier Device Package	240-LFBGA (13x13)
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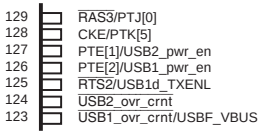
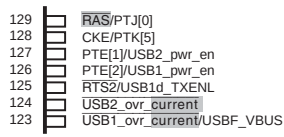
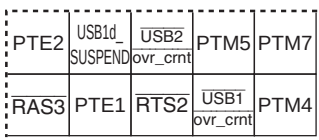
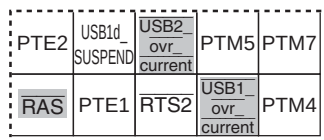
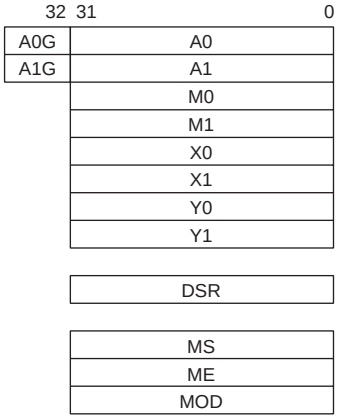
Page	Previous Version	Revised Version
3, 17, 236, 260, 261, 262, 265, 277, 479, 933	Crystal oscillator, (a) crystal oscillation, oscillator	Crystal resonator
9	1.3.1 Pin Arrangement Figure 1.2 Pin Arrangement (PRQP0240KC-B) 	
10	Figure 1.3 Pin Arrangement (PLBG0240JA-A) 	
15, 17, 18	1.3.2 Pin Functions Table 1.2 SH7727 Pin Function Pin No. (PRQP0240KC-B) / Pin No. (PLBG0240JA-A) / Name / I/O / Function 123 / W18 / USB1_ovr_crnt / USBF_VBUS / I/I / USB host 1 overcurrent detection / USB function VBUS 124 / V17 / USB2_ovr_crnt / I / USB host 2 overcurrent detection 129 / W15 / RAS3/PTJ[0] / O/IO / RAS for SDRAM / I/O port J 179 / V4 / XTAL / O / Clock oscillator 224 / G1 / Scan_testen / I / Test pin (fixed to 3.3 V)	Pin No. (PRQP0240KC-B) / Pin No. (PLBG0240JA-A) / Name / I/O / Function 123 / W18 / USB1_ovr_current/ USBF_VBUS / I/I / USB host 1 overcurrent detection / USB function VBUS 124 / V17 / USB2_ovr_current / I / USB host 2 overcurrent detection 129 / W15 / RAS/PTJ[0] / O/IO / RAS for SDRAM / I/O port J 179 / V4 / XTAL / O / Crystal resonator 224 / G1 / Scan_testen / I / Test pin (pull up to VccQ)
278	10.9 Notes on Board Design When Using a PLL Oscillator Circuit: ... In clock mode 7, connect the EXTAL pin to V_{CC} or V_{SS} and leave the XTAL pin open.	... In clock mode 7, connect the EXTAL pin to $V_{CC}Q$ or $V_{SS}Q$ and leave the XTAL pin open.
286	12.1.3 Pin Configuration Table 12.1 Pin Configuration Pin Name / Signal / I/O / Description Row address strobe 3 / RAS3 / Output / When synchronous DRAM is used in area 3, RAS3 for 64-Mbyte address. Column address strobe / CAS / Output / When synchronous DRAM is used, CAS signal is used for 64-Mbyte address.	Pin Name / Signal / I/O / Description Row address strobe / RAS / Output / When synchronous DRAM is used, RAS signal. Column address strobe / CAS / Output / When synchronous DRAM is used, CAS signal



(d) DSP mode register configuration (DSP = 1)

Figure 2.2 Register Configuration in Each Processing Mode (2)

Register values after a reset are shown in table 2.1.

Table 2.1 Initial Register Values

Type	Registers	Initial Value*
General registers	R0 to R15	Undefined
Control registers	SR	MD bit = 1, RB bit = 1, BL bit = 1, I3 to I0 = 1111 (H'F), reserved bits = 0, others undefined
	GBR, SSR, SPC	Undefined
	VBR	H'00000000
	RS, RE	Undefined
	MOD	Undefined
System registers	MACH, MACL, PR	Undefined
	PC	H'A0000000
DSP registers	A0, A0G, A1, A1G, M0, M1, X0, X1, Y0, Y1	Undefined
	DSR	H'00000000

Note: * Initialized by a power-on or manual reset.

Table 2.28 Single Data Transfer Instructions

Instruction	Instruction Code	Operation	Execution States	DC
MOVS.W @-As,Ds	111101AADDDD0000	As – 2 → As, (As) → MSW of Ds, 0 → LSW of Ds	1	—
MOVS.W @As,Ds	111101AADDDD0100	(As) → MSW of Ds, 0 → LSW of Ds	1	—
MOVS.W @As+,Ds	111101AADDDD1000	(As) → MSW of Ds, 0 → LSW of Ds, As + 2 → As	1	—
MOVS.W @As+Ix,Ds	111101AADDDD1100	(Asc) → MSW of Ds, 0 → LSW of Ds, As + Ix → As	1	—
MOVS.W Ds,@-As*	111101AADDDD0001	As – 2 → As, MSW of Ds → (As)	1	—
MOVS.W Ds,@As*	111101AADDDD0101	MSW of Ds → (As)	1	—
MOVS.W Ds,@As+*	111101AADDDD1001	MSW of Ds → (As), As + 2 → As	1	—
MOVS.W Ds,@As+Ix*	111101AADDDD1101	MSW of Ds → (As), As + Ix → As	1	—
MOVS.L @-As,Ds	111101AADDDD0010	As – 4 → As, (As) → Ds	1	—
MOVS.L @As,Ds	111101AADDDD0110	(As) → Ds	1	—
MOVS.L @As+,Ds	111101AADDDD1010	(As) → Ds, As + 4 → As	1	—
MOVS.L @As+Ix,Ds	111101AADDDD1110	(As) → Ds, As + Ix → As	1	—
MOVS.L Ds,@-As	111101AADDDD0011	As – 4 → As, Ds → (As)	1	—
MOVS.L Ds,@As	111101AADDDD0111	Ds → (As)	1	—
MOVS.L Ds,@As+	111101AADDDD1011	Ds → (As), As + 4 → As	1	—
MOVS.L Ds,@As+Ix	111101AADDDD1111	Ds → (As), As + Ix → As	1	—

Note: * If guard bit registers A0G and A1G are specified in source operand Ds, the data is output to the LDB[7:0] bus and the sign bit is copied into the upper bits, [31:8].

3.3.2 TLB Indexing

The TLB uses a 4-way set associative scheme, so entries must be selected by index. VPN bits 16 to 12 and ASID bits 4 to 0 in PTEH are used as the index number. The index number can be generated in two different ways depending on the setting of the IX bit in MMUCR.

1. When IX = 0, VPN bits 16 to 12 alone are used as the index number
2. When IX = 1, VPN bits 16 to 12 are EX-ORed with ASID bits 4 to 0 to generate the index number

The method 1 is used to prevent lowered TLB efficiency that results when multiple processes run simultaneously in the same logical address space (multiple virtual memory) and a specific entry is selected by indexing of each process. Figures 3.6 and 3.7 show the indexing schemes.

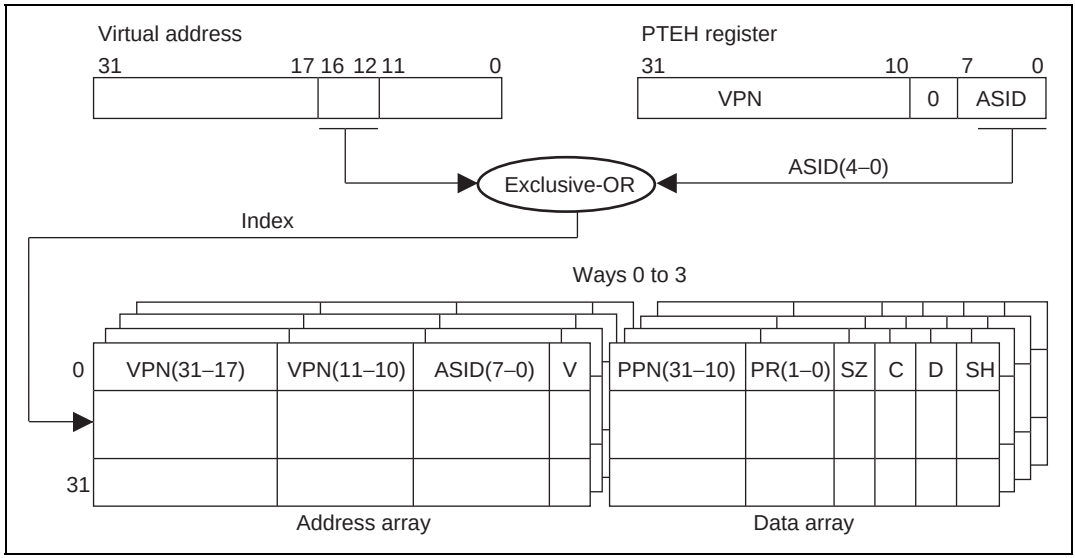


Figure 3.6 TLB Indexing (IX = 1)

7.3.5 Interrupt Control Register 3 (ICR3)

The ICR3 is a 16-bit read/write register that sets the mask to PC Card controller. This register is initialized to H'0000 at power-on reset or manual reset, but is not initialized in standby mode.

Bit:	15	14	13	12	11	10	9	8
	—	PC0SWIM	PC0IRIM	PC0SCIM	PC0CDIM	PC0RCIM	PC0BWIM	PC0BDIM
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 15—Reserved: This bit is always read as 0. The write value should always be 0.

Bit 14—PC0SWIM: PC Card controller0 SWI mask.

Bit 14: PC0SWIM	Description	
0	Interrupt requests is masked	(Initial value)
1	Interrupt requests is not masked	

Bit 13—PC0IRIM: PC Card controller0 IRI mask.

Bits 13: PC0IRIM	Description	
0	Interrupt requests is masked	(Initial value)
1	Interrupt requests is not masked	

Bit 12—PC0SCIM: PC Card controller0 SCI mask.

Bit 12: PC0SCIM	Description	
0	Interrupt requests is masked	(Initial value)
1	Interrupt requests is not masked	

Bit 5—USBF1I Interrupt Request (USBF1IR): Indicates whether a USBF1I (USB function) interrupt request is generated.

Bit 5: USBF1IR	Description	
0	A USBF1I interrupt request is not generated	(Initial value)
1	A USBF1I interrupt request is generated	

Bit 4—AFEIFI Interrupt Request (AFEIFIR): Indicates whether a AFEIFI (AFE I/F) interrupt request is generated.

Bit 4: AFEIFIR	Description	
0	An AFE I/F interrupt request is not generated	(Initial value)
1	An AFE I/F interrupt request is generated	

Bits 3 to 0—Reserved: These bits are always read as 0.

7.3.11 Interrupt Request Register 4 (IRR4)

The IRR4 is a 16-bit read-only register that indicates whether SIOF interrupt requests are generated. This register is initialized to H'0000 at power-on reset or manual reset, but is not initialized in standby mode.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	ERI	TXI	RXI	CCI
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bits 15 to 4—Reserved: These bits are always read as 0. The write value should always be 0.

7.4 INTC Operation

7.4.1 Interrupt Sequence

The sequence of interrupt operations is explained below. Figure 7.3 is a flowchart of the operations.

1. The interrupt request sources send interrupt request signals to the interrupt controller.
2. The interrupt controller selects the highest priority interrupt from the interrupt requests sent, following the priority levels set in interrupt priority registers A to G (IPRA to IPRG). Lower priority interrupts are held pending. If two of these interrupts have the same priority level or if multiple interrupts occur within a single module, the interrupt with the highest default priority or the highest priority within its IPR setting unit (as indicated in tables 7.4 and 7.5) is selected.
3. The priority level of the interrupt selected by the interrupt controller is compared with the interrupt mask bits (I3 to I0) in the status register (SR) of the CPU. If the request priority level is higher than the level in bits I3 to I0, the interrupt controller accepts the interrupt and sends an interrupt request signal to the CPU.
4. Detection timing: The INTC operates, and notifies the CPU of interrupt requests, in synchronization with the peripheral clock (Pϕ). The CPU receives an interrupt at a break in instructions.
5. The interrupt source code is set in the interrupt event registers (INTEVT and INTEVT2).
6. The status register (SR) and program counter (PC) are saved to SSR and SPC, respectively.
7. The block bit (BL), mode bit (MD), and register bank bit (RB) in SR are set to 1.
8. The CPU jumps to the start address of the interrupt handler (the sum of the value set in the vector base register (VBR) and H'00000600). This jump is not a delayed branch. The interrupt handler may branch with the INTEVT and INTEVT2 register value as its offset in order to identify the interrupt source. This enables it to branch to the processing routine for the individual interrupt source.

Notes: 1. The interrupt mask bits (I3 to I0) in the status register (SR) are not changed by acceptance of an interrupt in the SH7727.

2. The interrupt source flag should be cleared in the interrupt handler. To ensure that an interrupt request that should have been cleared is not inadvertently accepted again, read the interrupt source flag after it has been cleared, then wait for the interval shown in table 7.8 (Time for priority decision and SR mask bit comparison) before clearing the BL bit or executing an RTE instruction.

12.2 BSC Registers

12.2.1 Bus Control Register 1 (BCR1)

Bus control register 1 (BCR1) is a 16-bit read/write register that sets the functions and bus cycle state for each area. It is initialized to H'0000 by a power-on reset, but is not initialized by a manual reset or by standby mode. Do not access external memory outside area 0 until BCR1 register initialization is complete.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PULA	PULD	HIZ MEM	HIZ CNT	ENDI AN	A0 BST1	A0 BST0	A5 BST1	A5 BST0	A6 BST1	A6 BST0	DRAM TP2	DRAM TP1	DRAM TP0	A5 PCM	A6 PCM
Initial value:	0	0	0	0	0/1*	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Samples the value of the external pin (MD5) designating endian at power-on reset.

Bit 15—Pins A25 to A0 Pull-Up (PULA): Specifies whether or not pins A25 to A0 are pulled up for 4 cycles immediately after $\overline{\text{BACK}}$ is asserted.

Bit 15: PULA	Description	
0	Not pulled up	(Initial value)
1	Pulled up	

Bit 14—Pins D31 to D0 Pull-Up (PULD): Specifies whether or not pins D31 to D0 are pulled up when not in use.

Bit 14: PULD	Description
0	Not pulled up (Initial value)
1	Pulled up

Bit 13—Hi-Z memory control (HIZMEM): Specifies the state of A25 to A0, $\overline{\text{BS}}$, $\overline{\text{CS}}$, RD/$\overline{\text{WR}}$, $\overline{\text{WE}}$/DQM, $\overline{\text{RD}}$, $\overline{\text{CE2A}}$, $\overline{\text{CE2B}}$ and DRAK0 in standby mode.

Bit 13: HIZMEM	Description	
0	High-impedance state in standby mode.	(Initial value)
1	High in standby mode.	

12.2.3 Wait State Control Register 1 (WCR1)

Wait state control register 1 (WCR1) is a 16-bit read/write register that specifies the number of idle (wait) state cycles inserted for each area. For some memories, the drive of the data bus may not be turned off quickly even when the read signal from the external device is turned off. This can result in conflicts between data buses when consecutive memory accesses are to different memories or when a write immediately follows a memory read. This LSI automatically inserts idle states equal to the number set in WCR1 in those cases.

WCR1 is initialized to H'3FF3 by a power-on reset. It is not initialized by a manual reset or by standby mode.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WAIT SEL	—	A6 IW1	A6 IW0	A5 IW1	A5 IW0	A4 IW1	A4 IW0	A3 IW1	A3 IW0	A2 IW1	A2 IW0	—	—	A0 IW1	A0 IW0
Initial value:	0	0	1	1	1	1	1	1	1	1	1	1	0	0	1	1
R/W:	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W

Bit 15—WAIT Sampling Timing Select (WAITSEL): Specifies the $\overline{\text{WAIT}}$ signal sampling timing.

Bit 15: WAITSEL	Description	
0	Set to 1 when $\overline{\text{WAIT}}$ signal is used.*	(Initial value)
1	Sampled at the falling edge of CKIO.	

Note: * If low level is input to the $\overline{\text{WAIT}}$ by setting the WAITSEL bit, the LSI operation cannot be guaranteed.

Bits 14, 3, and 2 —Reserved: These bits are always read as 0. The write value should always be 0.

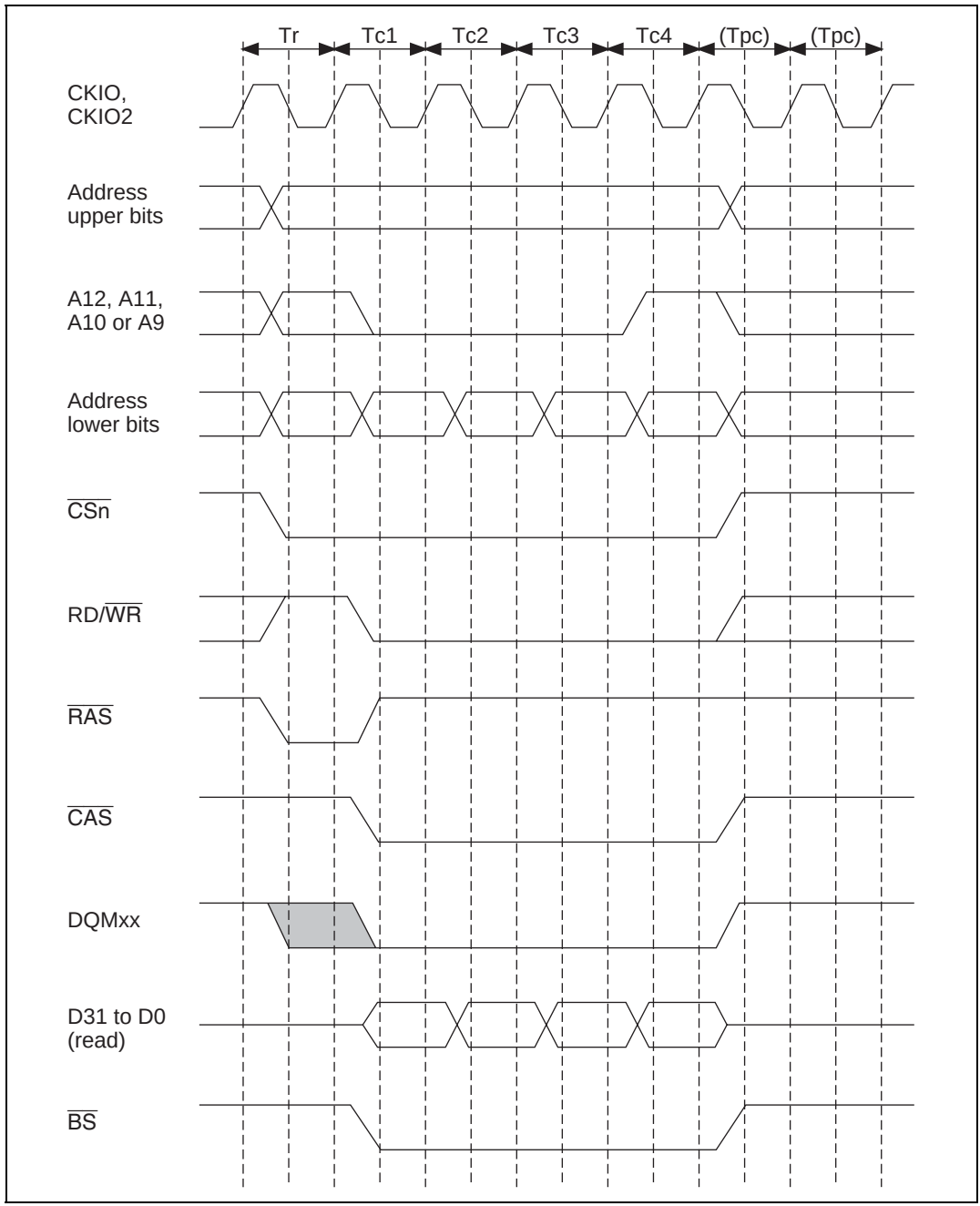


Figure 12.16 Basic Timing for Synchronous DRAM Burst Write

13.2 LBSC Operation

13.2.1 Bus Sharing Architecture

LCDC and USB Host Controller can share the system memory with CPU and DMA Controller, so these bus masters are able to work without any independent external memory and have huge available memory space up to 64 Mbyte at area 3.

Since each LCDC, USB Host Controller, CPU, and DMA Controller can access area 3 individually. Set addresses for each controller to avoid address sharing.

13.2.2 Usable System Memory

LBSC works at below memories.

Memory area	Area3
Memory type	Synchronous DRAM
Bus width	16 or 32 bits
Burst length	1 to 4 burst (USBH)
	4 to 32 burst (LCDC) with 32-bit bus width, 8 to 64 burst (LCDC) with 16-bit bus width

13.2.3 Bus Arbitration

LBSC accepts a request that comes from LCDC or USB Host at a same time without any prioritization to each module. LBSC tries to get bus right from BSC at any time when it get a request from LCDC or USB Host. Once BSC gives LBSC a right, LCDC or BSC can access external memory directly. The arbiter of LBSC gives a bus right to LCDC or USB Host as even.

13.2.4 LCDC Li Bus Access

While displaying images, the LCDC continuously reads data from the system memory with a 32 burst length. The LCDC burst length is specified by a register in the LCDC. If the data length is shorter than 32 burst length, such as the case for the edge of LCD panel, the LCDC uses a shorter burst length.

• Single Address Mode

The single address mode is used when transfer is performed between external devices including external memories, one of which is accessed (selected) by the DACK signal and the other of which is accessed by address. In this mode, the DMAC outputs the transfer request acknowledge signal DACK to one external device, and simultaneously outputs an address to the other device; thus DMA transfer is performed in one bus cycle. An example of transfer between an external memory and an external device with DACK is shown in figure 14.11. The external device outputs data to a data bus and the data is written to the external memory in a single bus cycle.

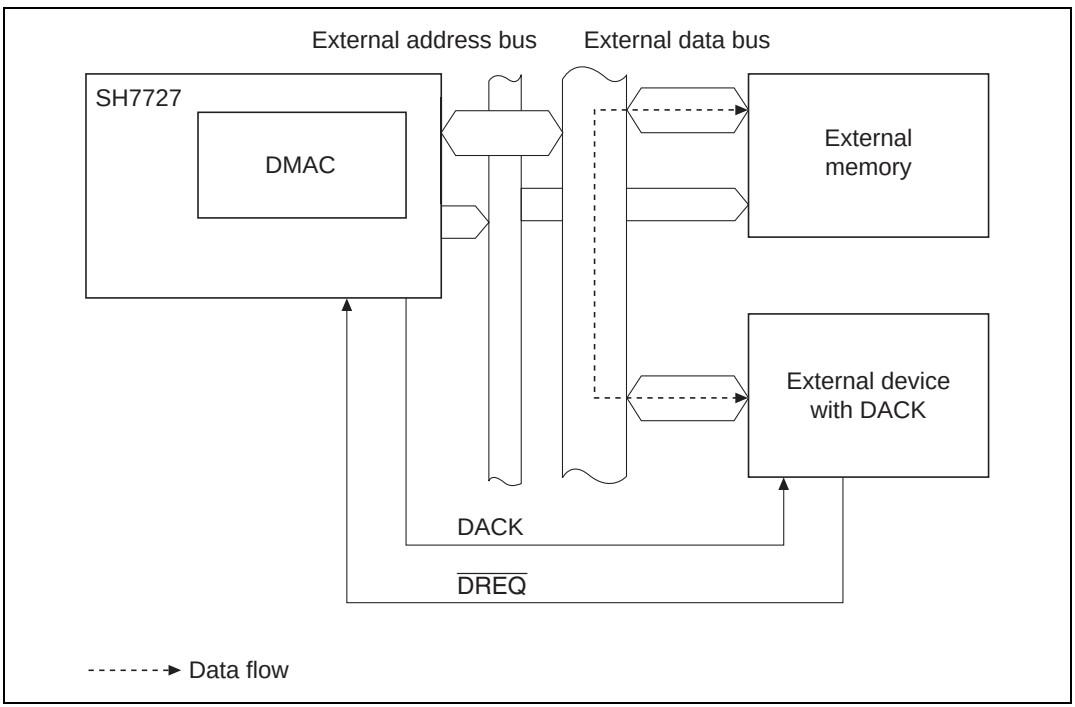


Figure 14.11 Data Flow in Single Address Mode

Two kinds of transfer are possible in single address mode: (1) transfer between an external device with DACK and a memory-mapped external device, and (2) transfer between an external device with DACK and an external memory. In both cases, only the external request signal ($\overline{\text{DREQ}}$) is used as a transfer request.

Figures 14.12 and 14.13 show examples of the DMA transfer timing in single address mode.

14.3.7 DMA Transfer Ending

DMA transfer ending conditions to terminate transfer differ according to the ending types, individual channel ending and all channel ending. At a transfer end, the following conditions are applied except the case when the DMA transfer count register (DMATCR) value reaches 0.

(a) Cycle-steal mode (external request, internal request, and auto request)

When a transfer ending condition is satisfied, DMAC transfer request acceptance is suspended. The DMAC stops operation after completing the number of transfers that has accepted before the ending conditions are satisfied.

In the cycle-steal mode, the same operation is provided regardless of the transfer request detection method; the level detection or the edge detection.

(b) Burst mode, edge detection (external request, internal request, and auto request)

The timing of DMAC operation ending after an ending condition is satisfied differs from that in cycle steal mode. In the edge detection in the burst mode, though only one transfer request is generated at the DMAC start-up, a stop request sampling is performed in the same timing as a transfer request sampling in the cycle-steal mode. As a result, the period when a stop request is not sampled is regarded as the period when a transfer request is generated, and after performing the DMA transfer for this period, the DMAC stops operation.

(c) Burst mode, level detection (external request)

Same as described in (a).

(d) Bus timing when transfers are suspended

Transfer is suspended when one transfer ends. Even if a transfer ending condition is satisfied during a read with the direct address transfer in the dual address mode, the subsequent write process is executed, and after the transfer in (a) to (c) above has been executed, DMAC operation suspends.

Bit 1—Reserved: This is a readable/writable bit, but the write value should be always be 0.

Bit 0—Count start 0 (STR0): Selects whether the compare-match timer counter 0 is operated or halted.

Bit 0: STR0	Description	
0	CMCNT0 count operation is halted	(Initial value)
1	CMCNT0 count operation is provided	

Compare-Match Timer Control/Status Register 0 (CMCSR0)

The compare-match timer control/status register 0 (CMCSR0) is a 16-bit register that indicates a compare-match occurrence and sets the incrementation clock. CMCSR0 is initialized to H'0000 by a reset, but it retains its previous values in standby mode.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	7	6	5	4	3	2	1	0
	CMF	—	—	—	—	—	CKS1	CKS0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/W	R	R	R	R	R/W	R/W

Note: * Only a 0 can be written, to clear the flag.

Bits 15 to 8 and 5 to 2—Reserved: These bits are always read as 0and should only be written with 0.

Bit 7—Compare-Match Flag (CMF): This flag indicates that a compare-match of the compare-match timer counter 0 (CMCNT0) and compare-match constant register 0 (CMCOR0) occurred.

Bit 7: CMF	Description	
0	CMCNT0 and CMCOR0 have not matched Clear condition: Write 0 to CMF after reading CMF = 1	(Initial value)
1	A compare-match of CMCNT0 and CMCOR0 occurred	

Bit 6—Reserved: This is a readable/writable bit, but the write value should be always be 0.

(7) A Case of bits Monaural (No. 2)

Sync pulse method, falling edge sampling and secondary FS are requested, Lch. data is assigned to slot No. 0, control ch. data 0 are assigned to slot No. 0, and frame length is 128 bits.

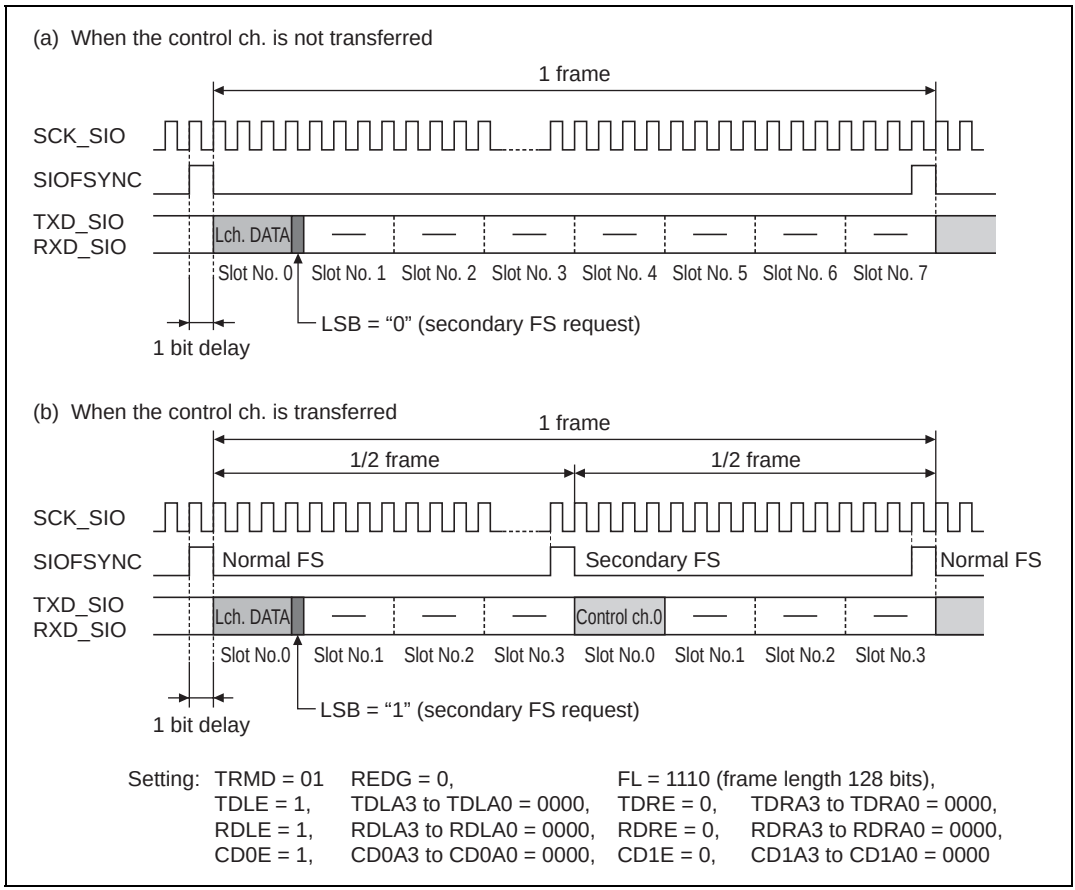


Figure 20.19 Transmit or Receive Timing (16 bits monaural—2)

At that time, make sure to set the watermark value so as not to receive FIFO full nor overflow when receive operation.

Example: When 12 empty slots are set to receive FIFO, read 12 data from receive FIFO with DMA auto request by receive FIFO transfer interrupt (SIFRXI).

Etc.

(1) Not to use DMA 16 bytes transfer. (See section 14.3.4, DMA Transfer Types.)

(2) Recommend DMA auto request for SIOF access. When from CPU, not to use continuous access.

(3) When newly use SIOF after transmit/receive operation, proceed transfer operation after transmit reset (TXRST) or receive reset (RXRST).

Bit 12—Vsync Interrupt Select (VINTSEL): Sets the starting point of the LCDC's Vsync interrupt.

Bit 12 VINTSEL	Description
0	Vsync interrupt is generated at starting point of vertical retrace period for memory access (Initial value)
1	Vsync interrupt is generated at starting point of vertical retrace period for LCD display

Bit 8—Vsync Interrupt Enable (VINTE): Sets whether or not to enable LCDC's Vsync interrupts.

Bit 8 VINTE	Description
0	Vsync interrupts are disabled (Initial value)
1	Vsync interrupts are enabled

Bit 0—Vsync Interrupt State (VINTS): Indicates the LCDC's Vsync interrupt handling state. This bit is set to 1 at the time a Vsync interrupt is generated. During the Vsync interrupt handling routine, this bit should be cleared by writing 0 to it.

Bit 0 VINTS	Description
0	LCDC did not generate a Vsync interrupt or has been informed that the generated Vsync interrupt has completed (Initial value)
1	LCDC has generated a Vsync interrupt and has not yet been informed that the generated Vsync interrupt has completed

Notes: • Interrupt Handling Flow:

1. An interrupt signal is input to the CPU.
2. The CPU reads from VINTS.
3. If VINTS is set to 1, a Vsync interrupt has occurred, and the Vsync interrupt handling is carried out.
4. If VINTS is cleared to 0, no Vsync interrupt has occurred and another processing is carried out.

• When Vsync interrupts are enabled, the VINTE bit must be set to 1 before the DON bit is set to 1, and the VINTE bit must not be cleared to 0.

Table 25.6 LCDC Operating Modes

Mode		Function
Display on (LCDC active)	Register setting: DON = 1 DON = 2	Fixed resolution, the format of the data for display is determined by the number of colors, timing signals are output to the LCD module.
Display off (LCDC stopped)	Register setting: DON = 0 DON2 = 0	Register access is enabled. Fixed resolution, the format of the data for display is determined by the number of colors, timing signals are not output to the LCD module.

Table 25.7 LCD Module Power-Supply States

(STN, DSTN module)

State	Power Supply for Logic	Display Data, Timing Signal	Power Supply for High-Voltage Systems	DON Signal
Control Pin	VCPWC	CL2, CL1, FLM, M/DISP, LCD	VEPWC	DON
Operating State	Supply	Supply	Supply	Supply
(Transitional State)	Supply	Supply	Supply	
	Supply	Supply		
	Supply			
Stopped State				

(TFT module)

State	Power Supply for Logic	Display Data, Timing Signal	Power Supply for High-Voltage Systems
Control Pin	VCPWC	CL2, CL1, FLM, M/DISP, LCD	VEPWC
Operating State	Supply	Supply	Supply
(Transitional State)	Supply	Supply	
	Supply		
Stopped State			

26.3.4 Port D Control Register (PDCR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PD7 MD1	PD7 MD0	PD6 MD1	PD6 MD0	PD5 MD1	PD5 MD0	PD4 MD1	PD4 MD0	PD3 MD1	PD3 MD0	PD2 MD1	PD2 MD0	PD1 MD1	PD1 MD0	PD0 MD1	PD0 MD0
Initial value:	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Port D Control Register (PDCR) is a 16-bit read/write register that selects the pin functions. PDCR is initialized to H'AAAA by power-on resets; however, it is not initialized by manual resets, in standby mode, or in sleep mode.

Bits 15, 14: PD7 Mode 1, 0 (PD7MD1, PD7MD0)
Bits 13, 12: PD6 Mode 1, 0 (PD6MD1, PD6MD0)
Bits 11, 10: PD5 Mode 1, 0 (PD5MD1, PD5MD0)
Bits 9, 8: PD4 Mode 1, 0 (PD4MD1, PD4MD0)
Bits 7, 6: PD3 Mode 1, 0 (PD3MD1, PD3MD0)
Bits 5, 4: PD2 Mode 1, 0 (PD2MD1, PD2MD0)
Bits 3, 2: PD1 Mode 1, 0 (PD1MD1, PD1MD0)
Bits 1, 0: PD0 Mode 1, 0 (PD0MD1, PD0MD0)
These bits select the pin functions and the input pullup MOS control.

Bit (2n + 1)	Bit 2n	
PDnMD1	**PDnMD0**	**Pin Function**
0	0	Other function (see table 26.1)
0	1	Port output (n = value other than 4 or 6), reserved (n = 4 or 6)
1	0	Port input (Pullup MOS: on) (Initial value)
1	1	Port input (Pullup MOS: off)

(n = 0 to 7)

5. With 16-bit access, it is not possible to read data in two registers simultaneously.
6. With 32-bit access, it is not possible to read data in the register at [accessed address + 2] simultaneously.