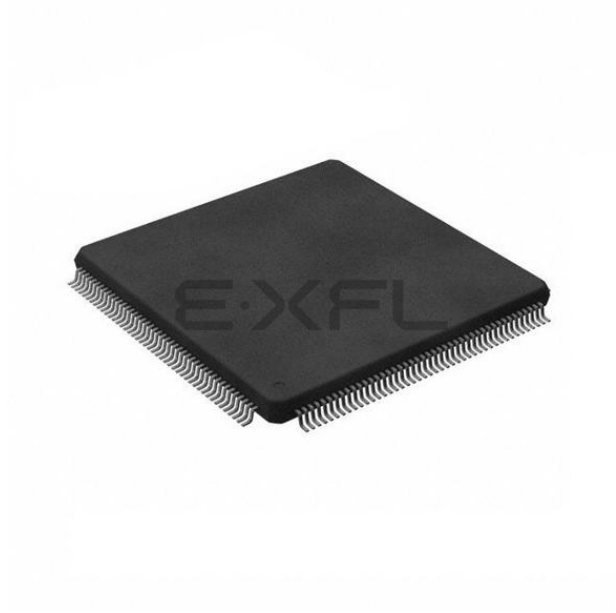

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, CSIO, EBI/EMI, Ethernet, I²C, LINbus, SmartCard, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	153
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2g26jhagv2000a

S6E2G Series

32-bit ARM® Cortex®-M4F FM4 Microcontroller

S6E2G Series are FM4 devices with up to 180 MHz CPU, 1 MB flash, 192 KB SRAM, 20x communication peripherals, 33x digital peripherals and 3x analog peripherals. They are designed for industrial automation and metering applications.

Devices in the S6E2G Series are highly integrated 32-bit microcontrollers with high performance and competitive cost. This series is based on the ARM Cortex-M4F processor with on-chip flash memory and SRAM. The series has peripherals such as motor control timers, A/D converters, and communications interfaces (USB, CAN, UART, CSIO (SPI), I^2C, LIN). The products that are described in this data sheet are placed into TYPE5-M4 product categories in the "FM4 Family Peripheral Manual Main Part (002-04856)".

- 32-bit ARM Cortex-M4F Core
  - Up to 180 MHz frequency operation
- On-chip Memories
  - Flash memory: Up to 1024 Kbytes
  - SRAM memory:
    - SRAM0: up to 128 Kbytes
    - SRAM1: 32 Kbytes
    - SRAM2: 32 Kbytes
- Direct Memory Access (DMA) Controller (Eight Channels)
- Descriptor System Data Transfer Controller (DSTC); 256 channels
- External Bus Interface
- USB Interface (Max two channels): Host and Device
- CAN Interface (Max one channel) Available on S6E2GM and S6E2GH Devices Only
- Multi-function Serial Interface (Max 10 Channels)
  - UART (Universal Asynchronous Receiver/Transmitter)
  - Clock Synchronous Serial Interface (CSIO (SPI))
  - Local Interconnect Network (LIN)
  - Inter-Integrated Circuit (I^2C)
  - Inter-IC Sound (I^2S)
- Base Timer (Max 16 channels)
- General Purpose I/O Port
  - Up to 121 high-speed general-purpose I/O ports in 144-pin package
  - Up to 153 high-speed general-purpose I/O ports in 176-pin package
- Multi-function Timer (Max two units)
- Real-Time Clock (RTC)
- Analog to Digital Converter (ADC) (Max 32 Channels)
- Dual Timer (32-/16-bit Down Counter)
- Quadrature Position/Revolution Counter (QPRC; Max two channels)
- Watch Counter
- External Interrupt Controller Unit
- Watchdog Timer (Two channels)
- Cyclic Redundancy Check (CRC) Accelerator
- SD Card Interface Available on S6E2GM, S6E2GH, and S6E2GK Devices Only
- Ethernet-MAC Available on S6E2GM, S6E2GK, and S6E2G2 Devices only
- Smartcard Interface (Max 2 channels)
- Five Clock Sources
- Six Reset Sources
- Clock Supervisor (CSV)
- Low-Voltage Detector (LVD)
- Six Low-power Consumption Modes
  - Sleep
  - Timer
  - RTC
  - Stop
  - Deep standby RTC
  - Deep standby stop
- Peripheral Clock Gating System
- Crypto Assist Function
- Debug
  - Serial wire JTAG debug port (SWJ-DP)
  - Embedded trace macrocells (ETM) provide comprehensive debug and trace facilities.
  - AHB trace macrocells (HTM)
- 41-bit Unique ID
- Wide range voltage: VCC = 2.7 to 5.5 V

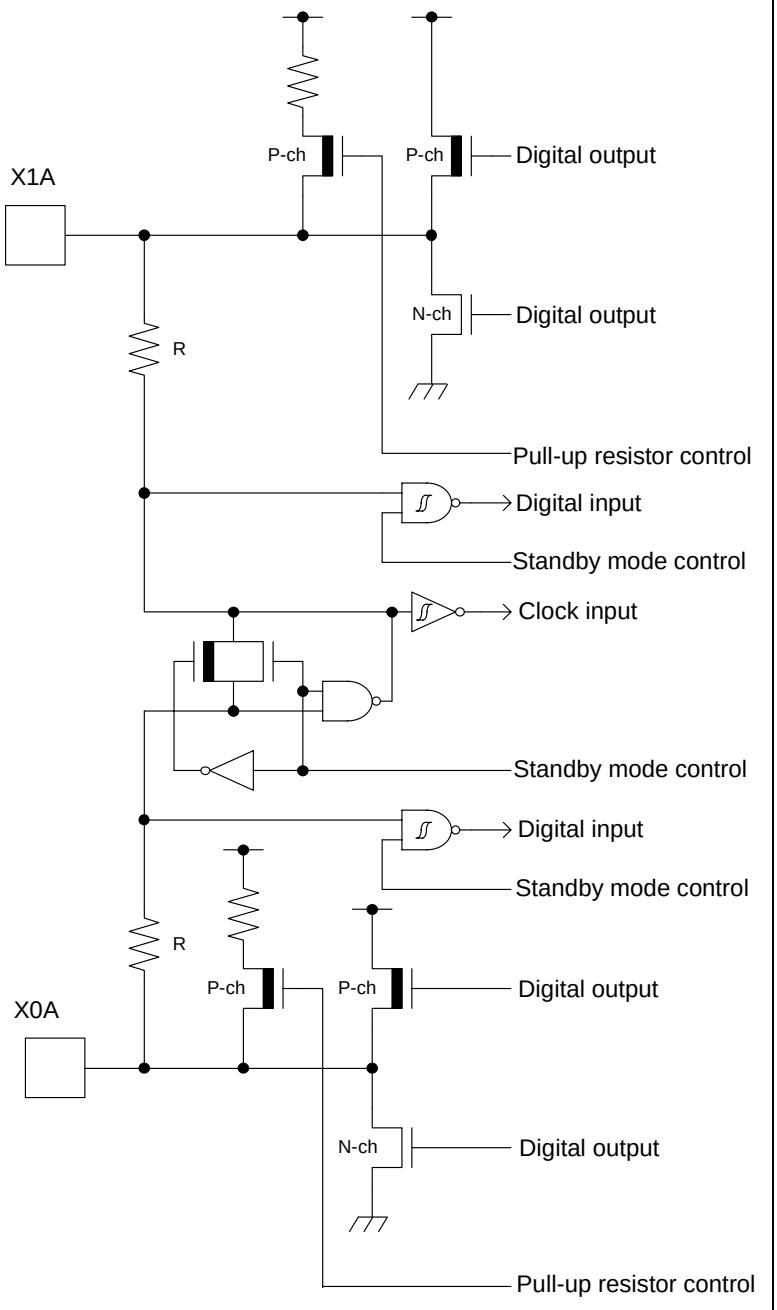
Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
38	33	P3C SIN2_1 RTO03_0 (PPG03_0) TIOA3_1 INT19_1 MAD21_0	G	K
39	34	P3D SOT2_1 (SDA2_1) RTO04_0 (PPG04_0) TIOA4_1 MAD20_0	G	I
40	35	P3E SCK2_1 (SCL2_1) RTO05_0 (PPG05_0) TIOA5_1 MAD19_0	G	I
41	-	P5D SIN1_1 MI2SDI1_1 TIOB12_2 INT03_2	E	K
42	-	P5E SOT1_1 (SDA1_1) MI2SDO1_1 TIOA13_2	E	I
43	-	P5F SCK1_1 (SCL1_1) MI2SCK1_1 TIOB13_2	E	I
44	36	VSS	-	-
45	37	VCC	-	-
46	38	P40 SIN7_1 RTO10_0 (PPG10_0) TIOA0_0 AIN0_0 INT23_0 MCSX7_0	G	K

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
66	56	P4E	L	Q
		SCK9_0 (SCL9_0)		
		INT05_0		
		WKUP2		
		MCSX1_0		
67	57	P70	L	I
		ADTG_7		
		SOT9_0 (SDA9_0)		
		MCSX0_0		
68	58	P71	I	K
		ADTG_8		
		SIN9_0		
		INT04_1		
		MRDY_0		
69	59	P72	E	I
		TIOB0_0		
		INT06_2		
		MAD00_0		
70	60	P73	E	K
		SIN8_0		
		TIOB1_0		
		INT20_0		
		MAD01_0		
71	61	P74	E	I
		SOT8_0 (SDA8_0)		
		TIOB2_0		
		MAD02_0		
72	62	P75	E	I
		SCK8_0 (SCL8_0)		
		TIOB3_0		
		MAD03_0		
73	63	P76	E	K
		SIN6_0		
		TIOB4_0		
		INT21_0		
		MAD04_0		
74	64	P77	L	I
		SOT6_0 (SDA6_0)		
		TIOB5_0		
		MAD05_0		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
75	65	P78	L	I
		SCK6_0 (SCL6_0)		
		AIN0_1		
		MAD06_0		
76	66	P79	E	K
		SCS60_0		
		BIN0_1		
		INT22_0		
		MAD07_0		
77	67	P7A	E	K
		SCS61_0		
		ZIN0_1		
		INT07_2		
		MAD08_0		
78	-	PF2	E	I
		SCS62_0		
		DTTI1X_1		
		TIOA6_1		
		IC1_CLK_1		
79	-	PF3	E	K
		SCS63_0		
		FRCK1_1		
		TIOB6_1		
		INT05_1		
		IC1_VCC_1		
80	-	PF4	E	K
		IC10_1		
		TIOA7_1		
		INT06_1		
		IC1_VPEN_1		
81	-	PF5	E	K
		SIN3_1		
		IC11_1		
		TIOB7_1		
		INT07_1		
		IC1_RST_1		
82	-	PF6	E	K
		SOT3_1 (SDA3_1)		
		IC12_1		
		TIOA14_1		
		INT20_1		
		IC1_DATA_1		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
112	-	PB6	F	N
		AN22		
		SOT8_1 (SDA8_1)		
		TIOA12_1		
		BIN1_2		
		TRACED14		
113	-	PB7	F	N
		AN23		
		SCK8_1 (SCL8_1)		
		TIOB12_1		
		ZIN1_2		
		TRACED15		
114	90	P1C	F	N
		AN12		
		SCK0_1 (SCL0_1)		
		TIOA5_2		
		TRACECLK		
115	91	P1D	F	L
		AN13		
		SOT0_1 (SDA0_1)		
		TIOB5_2		
		MAD09_0		
116	92	P1E	F	M
		AN14		
		SIN0_1		
		TIOA8_1		
		INT26_1		
		MAD10_0		
117	93	P1F	F	M
		AN15		
		RTS5_0		
		TIOB8_1		
		INT27_1		
		MAD11_0		
118	94	P2A	F	M
		AN24		
		CTS5_0		
		INT08_2		
		MAD12_0		

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
External bus	MADATA00_0	External bus interface data bus (address/data multiplex bus)	2	2
	MADATA01_0		3	3
	MADATA02_0		4	4
	MADATA03_0		5	5
	MADATA04_0		6	6
	MADATA05_0		7	7
	MADATA06_0		8	8
	MADATA07_0		9	9
	MADATA08_0		13	10
	MADATA09_0		14	11
	MADATA10_0		15	12
	MADATA11_0		16	13
	MADATA12_0		17	14
	MADATA13_0		18	15
	MADATA14_0		19	16
	MADATA15_0		20	17
	MDQM0_0	External bus interface byte mask signal output pin	21	18
	MDQM1_0		22	19
	MALE_0	External bus interface address latch enable output signal for multiplex	171	139
	MRDY_0	External bus interface external RDY input signal	68	58
	MCLKOUT_0	External bus interface external clock output pin	23	20
	MNALE_0	External bus interface ALE signal to control NAND flash output pin	97	81
	MNCLE_0	External bus interface CLE signal to control NAND flash output pin	96	80
	MNREX_0	External bus interface read enable signal to control NAND flash	94	78
	MNWEX_0	External bus interface write enable signal to control NAND flash	95	79
	MOEX_0	External bus interface read enable signal for SRAM	169	137
	MWEX_0	External bus interface write enable signal for SRAM	170	138
	MSDCLK_0	SDRAM interface SDRAM clock output pin	65	55
	MSDCKE_0	SDRAM interface SDRAM clock enable pin	64	54
	MRASX_0	SDRAM interface SDRAM row active strobe pin	60	50
	MCASX_0	SDRAM interface SDRAM column active strobe pin	61	51
	MSDWEX_0	SDRAM interface SDRAM write enable pin	62	52

Type	Circuit	Remarks
D		It is possible to select the sub oscillation/GPIO function. When the main oscillation is selected: ・ Oscillation feedback resistor: approximately 5 MΩ ・ Standby mode control When the GPIO is selected: ・ CMOS level output. ・ CMOS level hysteresis input ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA

8. Handling Precautions

Every semiconductor device has a characteristic, inherent rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

8.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins that connect semiconductor devices to power supply and I/O functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.
2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions, if present for extended periods of time, can damage the device; therefore, avoid this type of connection.
3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power-supply pin or ground pin.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent this, do the following:

1. Avoid exposure to rapid temperature changes, which can cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
3. When Dry Packages are opened, it is recommended to have humidity between 40% and 70%.
4. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in these aluminum laminate bags for storage.
5. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

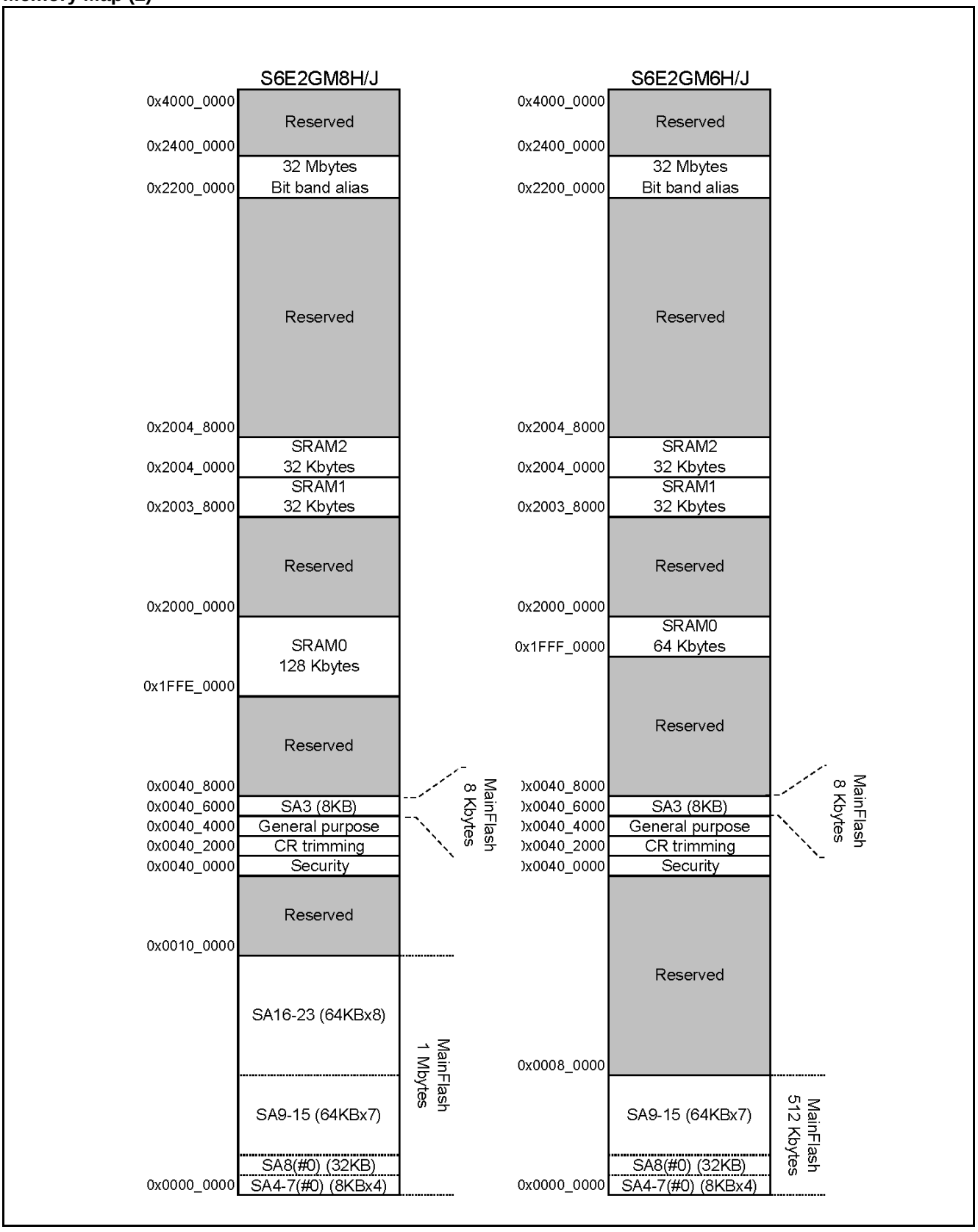
Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons, and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ). Wearing of conductive clothing and shoes, and the use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of Styrofoam or other highly static-prone materials for storage of completed board assemblies.

Memory Map (2)



*: See S6E2GM/GK/GH/G3/G2 Series Flash Programming Manual to confirm the detail of flash Memory.

11. Pin Status in Each CPU State

The terms used for pin status have the following meanings:

- INITX = 0

  This is the period when the INITX pin is at the L level.

- INITX = 1

  This is the period when the INITX pin is at the H level.

- SPL = 0

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 0.

- SPL = 1

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 1.

- Input enabled

  Indicates that the input function can be used.

- Internal input fixed at 0

  This is the status that the input function cannot be used. Internal input is fixed at L.

- Hi-Z

  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

  Indicates that the setting is disabled.

- Maintain previous state

  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.

- Analog input is enabled

  Indicates that the analog input is enabled.

- Trace output

  Indicates that the trace function can be used.

- GPIO selected

  In Deep standby mode, pins switch to the general-purpose I/O port.

- Setting prohibition

  Prohibition of a setting by specification limitation

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
J	Analog output selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	*2	*3	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External interrupt enable selected					Maintain previous state	Maintain previous state			
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									
K	External interrupt enable selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0			
	GPIO selected									
L	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	GPIO selected									

2: V_{CC} must not drop below V_{SS} - 0.5 V.

3: $USBV_{CC}0$, $USBV_{CC}1$ must not drop below V_{SS} - 0.5 V.

4: $ETHV_{CC}$ must not drop below V_{SS} - 0.5 V.

5: Ensure that the voltage does not exceed V_{CC} + 0.5V, for example, when the power is turned on.

6: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

7: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100-ms period.

8: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100-ms period.

WARNING:

- *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.*

Current Explanation Diagram

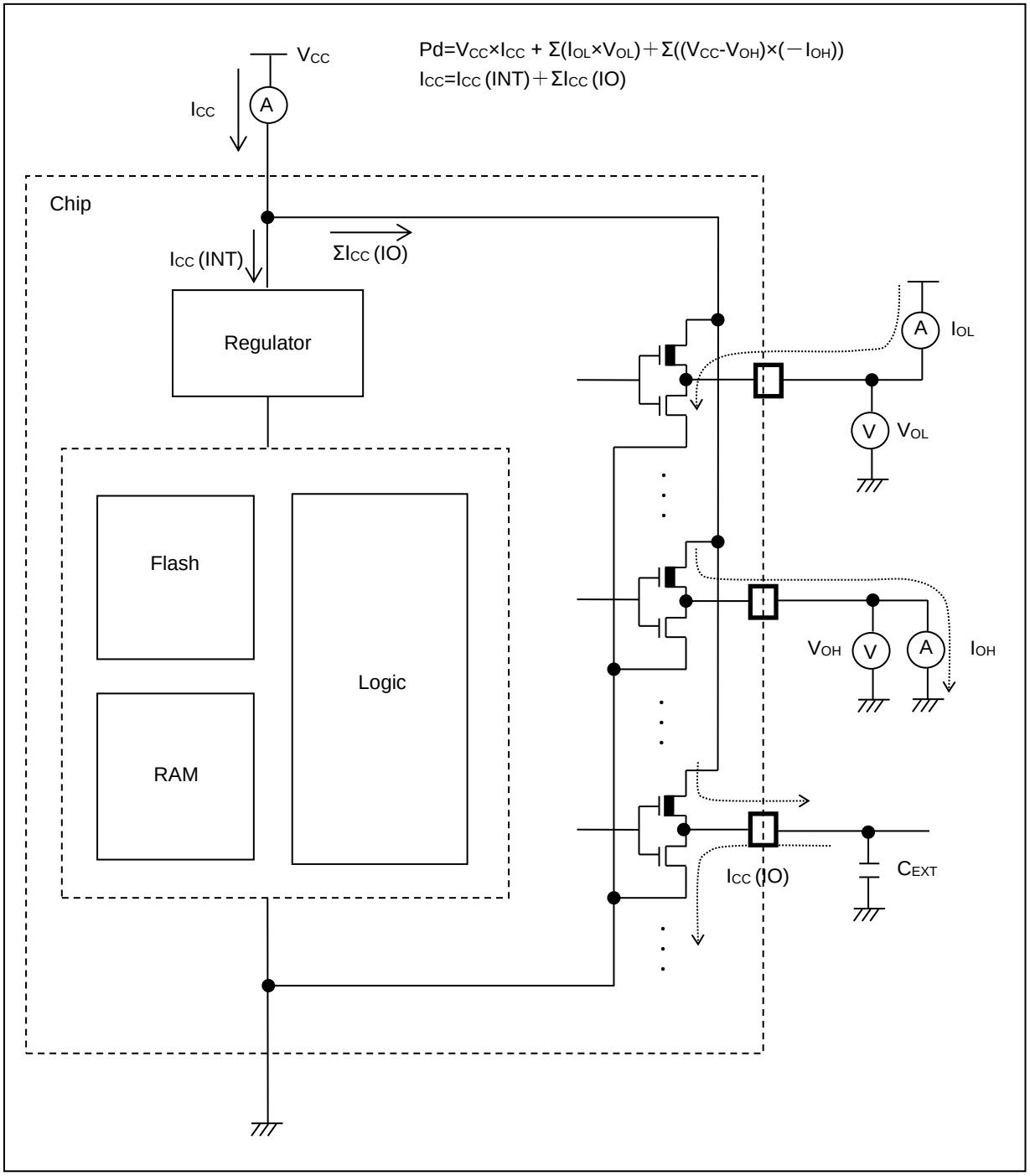


Table 12-2 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Disabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *7,*8 (PLL)	*5	180 MHz	82	140	mA	*3 When all peripheral clocks are on
				*6	160 MHz	74	132	mA	
					144 MHz	68	126	mA	
					120 MHz	58	116	mA	
					100 MHz	49	107	mA	
					80 MHz	40	98	mA	
					60 MHz	31	89	mA	
					40 MHz	22	80	mA	
					20 MHz	13	71	mA	
					8 MHz	7.5	65	mA	
					4 MHz	5.6	63	mA	
				*5	180 MHz	48	106	mA	*3 When all peripheral clocks are off
				*6	160 MHz	44	102	mA	
					144 MHz	41	99	mA	
					120 MHz	35	93	mA	
					100 MHz	30	88	mA	
					80 MHz	25	83	mA	
					60 MHz	20	78	mA	
					40 MHz	14	72	mA	
					20 MHz	8.7	66	mA	
					8 MHz	5.6	63	mA	
					4 MHz	4.5	62	mA	

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are input and are fixed at 0

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

5: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 0)

6: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 0)

7: With data access to a MainFlash memory.

8: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-9 Typical and Maximum Current Consumption in Deep Standby Stop Mode, Deep Standby RTC Mode

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCHD}	VCC	Deep standby Stop mode (When RAM is off)	-	89	162	µA	*3, *4 T_A = +25°C
					-	1689	µA	*3, *4 T_A = +85°C
					-	2189	µA	*3, *4 T_A = +105°C
			Deep standby Stop mode (When RAM is on)	-	101	245	µA	*3, *4 T_A = +25°C
					-	2401	µA	*3, *4 T_A = +85°C
					-	3223	µA	*3, *4 T_A = +105°C
	I_{CCRD}		Deep standby RTC mode*6 (When RAM is off)	32 kHz	93	166	µA	*3, *4 T_A = +25°C
					-	1693	µA	*3, *4 T_A = +85°C
					-	2193	µA	*3, *4 T_A = +105°C
			Deep standby RTC mode*6 (When RAM is on)		105	249	µA	*3, *4 T_A = +25°C
					-	2405	µA	*3, *4 T_A = +85°C
					-	3227	µA	*3, *4 T_A = +105°C

1: V_{CC} = 3.3 V

2: V_{CC} = 5.5 V

3: When all ports are input and are fixed at 0

4: When LVD is off

5: When sub oscillation is off

6: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

12.8 MainFlash Memory Write/Erase Characteristics

(V_{CC} = 2.7V to 5.5V)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large Sector	-	0.7	3.7	s	Includes write time prior to internal erase
	Small Sector	-	0.3	1.1	s	
Half word (16-bit) write time	Write cycles ≤ 100 times	-	12	100	µs	Not including system-level overhead time
	Write cycles > 100 times			200		
Chip erase time*		-	13.6	68	s	Includes write time prior to internal erase

*: It indicates the chip erase time of 1MB MainFlash memory

For devices with 1.5 MB or 2 MB of MainFlash memory, two erase cycles are required.

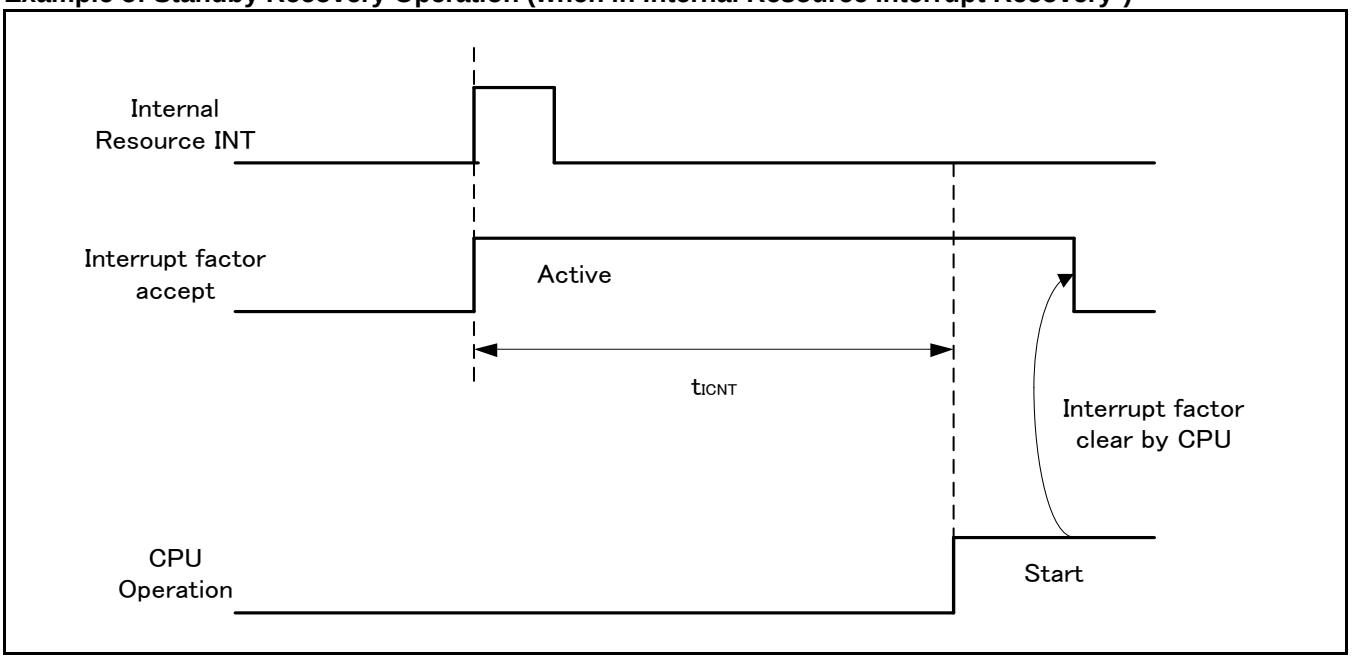
See 3.2.2 Command Operating Explanations and 3.3.3 Flash Erase Operation in this product's Flash Programming Manual for the detail.

Write Cycles and Data Retention Time

Erase/Write Cycles (Cycle)	Data Retention Time (Year)
1,000	20*
10,000	10*
100,000	5*

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C).

Example of Standby Recovery Operation (when in Internal Resource Interrupt Recovery*)

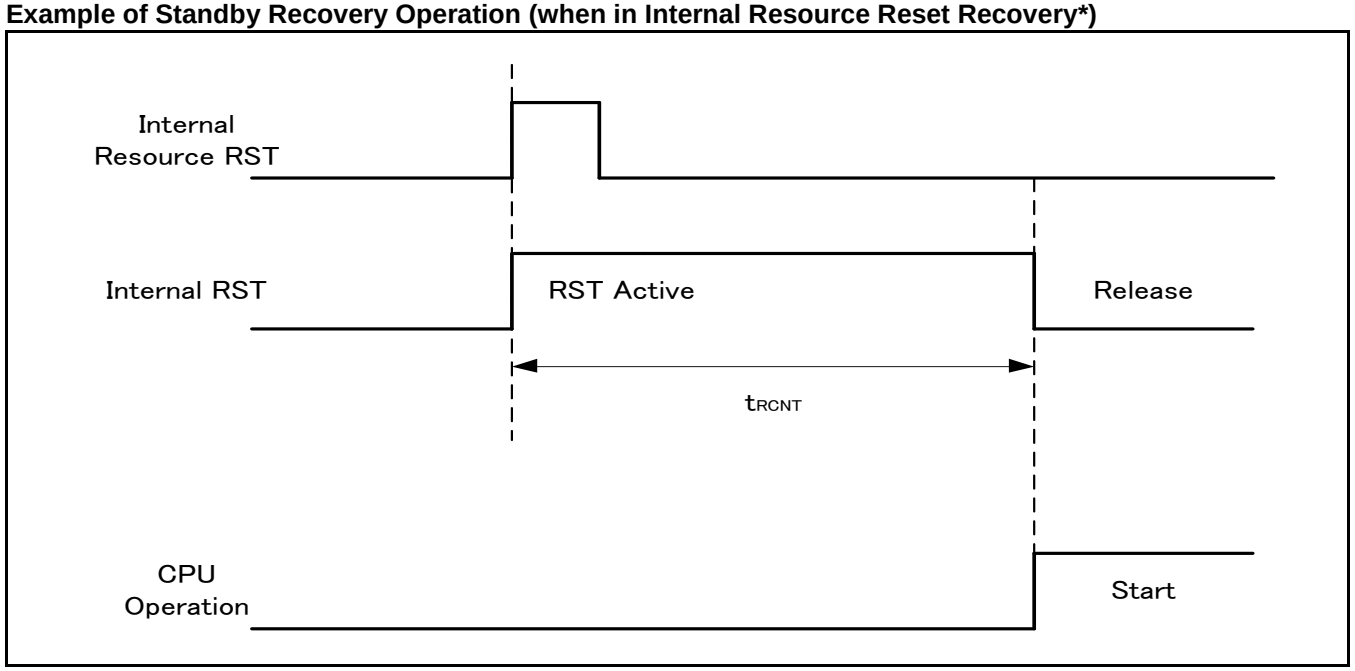


*: Depending on the standby mode, interrupt from the internal resource is not included in the recovery cause.

Notes:

- *The return factor is different in each low-power consumption mode. See Chapter 6: Low Power Consumption mode and Operations of Standby modes in FM4 Family Peripheral Manual Main Part (002-04856).*
- *The recovery process is unique for each operating mode. See Chapter 6: Low Power Consumption mode in FM4 Family Peripheral Manual Main Part (002-04856).*

Example of Standby Recovery Operation (when in Internal Resource Reset Recovery*)



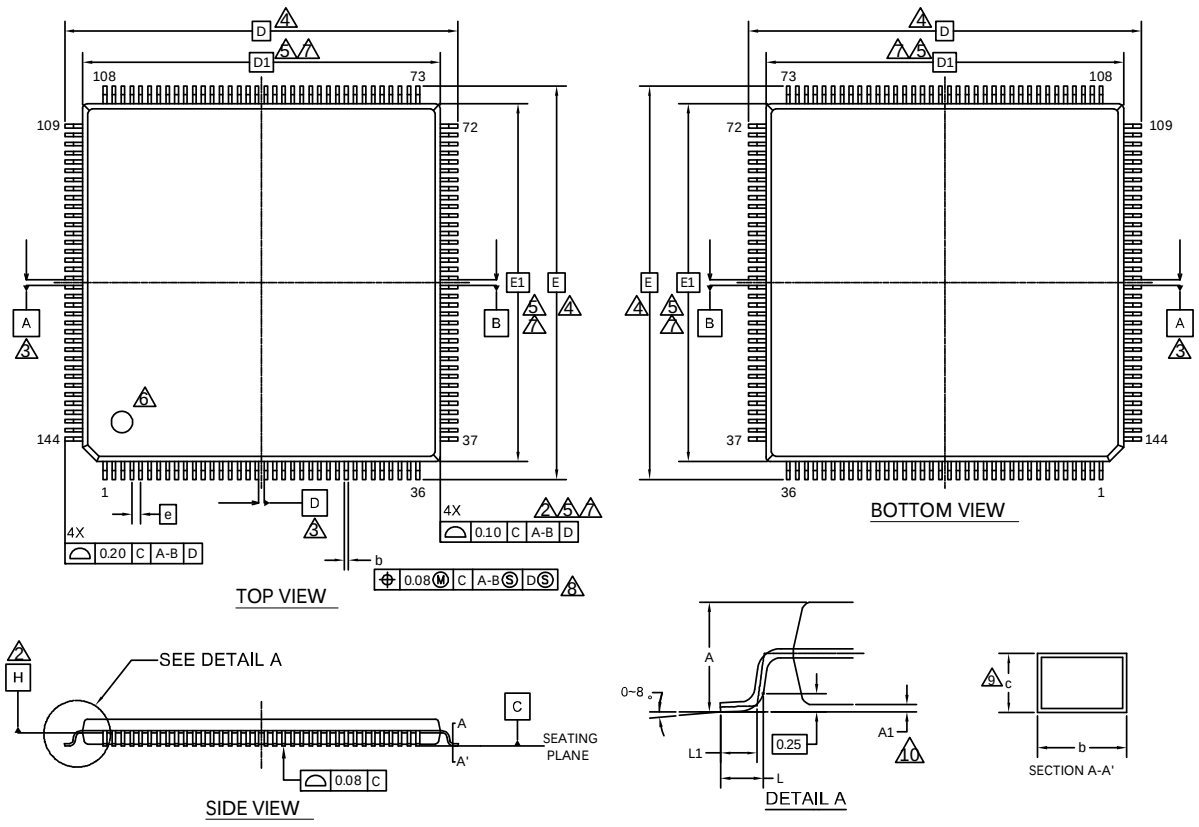
*: Depending on the low-power consumption mode, the reset issue from the internal resource is not included in the recovery cause.

Notes:

- *The return factor is different in each low power consumption mode.*
  See Chapter 6: Low Power Consumption mode and Operations of Standby modes in "FM4 Family Peripheral Manual Main Part (002-04856).
- *The recovery process is unique for each operating mode. See Chapter 6: Low Power Consumption mode in FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the power-on reset/low-voltage detection reset, they are not included in the return factor. See 12.4.8 Power-On Reset Timing.*
- *In recovering from reset, CPU changes to High-speed Run mode. In the case of using the main clock and PLL clock, they need further main clock oscillation stabilization wait time and oscillation stabilization wait time of Main PLL clock.*
- *Internal resource reset indicates Watchdog reset and CSV reset.*

14. Package Dimensions

Package Type	Package Code
LQFP 144	LQS144



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D		22.00 BSC	
D1		20.00 BSC	
e		0.50 BSC	
E		22.00 BSC	
E1		20.00 BSC	
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 144 LEAD LQFP
20.0X20.0X1.7 MM LQS144 REV*A

002-13015 *A