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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, CSIO, EBI/EMI, Ethernet, I²C, LINbus, SmartCard, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	121
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2g28hhagv2000a

3. Package-Dependent Features

All S6E2G Series of parts are available in both 144-pin LQFP and 176-pin LQFP.

Description	Base Part Number S6E2G			
	Package Suffix			
	H0A	HHA*	J0A	JHA*
LQFP: (0.5 mm pitch)	144 pins		176 pins	
I/O Ports	121 pins (Max)		153 pins (Max)	
12-bit ADC converter	24 (3 units)		32 ch (3 units)	
Crypto Assist Function	—	Yes	—	Yes

*HHA and JHA parts have the Crypto Assist Function built in. HHA and JHA options are not available for the S6E2GH or S6E2G3 parts. The HHA and JHA options are available on the S6E2GM, S6E2GK, and S6E2G2 parts.

Notes:

- *For an explicit list of part numbers and the feature differences among them, see 13. Ordering Information*
- *See 14. Package Dimensions for detailed information on each package.*

- Resets
  - Reset requests from INITX pin
  - Power on reset
  - Software reset
  - Watchdog timer reset
  - Low-voltage detector reset
  - Clock supervisor reset

Clock Supervisor (CSV)

Clocks generated by internal CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)

This Series include two-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage that has been set, the low-voltage detector function generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-power Consumption Mode

Six low power consumption modes are supported.

- Sleep
- Timer
- RTC
- Stop
- Deep standby RTC (selectable from with/without RAM retention)
- Deep standby stop (selectable from with/without RAM retention)

Peripheral Clock Gating

The system can reduce the current consumption of the total system with gating the operation clocks of peripheral functions not used.

Crypto Assist Function

These features are enabled for the crypto assist function.

The dedicated middleware is necessary for this calculator operation.

- PKA (Public Key Accelerator)
  - PKA（Public Key Accelerator）is modular exponentiation calculation accelerator used of RSA Public Key crypto and so on.
  - Available bit length: Up to 2048-bit
- AES calculator
  - AES (Advanced Encryption Standard) calculator is a AES common key crypto accelerator which is compliant with FIPS (Federal Information Processing Standard Publication)197.
  - Available key length: 128/192/256-bit
  - CBC mode and ECB mode support
- External Bus Data Scramble
  - It enables to scramble input/output data of External Bus Interface.

Debug

- Serial wire JTAG debug port (SWJ-DP)
- Embedded trace macrocells (ETM) provide comprehensive debug and trace facilities.
- AHB trace macrocells (HTM)

Unique ID

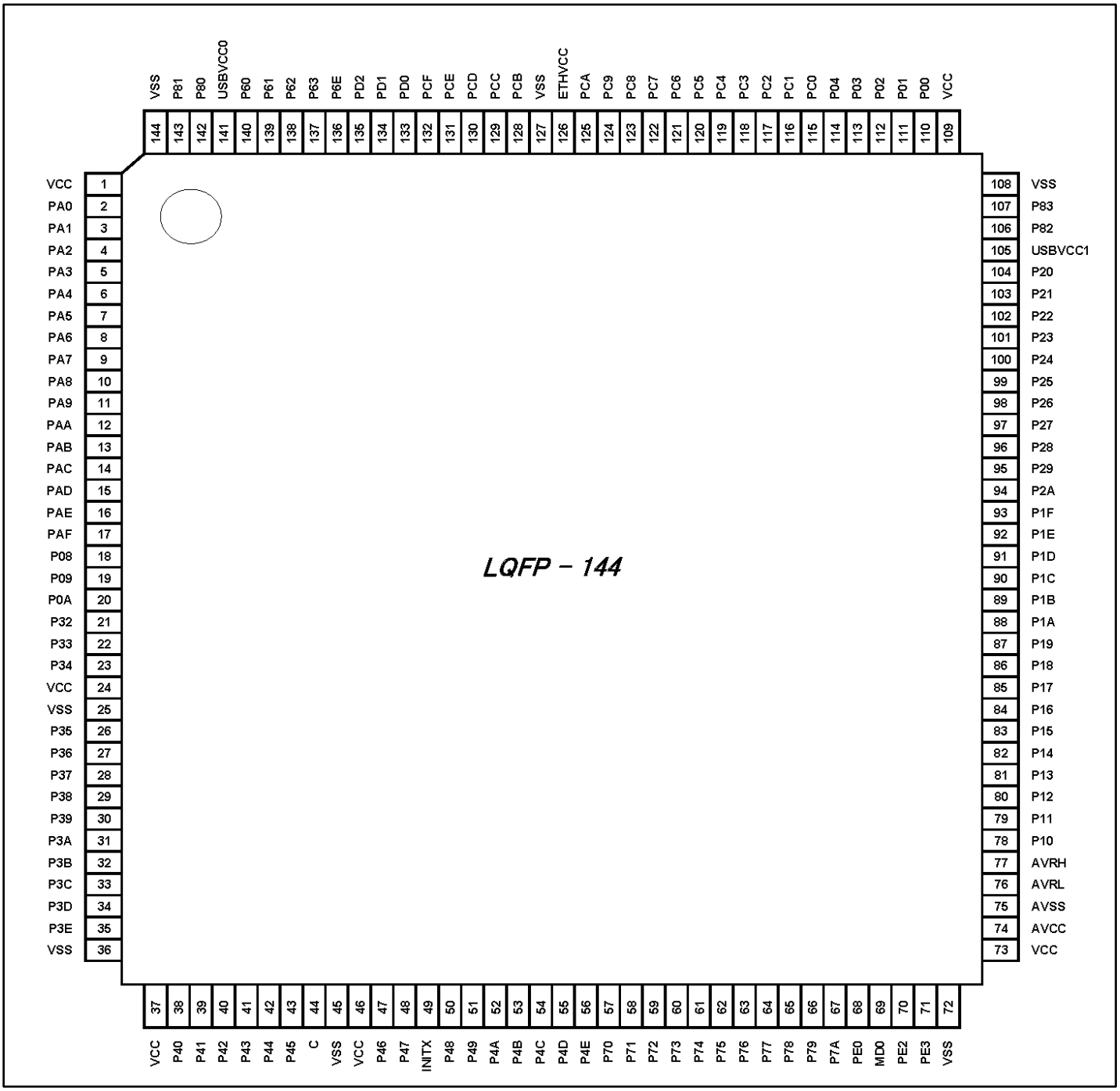
Unique value of the device (41-bit) is set.

Power Supply

- Four power supplies
  - Wide range voltage: VCC = 2.7 V to 5.5 V
  - Power supply for USB ch 0 I/O: USBVCC0
= 3.0 V to 3.6 V (when USB is used)
= 2.7 V to 5.5 V (when GPIO is used)
  - Power supply for USB ch 1 I/O: USBVCC1
= 3.0 V to 3.6 V (when USB is used)
= 2.7 V to 5.5 V (when GPIO is used)
  - Power supply for Ethernet-MAC I/O: ETHVCC
= 3.0 V to 5.5 V (when Ethernet is used.)

5. Pin Assignments

LQS144



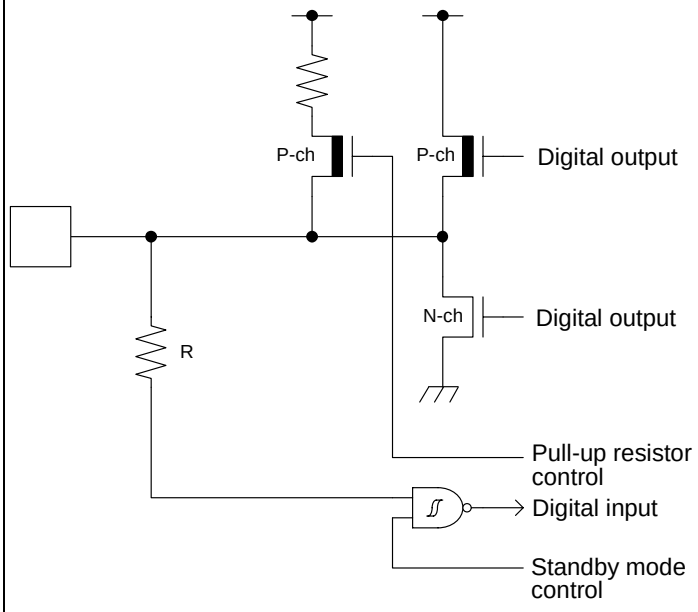
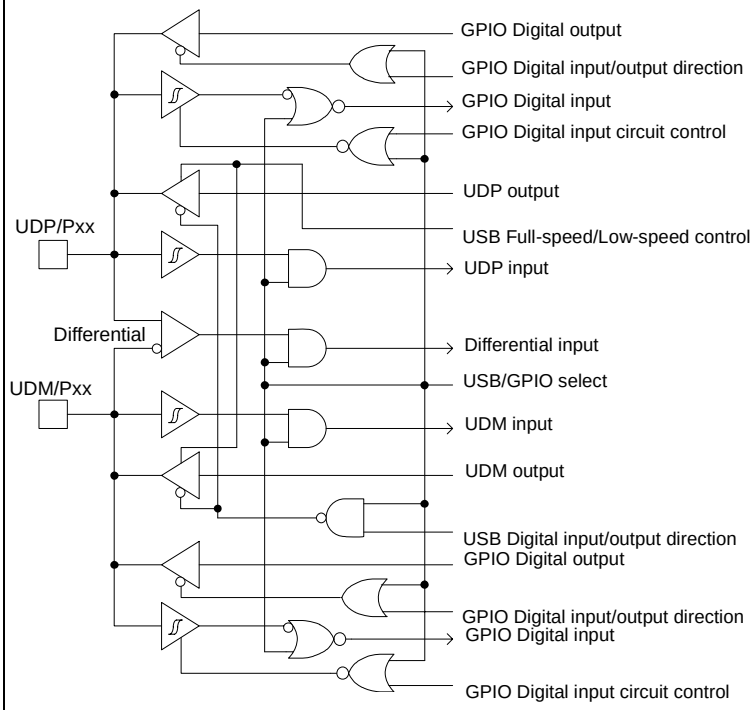
Note:

- *Only the GPIO function is shown on GPIO pins. See the table in Pin Descriptions for the full, multiplexed signal name.*

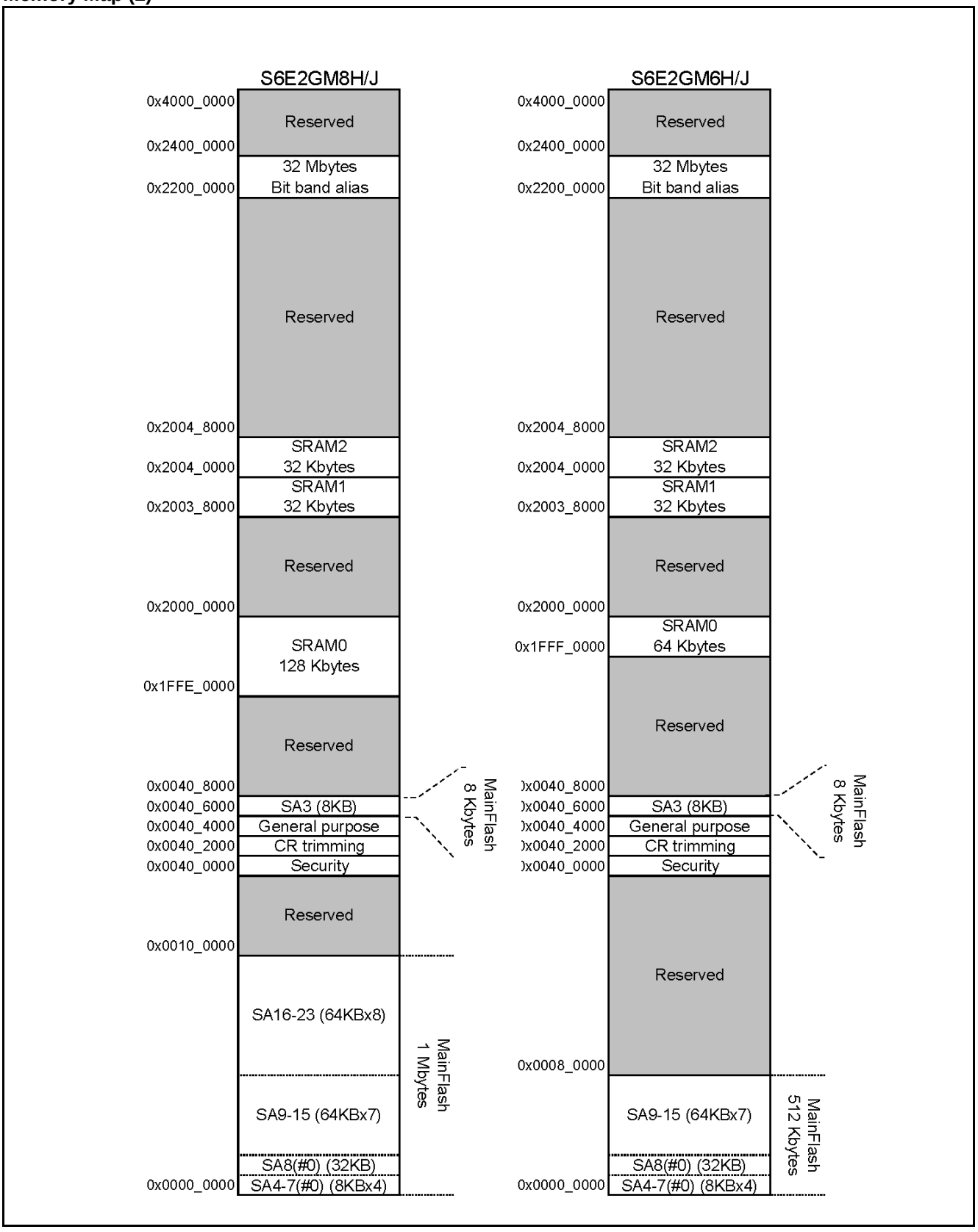
Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
105	-	PB3 AN19 SCS62_1 TIOB10_1 ZIN0_2 TRACED11	F	N
106	86	P18 AN08 SIN2_0 TIOA3_2 INT10_0 TRACED4	F	O
107	87	P19 AN09 SOT2_0 (SDA2_0) TIOB3_2 INT24_1 TRACED5	F	O
108	88	P1A AN10 SCK2_0 (SCL2_0) TIOA4_2 TRACED6	F	N
109	89	P1B AN11 TIOB4_2 INT11_0 TRACED7	F	O
110	-	PB4 AN20 SCS63_1 TIOA11_1 INT10_1 TRACED12	F	O
111	-	PB5 AN21 SIN8_1 TIOB11_1 AIN1_2 INT11_1 TRACED13	F	O

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Base Timer 7	TIOA7_0	Base Timer ch 7 TIOA pin	149	119
	TIOA7_1		80	-
	TIOA7_2		171	139
	TIOB7_0	Base Timer ch 7 TIOB pin	148	118
	TIOB7_1		81	-
	TIOB7_2		170	138
Base Timer 8	TIOA8_0	Base Timer ch 8 TIOA pin	2	2
	TIOA8_1		116	92
	TIOA8_2		10	-
	TIOB8_0	Base Timer ch 8 TIOB pin	17	14
	TIOB8_1		117	93
	TIOB8_2		11	-
Base Timer 9	TIOA9_0	Base Timer ch 9 TIOA pin	3	3
	TIOA9_1		102	-
	TIOA9_2		12	-
	TIOB9_0	Base Timer ch 9 TIOB pin	18	15
	TIOB9_1		103	-
Base Timer 10	TIOA10_0	Base Timer ch 10 TIOA pin	4	4
	TIOA10_1		104	-
	TIOB10_0	Base Timer ch 10 TIOB pin	19	16
	TIOB10_1		105	-
Base Timer 11	TIOA11_0	Base Timer ch 11 TIOA pin	5	5
	TIOA11_1		110	-
	TIOB11_0	Base Timer ch 11 TIOB pin	20	17
	TIOB11_1		111	-
	TIOB11_2		24	-
Base Timer 12	TIOA12_0	Base Timer ch 12 TIOA pin	6	6
	TIOA12_1		112	-
	TIOA12_2		25	-
	TIOB12_0	Base Timer ch 12 TIOB pin	21	18
	TIOB12_1		113	-
	TIOB12_2		41	-
Base Timer 13	TIOA13_0	Base Timer ch 13 TIOA pin	7	7
	TIOA13_1		124	100
	TIOA13_2		42	-
	TIOB13_0	Base Timer ch 13 TIOB pin	22	19
	TIOB13_1		125	101
	TIOB13_2		43	-
Base Timer 14	TIOA14_0	Base Timer ch 14 TIOA pin	151	121
	TIOA14_1		82	-
	TIOB14_0	Base Timer ch 14 TIOB pin	150	120
	TIOB14_1		83	-

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
SD I/F	S_CLK_0	SD memory card interface SD memory card clock output pin	28	23
	S_CMD_0	SD memory card interface SD memory card command output	31	26
	S_DATA1_0	SD memory card interface SD memory card data bus	26	21
	S_DATA0_0		27	22
	S_DATA3_0		32	27
	S_DATA2_0		33	28
	S_CD_0	SD memory card interface SD memory card detection pin	35	30
	S_WP_0	SD memory card interface SD memory card write protection	34	29
Ethernet	E_COL	Collision detection	154	124
	E_COUT	Clock output for Ethernet PHY	158	128
	E_CRS	Carrier detection	155	125
	E_MDC	Management clock	152	122
	E_MDIO	Management data I/O	151	121
	E_PPS	PTP counter monitor	166	136
	E_RX00	Received data0	149	119
	E_RX01	Received data1	148	118
	E_RX02	Received data2	147	117
	E_RX03	Received data3	146	116
	E_RXCK_REFCK	Received clock input/ Reference clock	153	123
	E_RXDV	Received data enable	150	120
	E_RXER	Received data error detection	145	115
	E_TCK	Transition clock input	159	129
	E_TX00	Transition data0	164	134
	E_TX01	Transition data1	163	133
	E_TX02	Transition data2	162	132
	E_TX03	Transition data3	161	131
	E_TXEN	Transition data enable	165	135
	E_TXER	Transition data error detection	160	130

Type	Circuit	Remarks
G		・ CMOS level output ・ CMOS level hysteresis input ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -12 mA, I_{OL} = 12 mA ・ When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
H		It is possible to select either USB I/O or GPIO function. When the USB I/O is selected: ・ Full-speed, low-speed control When the GPIO is selected: ・ CMOS level output ・ CMOS level hysteresis input ・ Standby mode control ・ I_{OH} = -20.5 mA, I_{OL} = 18.5 mA

Memory Map (2)



*: See S6E2GM/GK/GH/G3/G2 Series Flash Programming Manual to confirm the detail of flash Memory.

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
M	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	External interrupt enable selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									
N	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									

Table 12-4 Typical and Maximum Current Consumption in Normal Operation (Other than PLL), Code with Data Accessing Running from Flash Memory (Flash 0 Wait-Cycle Mode and Read Access 0 Wait)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *6, *7 (main oscillation)	*5	4 MHz	4.3	62	mA	*3 When all peripheral clocks are on
						3.7	61	mA	*3 When all peripheral clocks are off
			Normal operation *6 (built-in High-speed CR)	*5	4 MHz	3.5	61	mA	*3 When all peripheral clocks are on
						2.9	60	mA	*3 When all peripheral clocks are off
			Normal operation *6, *8 (sub oscillation)	*5	32 kHz	0.47	58	mA	*3 When all peripheral clocks are on
						0.46	58	mA	*3 When all peripheral clocks are off
			Normal operation *6 (built-in low-speed CR)	*5	100 kHz	0.51	58	mA	*3 When all peripheral clocks are on
						0.50	58	mA	*3 When all peripheral clocks are off

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are input and are fixed at 0

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

5: When operating flash 0 wait-cycle mode and read access 0 wait (FRWTR.RWT = 00, FBFCR.SD = 000)

6: With data access to a MainFlash memory.

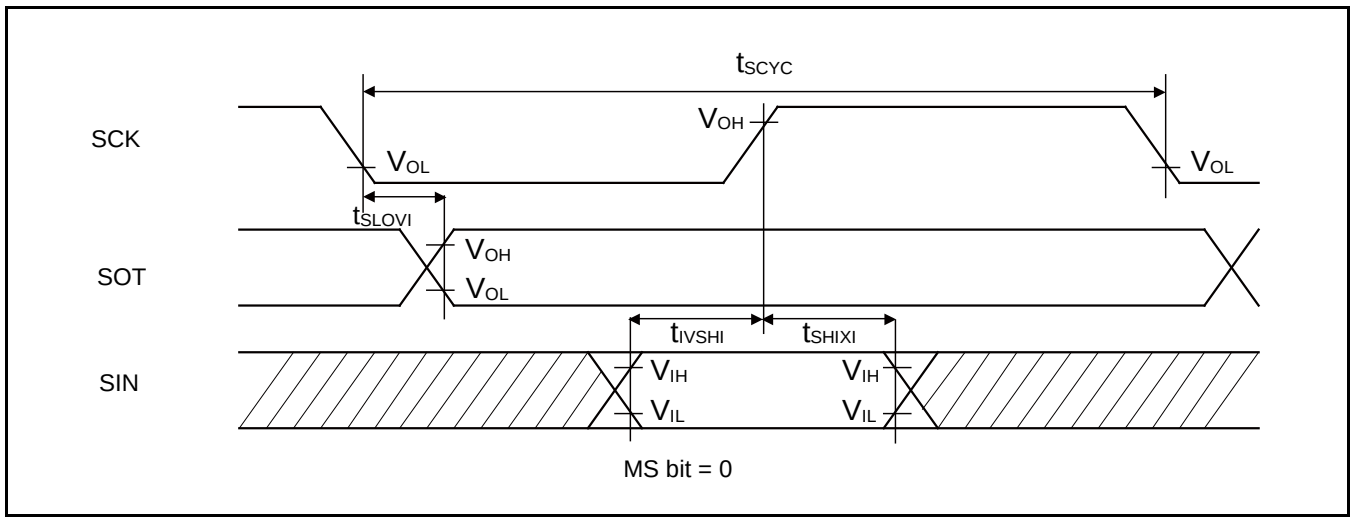
7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

8: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

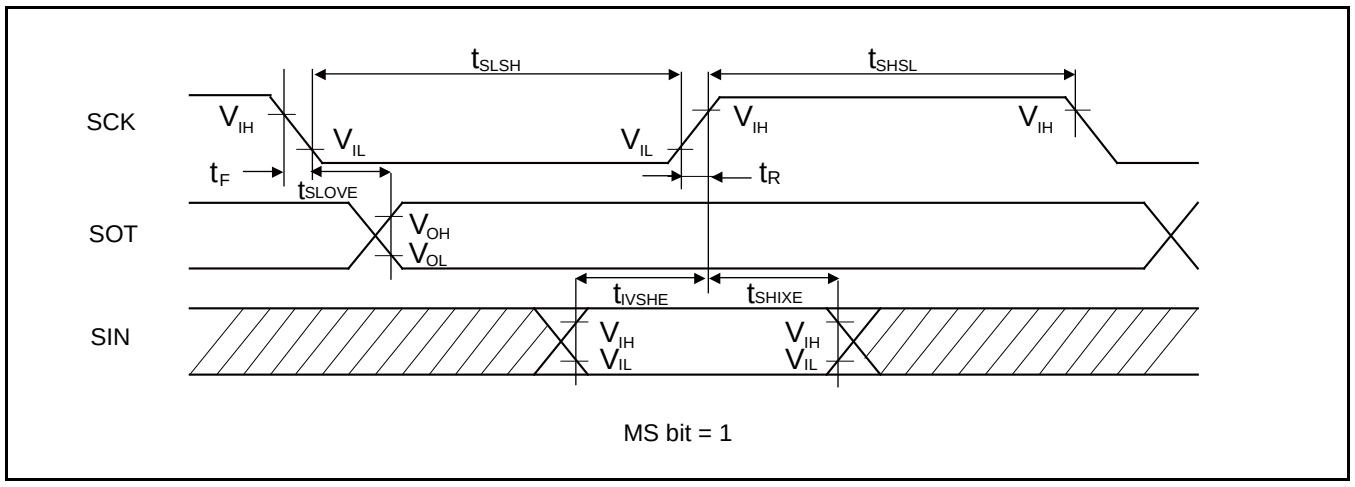
12.3.2 Pin Characteristics

(V_{CC} = $USBV_{CC}0$ = $USBV_{CC}1$ = $ETHV_{CC}$ = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V)

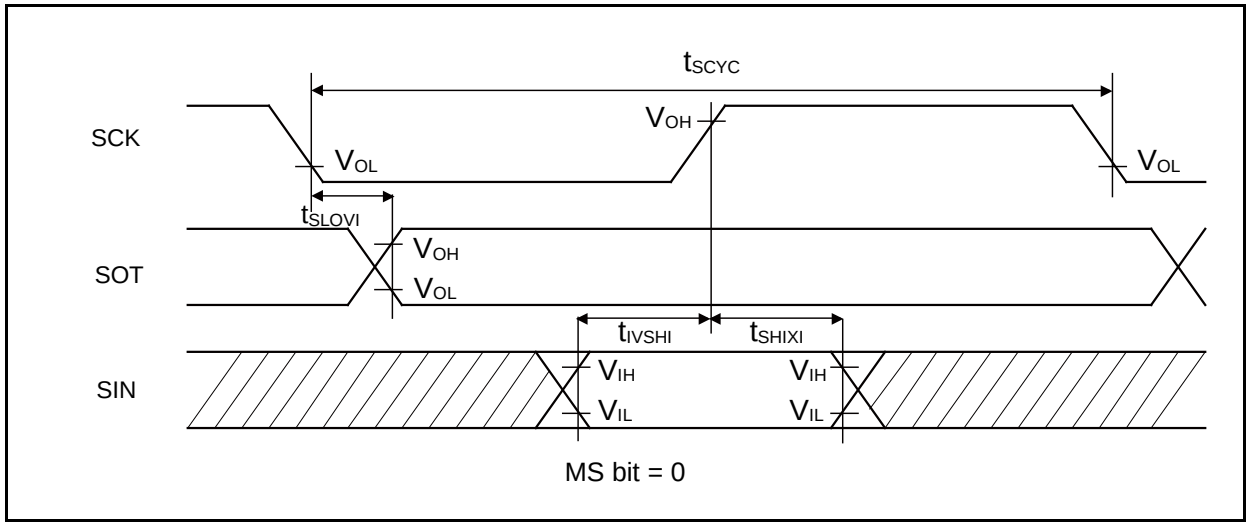
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	-	V_{CC}×0.8	-	V_{CC} + 0.3	V	
				$ETHV_{CC}$×0.8	-	$ETHV_{CC}$ + 0.3	V	
		MADATAxx	V_{CC} > 3.0 V, V_{CC} ≤ 3.6 V,	2.4	-	V_{CC} + 0.3	V	At External Bus
		5V tolerant input pin	-	V_{CC}×0.8	-	V_{SS} + 5.5	V	
		Input pin doubled as I^2C Fm+	-	V_{CC}×0.7	-	V_{SS} + 5.5	V	
		TTL Schmitt input pin	-	2.0	-	$ETHV_{CC}$+0.3	V	
L level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
				V_{SS} - 0.3	-	$ETHV_{CC}$×0.2	V	
		5V tolerant input pin	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		Input pin doubled as I^2C Fm+	-	V_{SS}	-	V_{CC}×0.3	V	
		TTL Schmitt input pin	-	V_{SS} - 0.3	-	0.8	V	
H level output voltage	V_{OH}	4 mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 2 mA					
			$ETHV_{CC}$ ≥ 4.5 V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	$ETHV_{CC}$	V	
			$ETHV_{CC}$ < 4.5 V, I_{OH} = - 2 mA					
		8 mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 8 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 4 mA					
			$ETHV_{CC}$ ≥ 4.5 V, I_{OH} = - 8 mA	$ETHV_{CC}$ - 0.5	-	$ETHV_{CC}$	V	
			$ETHV_{CC}$ < 4.5 V, I_{OH} = - 4 mA					
		12 mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 12 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 8 mA					
		The pin doubled as USB I/O	$USBV_{CC}$ ≥ 4.5 V, I_{OH} = - 20.5 mA	$USBV_{CC}$ - 0.4	-	$USBV_{CC}$	V	*1
			$USBV_{CC}$ < 4.5 V, I_{OH} = - 13.0 mA					
		The pin doubled as I^2C Fm+	V_{CC} ≥ 4.5 V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	At GPIO
			V_{CC} < 4.5V, I_{OH} = - 3 mA					



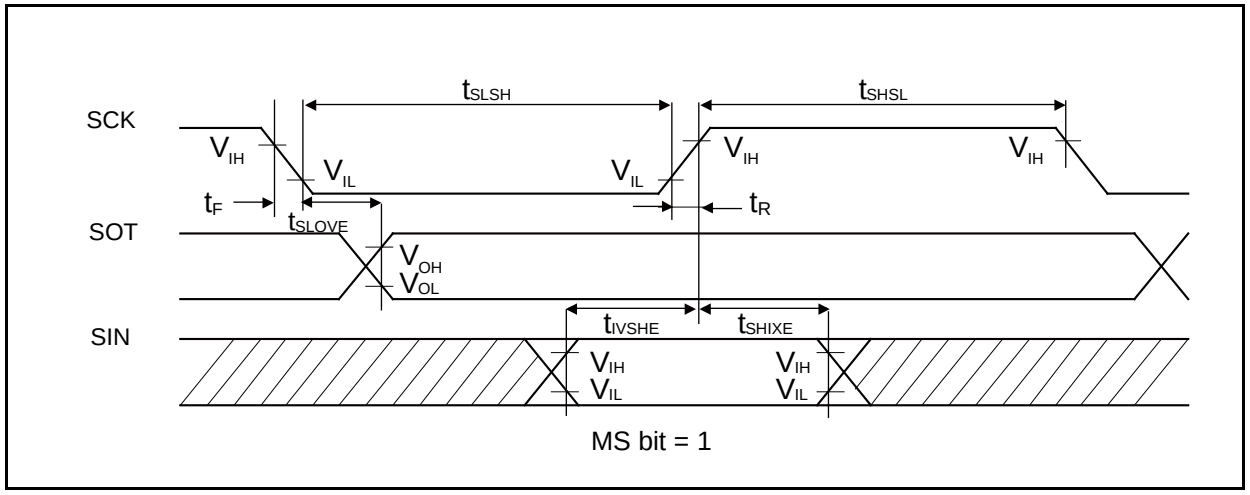
MS bit = 0



MS bit = 1



MS bit = 0



MS bit = 1

When Using High-Speed Synchronous Serial Chip Select (SCINV = 1, CSLVL = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC}≥ 4.5 V		Unit
			Min	Min	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↓→SCK↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↓→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 1. S6E2G Series Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

12.4.16 SD Card Interface Timing

Default-Speed Mode

■ Clock CLK (All values are referenced to V_{IH} and V_{IL} transition points)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Clock frequency Data Transfer mode	f_{PP}	S_CLK	C_{CARD} ≤ 10 pF (1card)	0	25	MHz
Clock frequency Identification mode	f_{OD}	S_CLK		0/100	400	kHz
Clock low time	t_{WL}	S_CLK		10	-	ns
Clock high time	t_{WH}	S_CLK		10	-	ns
Clock rise time	t_{TLH}	S_CLK		-	10	ns
Clock fall time	t_{THL}	S_CLK		-	10	ns

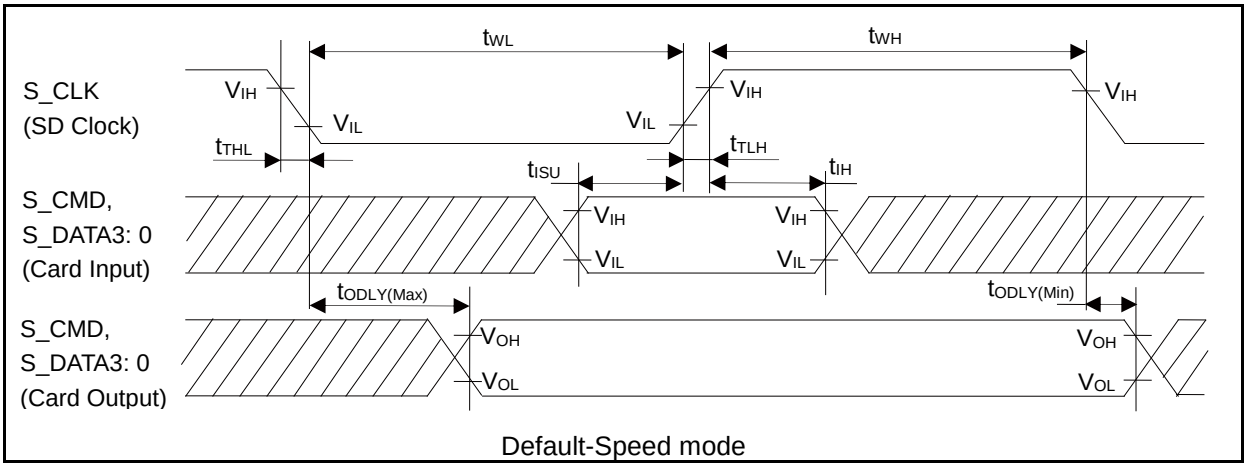
*: 0 Hz means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required.

■ Card Inputs CMD, DAT (referenced to Clock CLK)

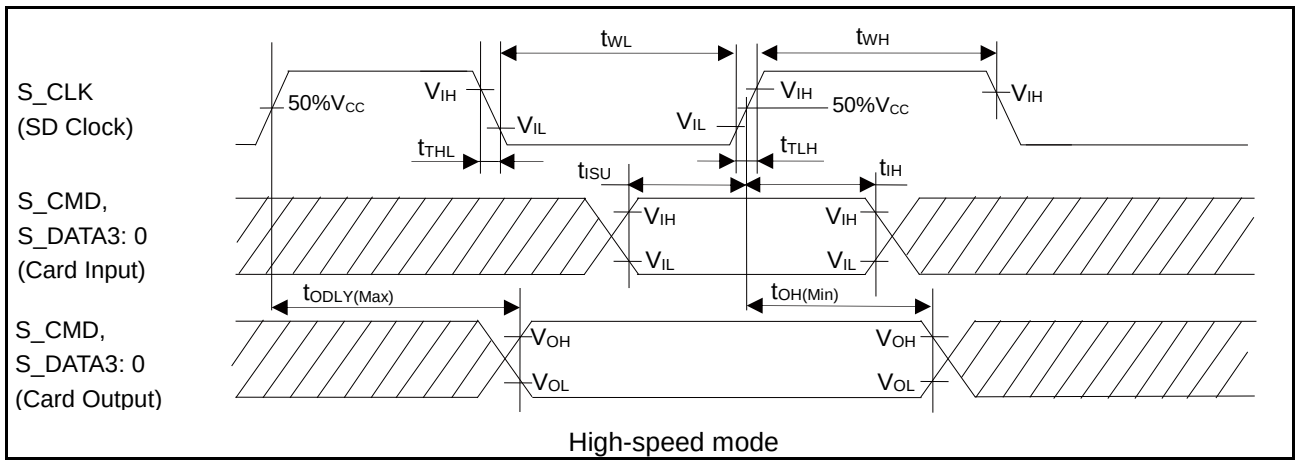
Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Input set-up time	t_{ISU}	S_CMD, S_DATA3: 0	C_{CARD} ≤ 10 pF (1card)	5	-	ns
Input hold time	t_{IH}	S_CMD, S_DATA3: 0		5	-	ns

■ Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Output Delay time during Data Transfer mode	t_{ODLY}	S_CMD, S_DATA3: 0	C_{CARD} ≤ 40 pF (1card)	0	14	ns
Output Delay time during Identification mode	t_{ODLY}	S_CMD, S_DATA3: 0		0	50	ns



Default-Speed mode



High-speed mode

Notes:

- *The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.*
- *For more information about clock frequency (f_{PP}), see Chapter 15: SD card Interface in FM4 Family Peripheral Manual Main Part (002-04856).*

12.4.17 ETM/ HTM Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK, TRACED[15: 0]	V_{CC} ≥ 4.5 V	2	9	ns	
			V_{CC} <4.5 V	2	15		
TRACECLK frequency	$1/t_{TRACE}$	TRACECLK	V_{CC} ≥ 4.5 V		50	MHz	
			V_{CC} <4.5 V		32	MHz	
TRACECLK clock cycle	t_{TRACE}		V_{CC} ≥ 4.5 V	20	-	ns	
			V_{CC} <4.5 V	31.25	-	ns	

Note:

- *When the external load capacitance C_L = 30 pF.*

12.4.19 Ethernet-MAC Timing

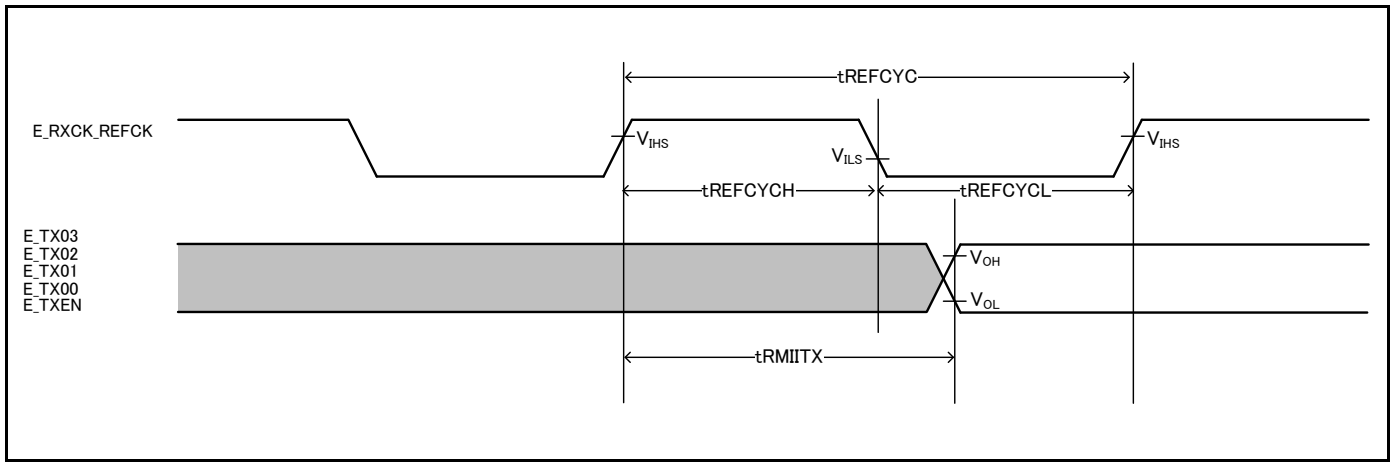
RMII Transmission (100 Mbps/10 Mbps)

($ETHV_{CC}$ = 3.0V to 3.6V, 4.5V to 5.5V*1, V_{SS} = 0V, C_L = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Reference clock cycle time*2	t_{REFCYC}	E_RXCK_REFCK	20 ns (typical)	-	-	ns
Reference clock High-pulse-width duty cycle	$t_{REFCYCH}$	E_RXCK_REFCK	$t_{REFCYCH}/t_{REFCYC}$	35	65	%
Reference clock Low-pulse-width duty cycle	$t_{REFCYCL}$	E_RXCK_REFCK	$t_{REFCYCL}/t_{REFCYC}$	35	65	%
REFCK ↑ → Transmitted data delay time	t_{RMIITX}	E_TX03, E_RX02, E_TX01, E_TX00, E_TXEN	-	-	12	ns

*1: When ETHV = 4.5 V to 5.5 V, it is recommended to add a series resistor at the output pin to suppress the output current.

*2: The reference clock is fixed to 50 MHz in the RMII specifications. The clock accuracy should meet the PHY-device specifications.



12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V)

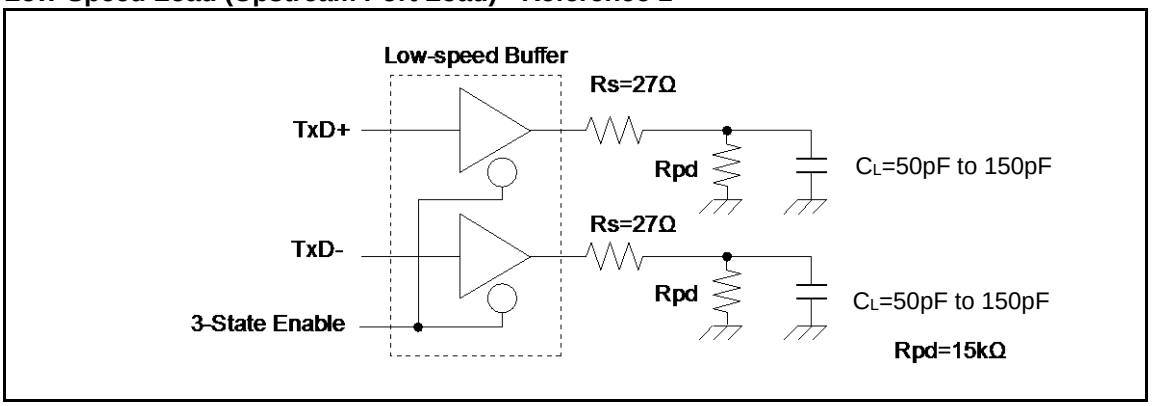
Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral nonlinearity	-	-	-	-	± 4.5	LSB	AVRH = 2.7 V to 5.5 V Offset calibration when used
Differential nonlinearity	-	-	-	-	± 2.5	LSB	
Zero transition voltage	V_{ZT}	Anxx	-	± 2	± 7	LSB	
Full-scale transition voltage	V_{FST}	Anxx	-	AVRH ± 2	AVRH ± 7	LSB	
Total error	-	-	-	± 3	± 8	LSB	
Conversion time	-	-	0.5 *1	-	-	µs	AV_{CC} ≥ 4.5 V
Sampling time *2	t_S	-	0.15	-	10	µs	AV_{CC} ≥ 4.5 V
			0.3	-			AV_{CC} < 4.5 V
Compare clock cycle*3	t_{CCK}	-	25	-	1000	ns	AV_{CC} ≥ 4.5 V
			50	-	1000		AV_{CC} < 4.5 V
State transition time to operation permission	t_{STT}	-	-	-	1.0	µs	
Power supply current (analog + digital)	-	AVCC	-	0.69	0.92	mA	A/D 1 unit operation
			-	1.3	22	µA	When A/D stop
Reference power supply current (AVRH)	-	AVRH	-	1.1	1.97	mA	A/D 1 unit operation AVRH = 5.5 V
			-	0.3	6.3	µA	When A/D stop
Analog input capacity	C_{AIN}	-	-	-	12.05	pF	
Analog input resistance	R_{AIN}	-	-	-	1.2	kΩ	AV_{CC} ≥ 4.5 V
					1.8		AV_{CC} < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	Anxx	-	-	5	µA	
Analog input voltage	-	Anxx	AV_{SS}	-	AVRH	V	
			AV_{SS}	-	AV_{CC}	V	
Reference voltage	-	AVRH	4.5	-	AV_{CC}	V	Tcck ＜50 ns
			2.7	-	AV_{CC}		Tcck ≥ 50 ns
	-	AVRL	AV_{SS}	-	AV_{SS}	V	

1: The conversion time is the value of sampling time (t_S) + compare time (t_C).
The condition of the minimum conversion time is when the value of Ts = 150 ns and Tc = 350 ns (AV_{CC} ≥ 4.5V). Ensure that it satisfies the value of sampling time (t_S) and compare clock cycle (t_{CCK}).
For setting of sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM4 Family Peripheral Manual Analog Macro Part (002-04860). The register setting of the A/D converter is reflected by the APB bus clock timing. For more information about the APB bus number to which the A/D converter is connected, see 1. S6E2G Series Block Diagram in this data sheet.
The sampling clock and compare clock are set at base clock (HCLK).

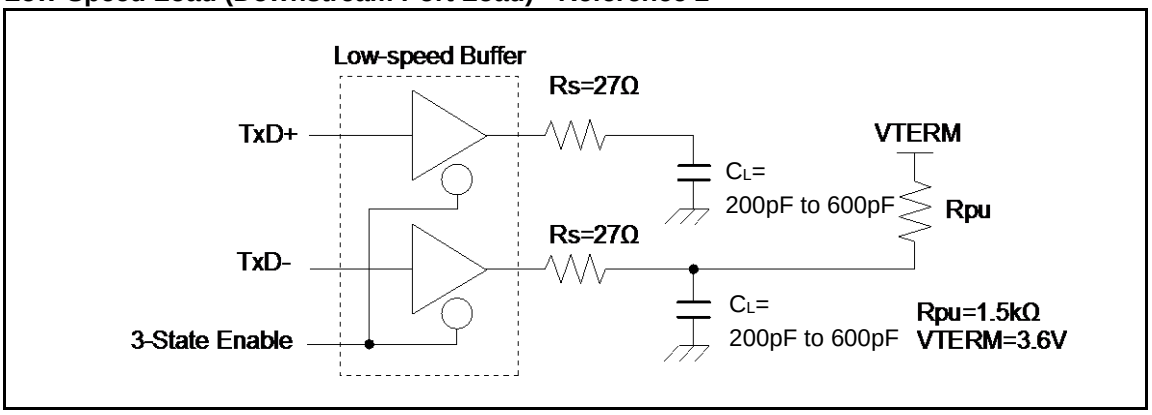
2: A necessary sampling time changes by external impedance. Ensure that it sets the sampling time to satisfy (Equation 1).

3: The compare time (t_C) is the value of (Equation 2).

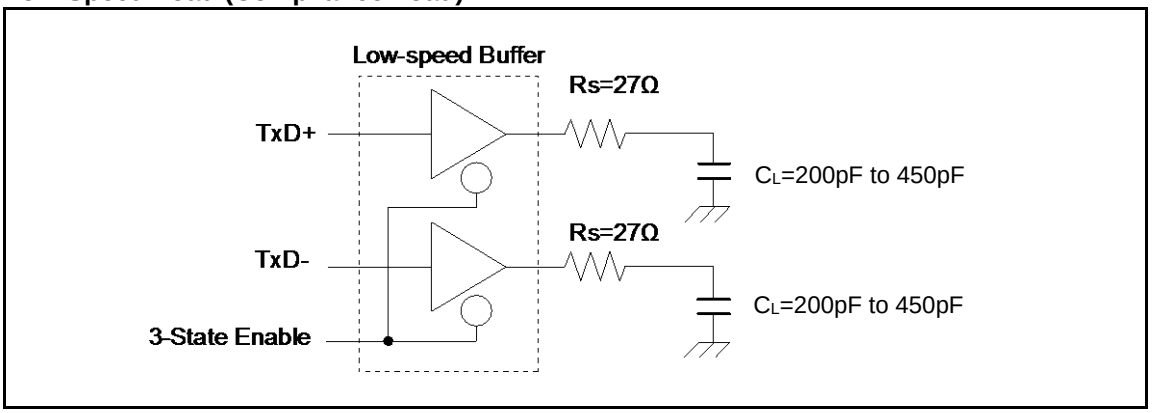
Low-Speed Load (Upstream Port Load) - Reference 1



Low-Speed Load (Downstream Port Load) - Reference 2

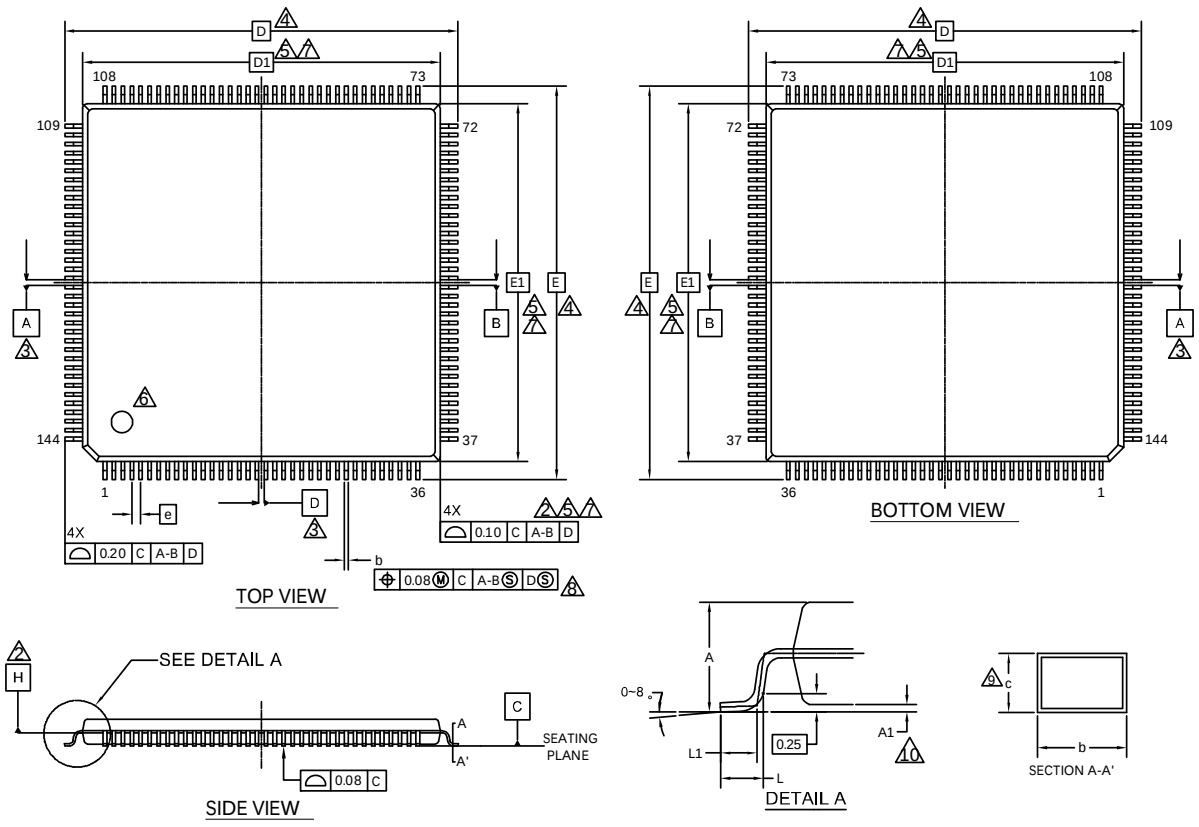


Low-Speed Load (Compliance Load)



14. Package Dimensions

Package Type	Package Code
LQFP 144	LQS144



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D		22.00 BSC	
D1		20.00 BSC	
e		0.50 BSC	
E		22.00 BSC	
E1		20.00 BSC	
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 144 LEAD LQFP
20.0X20.0X1.7 MM LQS144 REV*A

002-13015 *A