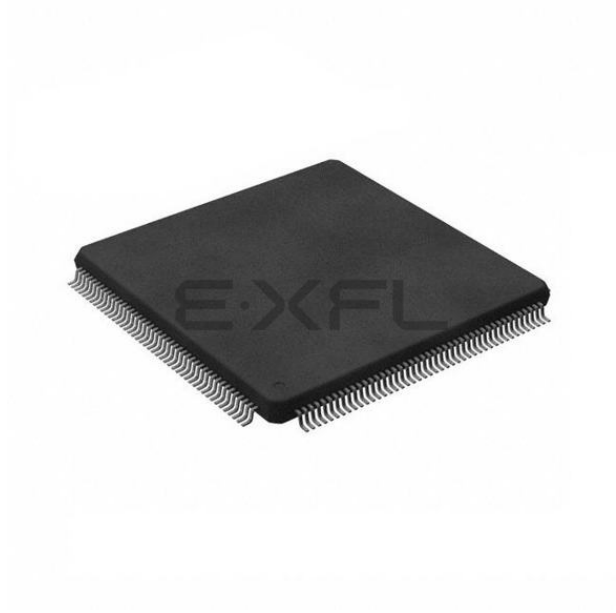

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, CSIO, EBI/EMI, Ethernet, I²C, LINbus, SmartCard, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	153
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2g28j0agv2000a

3. Package-Dependent Features

All S6E2G Series of parts are available in both 144-pin LQFP and 176-pin LQFP.

Description	Base Part Number S6E2G			
	Package Suffix			
	H0A	HHA*	J0A	JHA*
LQFP: (0.5 mm pitch)	144 pins		176 pins	
I/O Ports	121 pins (Max)		153 pins (Max)	
12-bit ADC converter	24 (3 units)		32 ch (3 units)	
Crypto Assist Function	—	Yes	—	Yes

*HHA and JHA parts have the Crypto Assist Function built in. HHA and JHA options are not available for the S6E2GH or S6E2G3 parts. The HHA and JHA options are available on the S6E2GM, S6E2GK, and S6E2G2 parts.

Notes:

- *For an explicit list of part numbers and the feature differences among them, see 13. Ordering Information*
- *See 14. Package Dimensions for detailed information on each package.*

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
127	103	P21	I	K
		ADTG_4		
		SIN0_0		
		INT27_0		
		CROUT_0		
128	104	P20	I	F
		NMIX		
		WKUP0		
129	105	USBVCC1	-	-
130	106	P82	H	R
		UDM1		
131	107	P83	H	R
		UDP1		
132	108	VSS	-	-
133	109	VCC	-	-
134	110	P00	E	G
		TRSTX		
135	111	P01	E	G
		TCK		
		SWCLK		
136	112	P02	E	G
		TDI		
137	113	P03	E	G
		TMS		
		SWDIO		
138	114	P04	E	G
		TDO		
		SWO		
139	-	P90	E	K
		RTO10_1 (PPG10_1)		
		TIOB0_1		
		INT12_1		
		IC0_CLK_1		
140	-	P91	E	K
		SIN5_1		
		RTO11_1 (PPG11_1)		
		TIOB1_1		
		INT13_1		
		IC0_VCC_1		

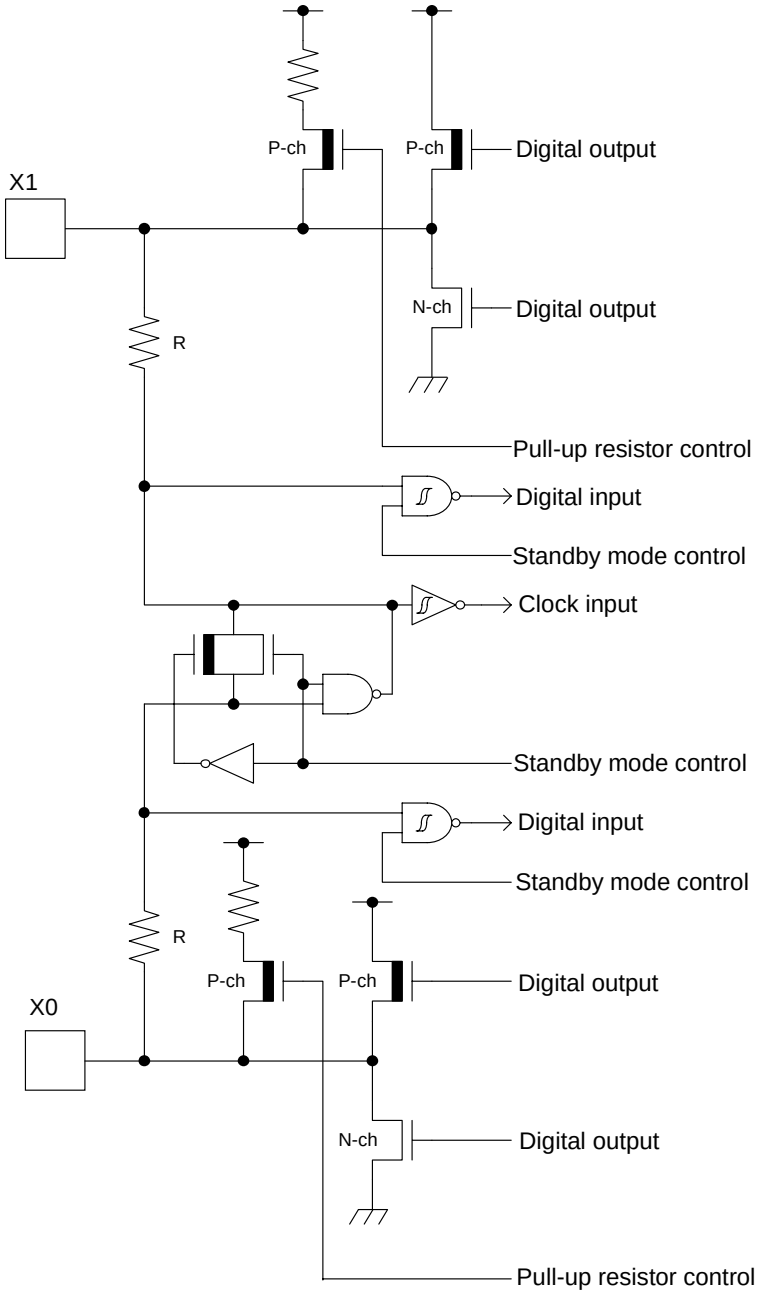
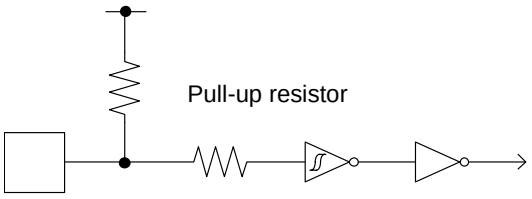
Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
Base Timer 15	TIOA15_0	Base Timer ch 15 TIOA pin	155	125
	TIOA15_1		58	-
	TIOB15_0	Base timer ch 15 TIOB pin	154	124
	TIOB15_1		59	-
CAN 0	TX0_0	CAN interface ch 0 TX output pin	101	85
	TX0_1		25	-
	TX0_2		59	-
	RX0_0	CAN interface ch 0 RX input pin	100	84
	RX0_1		24	-
	RX0_2		58	-
Debugger	SWCLK	Serial wire debug interface clock input pin	135	111
	SWDIO	Serial wire debug interface data input/ output pin	137	113
	SWO	Serial wire viewer output pin	138	114
	TCK	JTAG test clock input pin	135	111
	TDI	JTAG test data input pin	136	112
	TDO	JTAG debug data output pin	138	114
	TMS	JTAG test mode state input/output pin	137	113
	TRACECLK	Trace CLK output pin of ETM/HTM	114	90
	TRACED0	Trace data output pin of ETM/ Trace data output pin of HTM	98	82
	TRACED1		99	83
	TRACED2		100	84
	TRACED3		101	85
	TRACED4	Trace data output pin of HTM	106	86
	TRACED5		107	87
	TRACED6		108	88
	TRACED7		109	89
	TRACED8		102	-
	TRACED9		103	-
	TRACED10		104	-
	TRACED11		105	-
	TRACED12		110	-
	TRACED13		111	-
	TRACED14		112	-
	TRACED15		113	-
	TRSTX	JTAG test reset Input pin	134	110

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
External bus	MADATA00_0	External bus interface data bus (address/data multiplex bus)	2	2
	MADATA01_0		3	3
	MADATA02_0		4	4
	MADATA03_0		5	5
	MADATA04_0		6	6
	MADATA05_0		7	7
	MADATA06_0		8	8
	MADATA07_0		9	9
	MADATA08_0		13	10
	MADATA09_0		14	11
	MADATA10_0		15	12
	MADATA11_0		16	13
	MADATA12_0		17	14
	MADATA13_0		18	15
	MADATA14_0		19	16
	MADATA15_0		20	17
	MDQM0_0	External bus interface byte mask signal output pin	21	18
	MDQM1_0		22	19
	MALE_0	External bus interface address latch enable output signal for multiplex	171	139
	MRDY_0	External bus interface external RDY input signal	68	58
	MCLKOUT_0	External bus interface external clock output pin	23	20
	MNALE_0	External bus interface ALE signal to control NAND flash output pin	97	81
	MNCLE_0	External bus interface CLE signal to control NAND flash output pin	96	80
	MNREX_0	External bus interface read enable signal to control NAND flash	94	78
	MNWEX_0	External bus interface write enable signal to control NAND flash	95	79
	MOEX_0	External bus interface read enable signal for SRAM	169	137
	MWEX_0	External bus interface write enable signal for SRAM	170	138
	MSDCLK_0	SDRAM interface SDRAM clock output pin	65	55
	MSDCKE_0	SDRAM interface SDRAM clock enable pin	64	54
	MRASX_0	SDRAM interface SDRAM row active strobe pin	60	50
	MCASX_0	SDRAM interface SDRAM column active strobe pin	61	51
	MSDWEX_0	SDRAM interface SDRAM write enable pin	62	52

Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
GPIO	P00	General-purpose I/O port 0	134	110
	P01		135	111
	P02		136	112
	P03		137	113
	P04		138	114
	P08		21	18
	P09		22	19
	P0A		23	20
	P10	General-purpose I/O port 1	94	78
	P11		95	79
	P12		96	80
	P13		97	81
	P14		98	82
	P15		99	83
	P16		100	84
	P17		101	85
	P18		106	86
	P19		107	87
	P1A		108	88
	P1B		109	89
	P1C		114	90
	P1D		115	91
	P1E		116	92
	P1F		117	93
	P20	General-purpose I/O port 2	128	104
	P21		127	103
	P22		126	102
	P23		125	101
	P24		124	100
	P25		123	99
	P26		122	98
	P27		121	97
	P28		120	96
	P29		119	95
	P2A		118	94

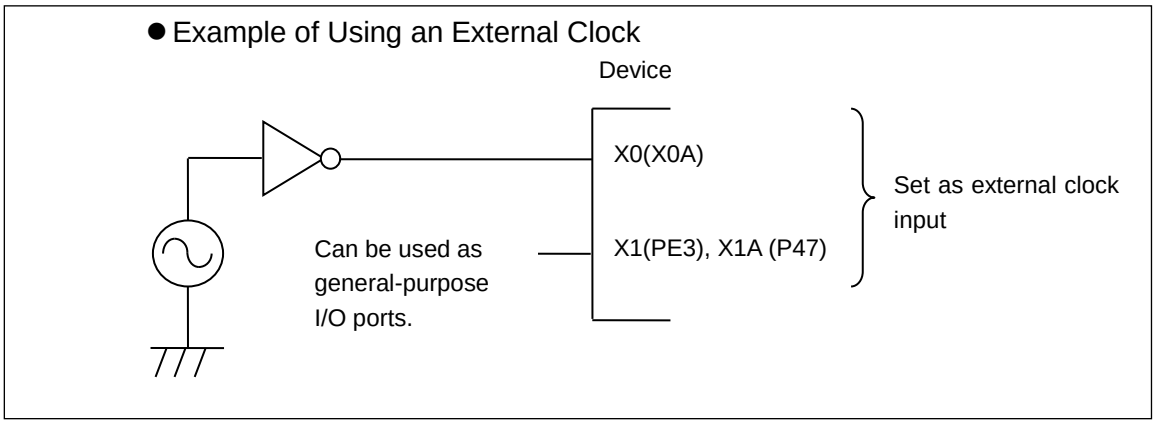
Module	Pin Name	Function	Pin Number	
			LQFP 176	LQFP 144
GPIO	P30	General-purpose I/O port 3	24	-
	P31		25	-
	P32		26	21
	P33		27	22
	P34		28	23
	P35		31	26
	P36		32	27
	P37		33	28
	P38		34	29
	P39		35	30
	P3A		36	31
	P3B		37	32
	P3C		38	33
	P3D		39	34
	P3E		40	35
	P40	General-purpose I/O port 4	46	38
	P41		47	39
	P42		48	40
	P43		49	41
	P44		50	42
	P45		51	43
	P46		55	47
	P47		56	48
	P48		60	50
	P49		61	51
	P4A		62	52
	P4B		63	53
	P4C		64	54
	P4D		65	55
	P4E		66	56
	P50	General-purpose I/O port 5	10	-
	P51		11	-
	P52		12	-
	P5D		41	-
	P5E		42	-
	P5F		43	-
	P60	General-purpose I/O port 6	172	140
	P61		171	139
	P62		170	138
	P63		169	137
	P64		168	-
	P65		167	-
	P6E		166	136

7. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main Oscillation/GPIO function. When the main oscillation is selected: ・ Oscillation feedback resistor: approximately 1 MΩ ・ Standby mode control When the GPIO is selected: ・ CMOS level output. ・ CMOS level hysteresis input ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA
B		・ CMOS level hysteresis input ・ Pull-up resistor: approximately 50 kΩ

Using an External Clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port. Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

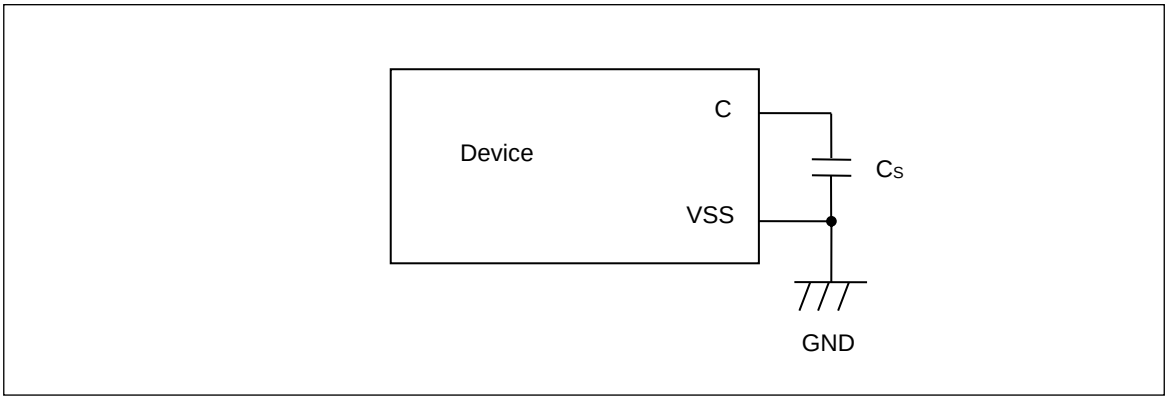


Handling When Using Multi-Function Serial Pin as I²C Pin

If the application uses the multi-function serial pin as an I²C pin, the P-channel transistor of the digital output must be disabled. I²C pins need to conform to electrical limitations like other pins, however, and avoid connecting to live external systems with the MCU power off.

C Pin

Devices in this series contain a regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor. Some laminated ceramic capacitors have a large capacitance variation due to thermal fluctuation. Please select a capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of the device. A smoothing capacitor of about 4.7 µF would be recommended for this series.



Mode Pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, the distance between the mode pins and VCC pins or VSS pins is as short as possible, and the connection impedance is low when the pins are pulled up/down such as for switching the pin level and rewriting the flash memory data. This is important to prevent the device from erroneously switching to test mode as a result of noise.

Start Address	End Address	Bus	Peripherals
0x4004_0000	0x4004_FFFF	AHB	USB ch 0
0x4005_0000	0x4005_FFFF		USB ch 1
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x4006_1FFF		DSTC register
0x4006_2000	0x4006_2FFF		CAN ch 0
0x4006_3000	0x4006_3FFF		Reserved
0x4006_4000	0x4006_5FFF		Ethernet-MAC ch 0
0x4006_6000	0x4006_6FFF		Ethernet-MAC setting register
0x4006_7000	0x4006_DFFF		Reserved
0x4006_E000	0x4006_EFFF		SD card I/F
0x4006_F000	0x4006_FFFF		GPIO
0x4007_0000	0x41FF_FFFF		Reserved

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
J	Analog output selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	*2	*3	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External interrupt enable selected					Maintain previous state	Maintain previous state			
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									
K	External interrupt enable selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0			
	GPIO selected									
L	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	GPIO selected									

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
Q	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	WKUP input enabled
	External interrupt enable selected							GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0			
	GPIO selected									
R	GPIO selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	USB I/O pin	Setting disabled	Setting disabled	Setting disabled	Hi-Z at trans-mission/ input enabled/ internal input fixed at 0 at reception	Hi-Z at trans-mission/ input enabled/ internal input fixed at 0 at reception	Hi-Z at trans-mission/ input enabled/ internal input fixed at 0 at reception	Hi-Z/ input enabled	Hi-Z/ input enabled	Hi-Z/ input enabled
S	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Sub crystal oscillator input pin/ external main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input Enabled

Table 12-4 Typical and Maximum Current Consumption in Normal Operation (Other than PLL), Code with Data Accessing Running from Flash Memory (Flash 0 Wait-Cycle Mode and Read Access 0 Wait)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *6, *7 (main oscillation)	*5	4 MHz	4.3	62	mA	*3 When all peripheral clocks are on
						3.7	61	mA	*3 When all peripheral clocks are off
			Normal operation *6 (built-in High-speed CR)	*5	4 MHz	3.5	61	mA	*3 When all peripheral clocks are on
						2.9	60	mA	*3 When all peripheral clocks are off
			Normal operation *6, *8 (sub oscillation)	*5	32 kHz	0.47	58	mA	*3 When all peripheral clocks are on
						0.46	58	mA	*3 When all peripheral clocks are off
			Normal operation *6 (built-in low-speed CR)	*5	100 kHz	0.51	58	mA	*3 When all peripheral clocks are on
						0.50	58	mA	*3 When all peripheral clocks are off

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are input and are fixed at 0

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

5: When operating flash 0 wait-cycle mode and read access 0 wait (FRWTR.RWT = 00, FBFCR.SD = 000)

6: With data access to a MainFlash memory.

7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

8: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

12.4.4 Operating Conditions of Main PLL (in the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (lock up time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	400	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	180	MHz	

1: Time from when the PLL starts operating until the oscillation stabilizes

2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).

12.4.5 Operating Conditions of USB/Ethernet PLL (in the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (lock up time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	400	MHz	USB/Ethernet
USB/Ethernet clock frequency *2	f_{CLKPLL}	-	-	50	MHz	After the M frequency division

1: Time from when the PLL starts operating until the oscillation stabilizes

2: For more information about USB/Ethernet clock, see Chapter 2-2: USB/Ethernet Clock Generation in FM4 Family Peripheral Manual Communication Macro Part (002-04862).

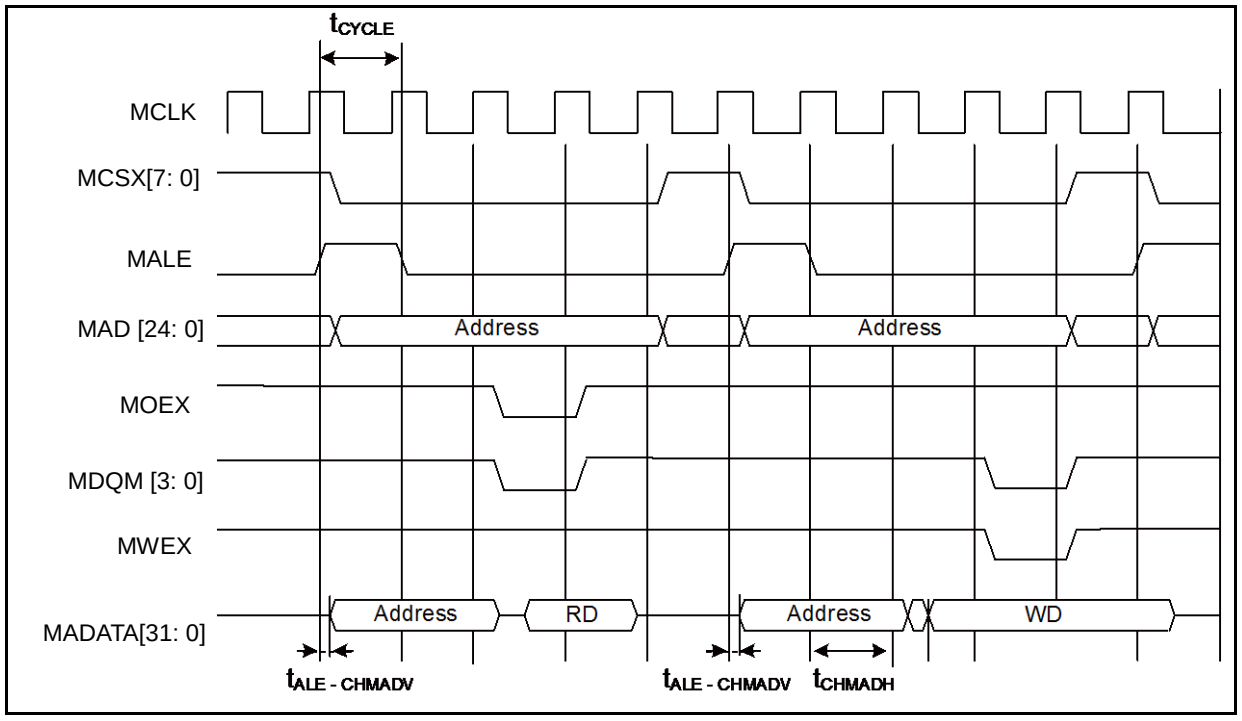
Multiplexed Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Multiplexed address delay time	$t_{ALE-CHMADV}$	MALE, MAD[24: 0]	-	0	10	ns	
Multiplexed address hold time	t_{CHMADH}		-	MCLK×n+0	MCLK×n+10	ns	

Note:

- *When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16)*

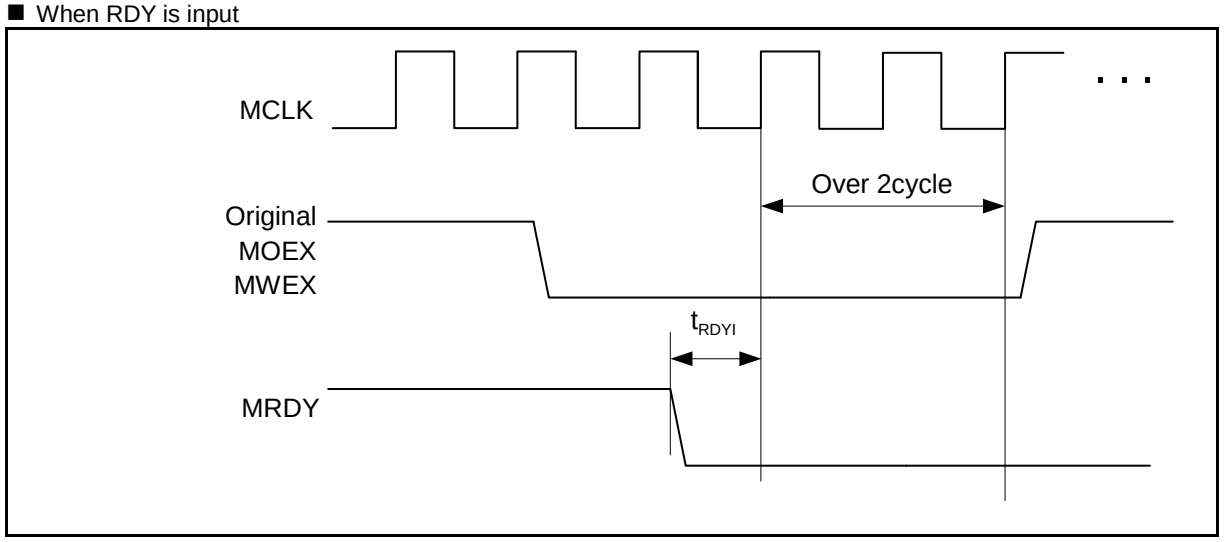


External Ready Input Timing

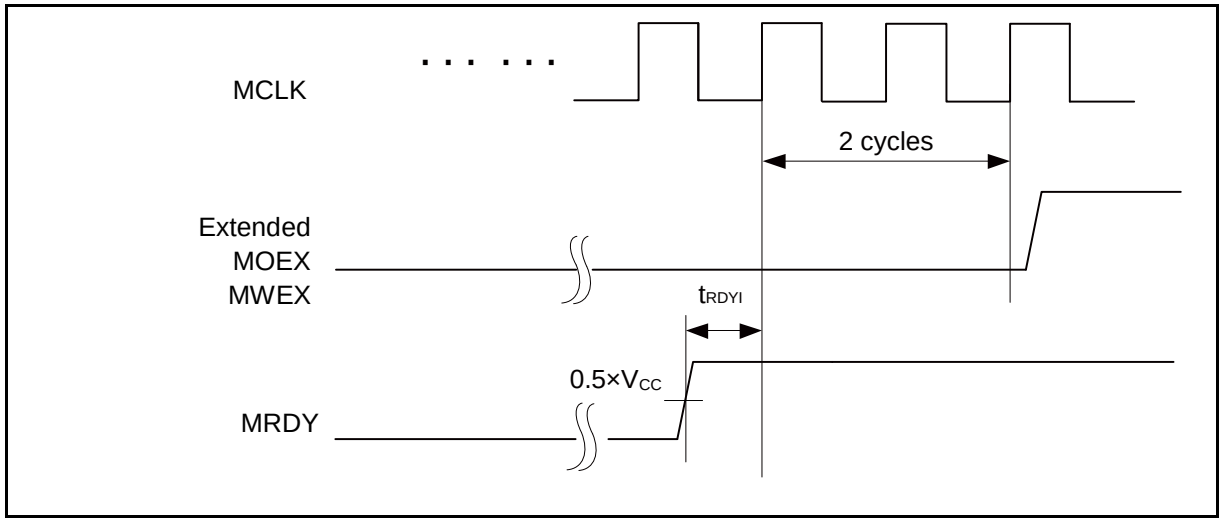
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

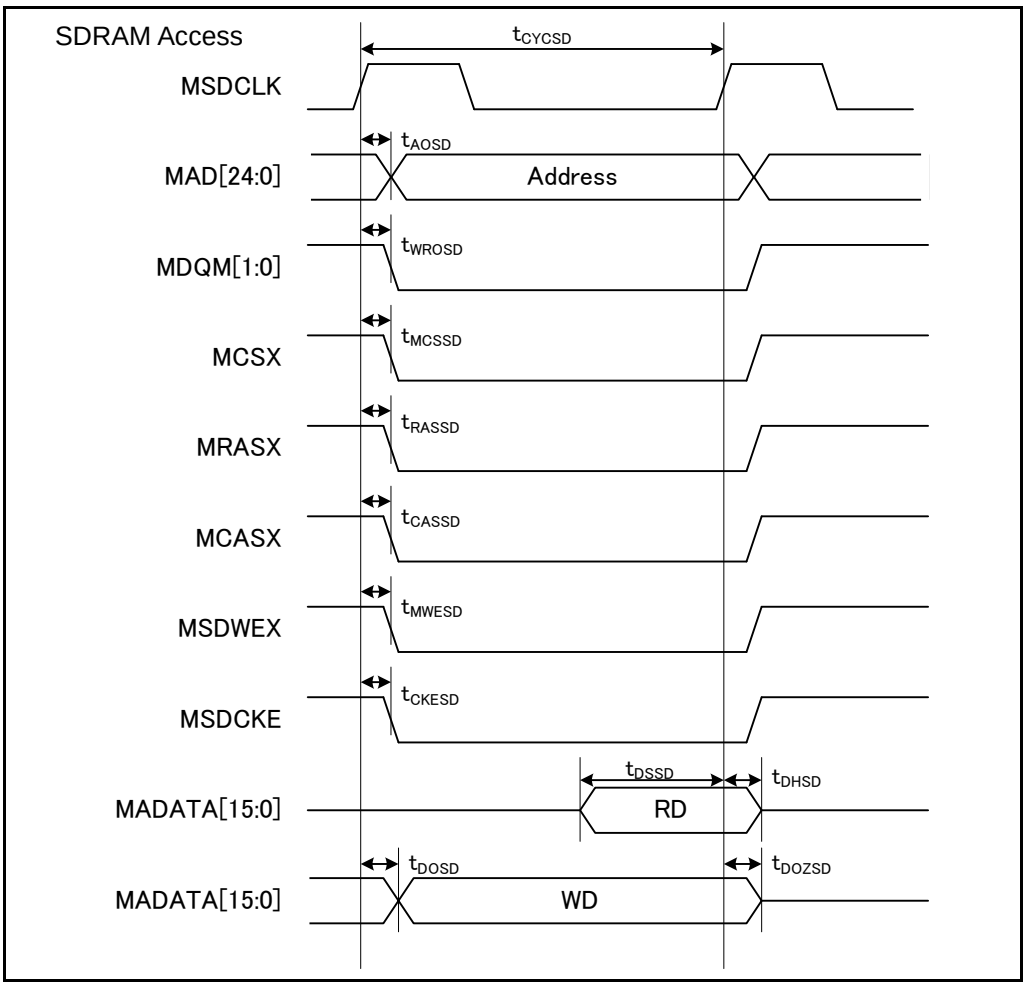
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK↑ MRDY input setup time	t_{RDYI}	MCLK, MRDY	-	19	-	ns	

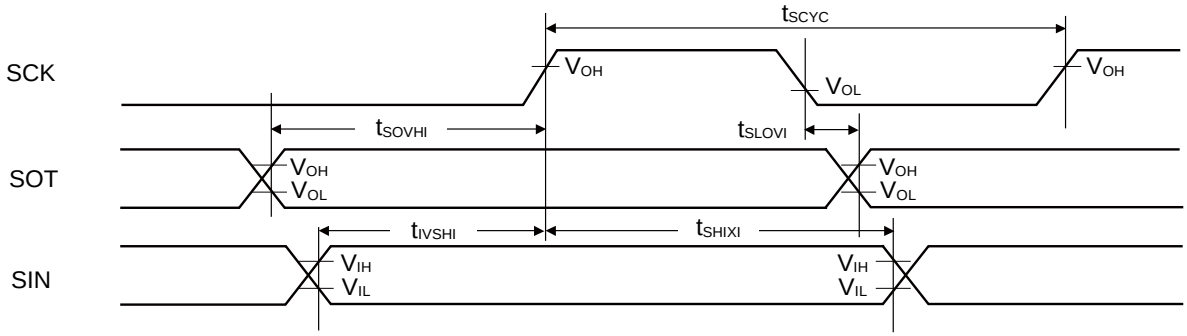
■ When RDY is input



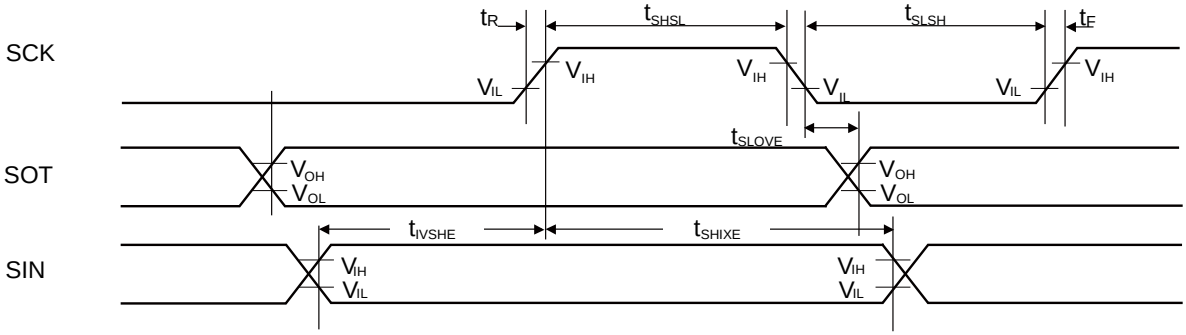
■ When RDY is released



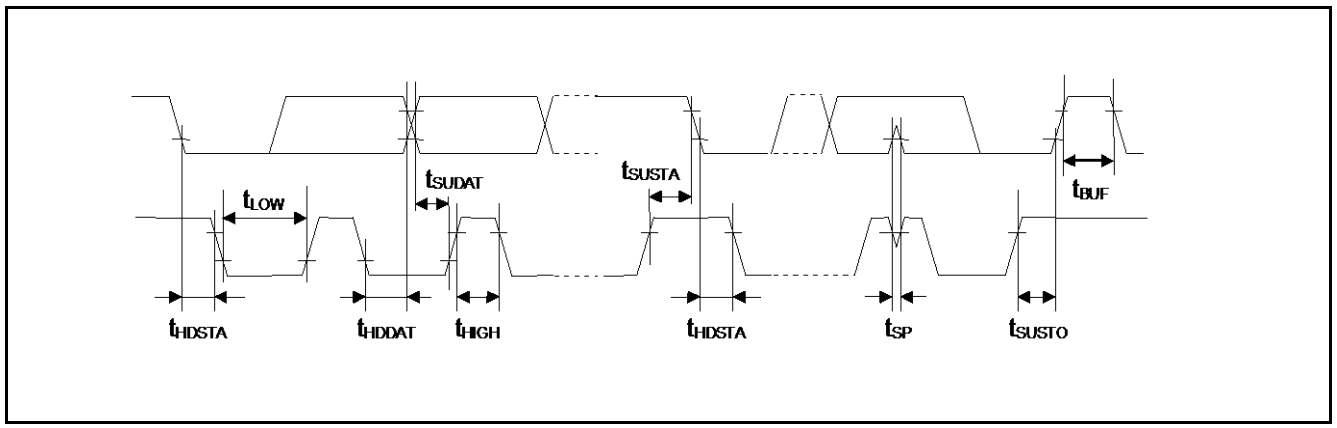

SDRAM Access
tCYCSD
MSDCLK
tAOSD
MAD[24:0]
Address
tWROSD
MDQM[1:0]
tMCSSD
MCSX
tRASSD
MRASX
tCASSD
MCASX
tMWESD
MSDWEX
tCKESD
MSDCKE
tDSSD
tDHSD
MADATA[15:0]
RD
tDOSD
tDOZSD
MADATA[15:0]
WD



MS bit = 0



MS bit = 1

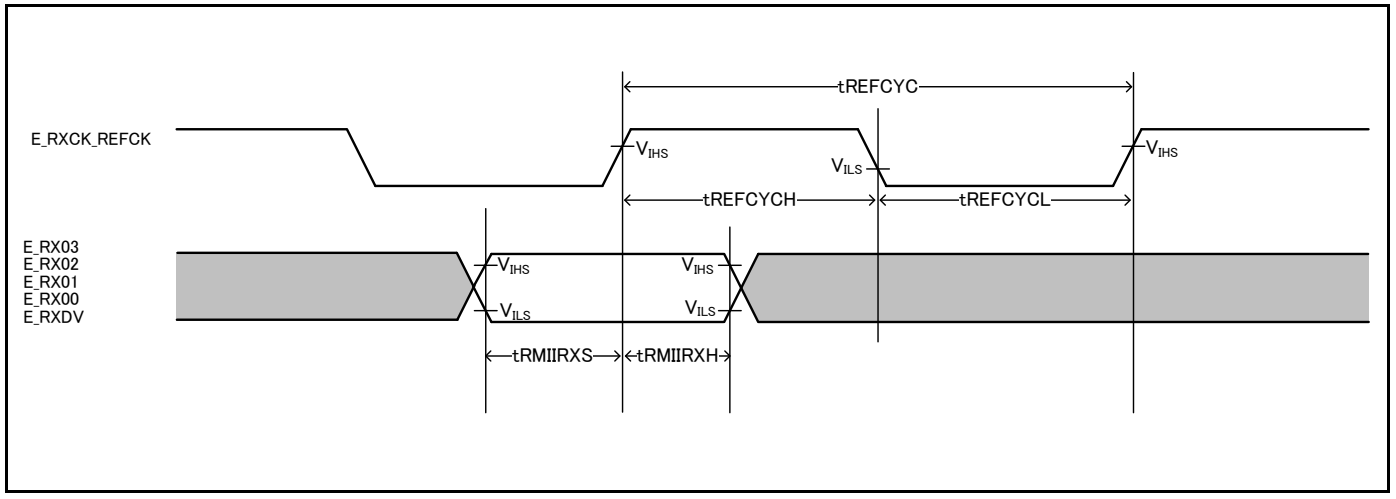

tLOW
tSUDAT
tSUSTA
tBUF
tHDSTA
tHDDAT
tHIGH
tHDSTA
tSP
tSUSTO

RMII Receiving (100 Mbps/10 Mbps)

($ETHV_{CC}$ = 3.0V to 3.6V, 4.5V to 5.5V, V_{SS} = 0V, C_L = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Reference clock cycle time*	t_{REFCYC}	E_RXCK_REFCK	20 ns (typical)	-	-	ns
Reference clock High-pulse-width duty cycle	$t_{REFCYCH}$	E_RXCK_REFCK	$t_{REFCYCH}/t_{REFCYC}$	35	65	%
Reference clock Low-pulse-width duty cycle	$t_{REFCYCL}$	E_RXCK_REFCK	$t_{REFCYCL}/t_{REFCYC}$	35	65	%
Received data → REFCK ↑ Setup time	$t_{RMIIRXS}$	E_RX03, E_RX02, E_RX01, E_RX00, E_RXDV	-	4	-	ns
REFCK ↑ → Received data Hold time	$t_{RMIIRXH}$	E_RX03, E_RX02, E_RX01, E_RX00, E_RXDV	-	2	-	ns

*: The reference clock is fixed to 50 MHz in the RMII specifications.
The clock accuracy should meet the PHY-device specifications.



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